Date: Apr. 21, 2016

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A061A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G1F Descriptions in the Hardware User's Manual Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G1F Group	Lot No. All lots	Reference Document	RL78/G1F User's Manual: Hardware Rev.1.00 R01UH0516EJ0100 (Apr. 2015)		

This document describes misstatements found in the RL78/G1F User's Manual: Hardware Rev.1.00 (R01UH0516EJ0100).

Corrections

Applicable Item	Applicable Page	Contents
1.3.2 32-pin products ·32-pin plastic LQFP (7x7mm,0.8mm pitch)	Page 7	Incorrect descriptions revised
2.1.2 32-pin products	Page 18	Incorrect descriptions revised
2.1.3 36-pin products	Page 20	Incorrect descriptions revised
2.1.4 48-pin products	Page 22	Incorrect descriptions revised
2.1.5 64-pin products	Page 24	Incorrect descriptions revised
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8.3.9 Timer RD output control register (TRDOCR) Figure 8-12 Format of Timer RD output control register (TRDOCR) [Reset Synchronous PWM Mode, Complementary PWM Mode]	—	Specification added
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8.8.3.2 Hardware release (HS_SEL = 0) Figure 8 - 78 Operation example of hardware cutoff release Function (an example of TRDIOB0 and TRDIOD0)	Page 435	Incorrect descriptions revised
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8.8.3.3 Software cutoff release (HS_SEL = 1) Figure 8 - 87 Operation example of output cutoff release by software	Page 444	Incorrect descriptions revised
17.1 Functions of Comparator Table 17 - 1 CMP Function Overview	Page 621	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items				Pages in this document for corrections
		Document No.	English	R01UH0516EJ0100	
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15	2.4 Pin Block Diagrams Figure 2-24 Pin Block Diagram of Pin Type 8-9-2			Page 54	Page 18
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18	8.3.11 Timer RD control register i (TRDCRi) (i = 0 or 1) Figure 8-18 Format of Timer RD control register 0 (TRDCR0) [Complementary PWM Mode]	Page 346	Page 21
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26	8.8.3.3 Software cutoff release (HS_SEL = 1) Figure 8-87 Operation example of output cutoff release by software	Page 444	Page 27
27	17.1 Functions of Comparator Table 17-1 CMP Function Overview	Page 621	Page 28

Incorrect,OLD: Bold with underline; Correct,NEW: Gray hatched

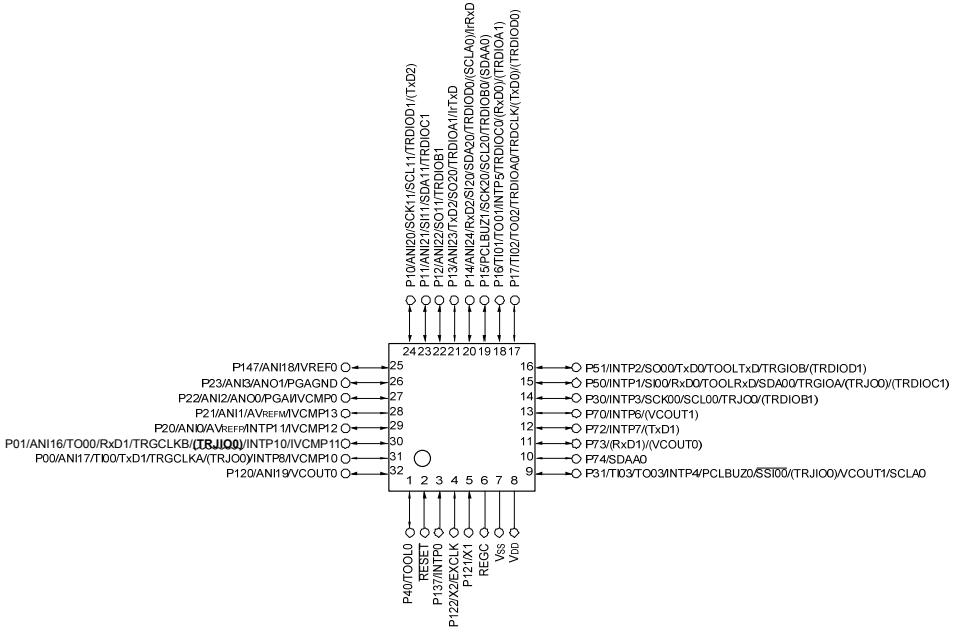
Revision History

RL78/G1F User's Manual: Hardware Rev.1.00 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A061A/E	Apr. 21, 2016	First edition issued No.1 to 27 in corrections (This notice)

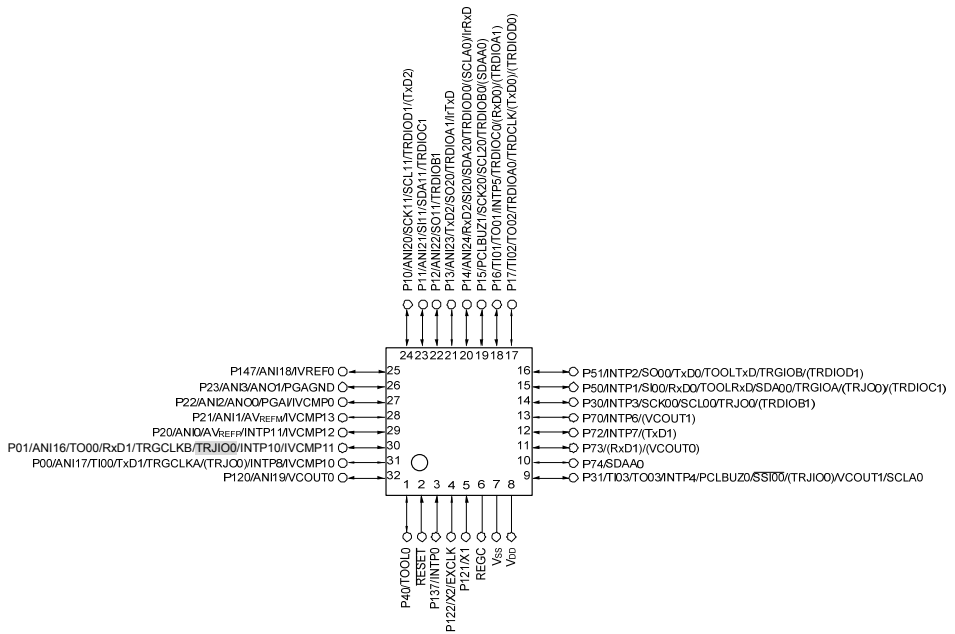
1. 1.3.2 32-pin products
   •32-pin plastic LQFP (7x7mm,0.8mm pitch) (Page 7)

Incorrect:



(Omitted)

Correct:



(Omitted)

2. 2.1.2 32-pin products (Page 18)

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P10	8-3-8	I/O	**Analog function**	ANI20/SCK11/SCL11/TRDIOD1 /(TxD2)	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (VDD tolerance). P10 to P14 can be set to analog input[Note].
P11	7-3-8			ANI21/SI11/SDA11/TRDIOC1	
P12	7-3-7			ANI22/SO11/TRDIOB1	
P13	7-3-8			ANI23/TxD2/SO20/TRDIOA1 /IrTxD	
P14	8-3-8			ANI24/RxD2/SI20/SDA20 /TRDIOD0/(SCLA0)/IrRxD	
P15	8-1-8			PCLBUZ1/SCK20/SCL20 /TRDIOB0/	
P16	8-1-7			TI01/TO01/INTP5/TRDIOC0 /(RxD0)/(TRDIOA1)	
P17	8-1-8			TI02/TO02/TRDIOA0/TRDCLK /(TxD0)/(TRDIOD0)	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P10	8-3-8	I/O	Analog function	ANI20/SCK11/SCL11/TRDIOD1 /(TxD2)	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (VDD tolerance). P10 to P14 can be set to analog input[Note].
P11	7-3-8			ANI21/SI11/SDA11/TRDIOC1	
P12	7-3-7			ANI22/SO11/TRDIOB1	
P13	7-3-8			ANI23/TxD2/SO20/TRDIOA1 /IrTxD	
P14	8-3-8			ANI24/RxD2/SI20/SDA20 /TRDIOD0/(SCLA0)/IrRxD	
P15	8-1-8	I/O	Input port	PCLBUZ1/SCK20/SCL20 /TRDIOB0/	
P16	8-1-7			TI01/TO01/INTP5/TRDIOC0 /(RxD0)/(TRDIOA1)	
P17	8-1-8			TI02/TO02/TRDIOA0/TRDCLK /(TxD0)/(TRDIOD0)	
(Omitted)					

3. 2.1.3 36-pin products (Page 20)

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P10	8-3-8	I/O	**Analog function**	ANI20/SCK11/SCL11/TRDIOD1 /(TxD2)	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (EVDD tolerance). P10 to P14 can be set to analog input[Note].
P11	7-3-8			ANI21/SI11/SDA11/TRDIOC1	
P12	7-3-7			ANI22/SO11/TRDIOB1	
P13	7-3-8			ANI23/TxD2/SO20/TRDIOA1 /IrTxD	
P14	8-3-8			ANI24/RxD2/SI20/SDA20 /TRDIOD0/(SCLA0)/IrRxD	
P15	8-1-8			PCLBUZ1/SCK20/SCL20 /TRDIOB0/(SDAA0)	
P16	8-1-7			TI01/TO01/INTP5/TRDIOC0 /(RxD0)/(TRDIOA1)	
P17	8-1-8			TI02/TO02/TRDIOA0/TRDCLK /(TxD0)/(TRDIOD0)	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P10	8-3-8	I/O	Analog function	ANI20/SCK11/SCL11/TRDIOD1 /(TxD2)	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (EVDD tolerance). P10 to P14 can be set to analog input[Note]
P11	7-3-8			ANI21/SI11/SDA11/TRDIOC1	
P12	7-3-7			ANI22/SO11/TRDIOB1	
P13	7-3-8			ANI23/TxD2/SO20/TRDIOA1 /IrTxD	
P14	8-3-8			ANI24/RxD2/SI20/SDA20 /TRDIOD0/(SCLA0)/IrRxD	
P15	8-1-8	I/O	Input port	PCLBUZ1/SCK20/SCL20 /TRDIOB0/(SDAA0)	
P16	8-1-7			TI01/TO01/INTP5/TRDIOC0 /(RxD0)/(TRDIOA1)	
P17	8-1-8			TI02/TO02/TRDIOA0/TRDCLK /(TxD0)/(TRDIOD0)	
(Omitted)					

4. 2.1.4 48-pin products (Page 22)

Incorrect:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P10	8-3-8	I/O	**Analog function**	ANI20/SCK11/SCL11/TRDIOD1 /(TxD2)	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (EVDD tolerance). P10 to P14 can be set to analog input[Note].
P11	7-3-8			ANI21/SI11/SDA11/TRDIOC1	
P12	7-3-7			ANI22/SO11/TRDIOB1	
P13	7-3-8			ANI23/TxD2/SO20/TRDIOA1 /IrTxD	
P14	8-3-8			ANI24/RxD2/SI20/SDA20 /TRDIOD0/(SCLA0)/IrRxD	
P15	8-1-8			PCLBUZ1/SCK20/SCL20 /TRDIOB0/(SDAA0)	
P16	8-1-7			TI01/TO01/INTP5/TRDIOC0 /(RxD0)/(TRDIOA1)	
P17	8-1-8			TI02/TO02/TRDIOA0/TRDCLK /(TxD0)/(TRDIOD0)	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P10	8-3-8	I/O	Analog function	ANI20/SCK11/SCL11/TRDIOD1 /(TxD2)	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (EVDD tolerance). P10 to P14 can be set to analog input[Note]
P11	7-3-8			ANI21/SI11/SDA11/TRDIOC1	
P12	7-3-7			ANI22/SO11/TRDIOB1	
P13	7-3-8			ANI23/TxD2/SO20/TRDIOA1 /IrTxD	
P14	8-3-8			ANI24/RxD2/SI20/SDA20 /TRDIOD0/(SCLA0)/IrRxD	
P15	8-1-8	I/O	Input port	PCLBUZ1/SCK20/SCL20 /TRDIOB0/	
P16	8-1-7			TI01/TO01/INTP5/TRDIOC0 /(RxD0)/(TRDIOA1)	
P17	8-1-8			TI02/TO02/TRDIOA0/TRDCLK /(TxD0)/(TRDIOD0)	
(Omitted)					

5. 2.1.5 64-pin products (Page 24)

Incorrect:

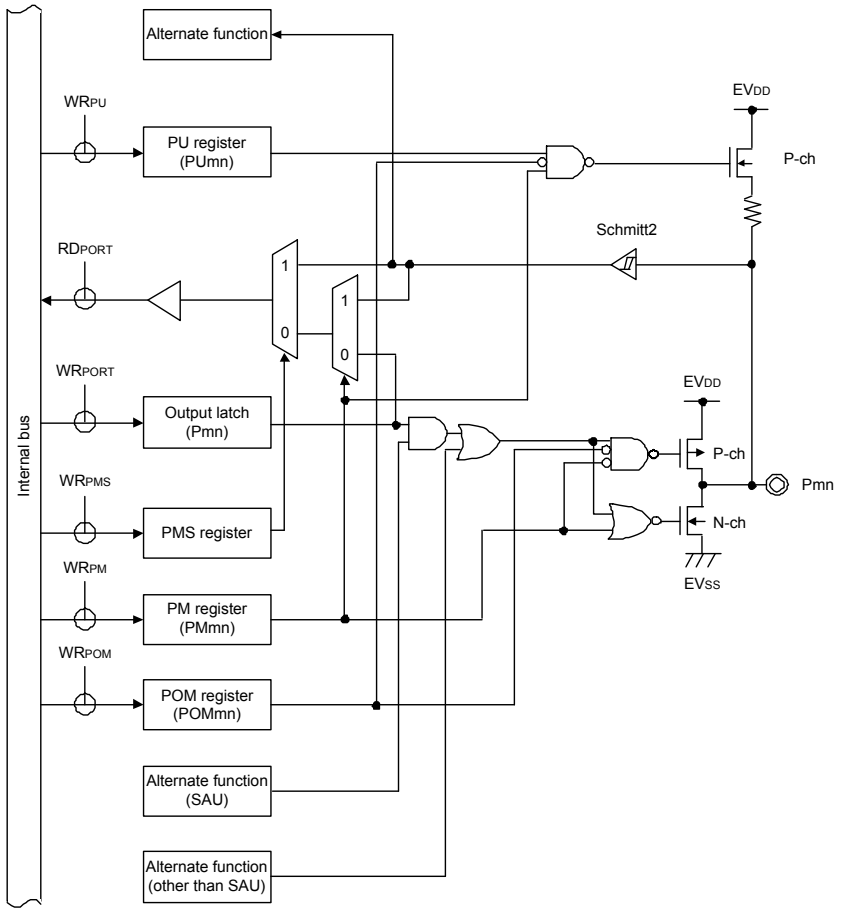
Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P10	8-3-8	I/O	Analog function	ANI20/SCK11/SCL11/TRDIOD1	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (EVDD tolerance). P10 to P14 can be set to analog input[Note].
P11	7-3-8			ANI21/SI11/SDA11/TRDIOC1	
P12	7-3-7			ANI22/SO11/TRDIOB1/(INTP5)	
P13	7-3-8			ANI23/TxD2/SO20/TRDIOA1 /IrTxD	
P14	8-3-8			ANI24/RxD2/SI20/SDA20/TRDI OD0/(SCLA0)/IrRxD	
P15	8-1-8			SCK20/SCL20/TRDIOB0 /(SDAA0)	
P16	8-1-7			TI01/TO01/INTP5/TRDIOC0 /(SI00/RxD0)/(TRDIOA1)	
P17	8-1-8			TI02/TO02/TRDIOA0/TRDCLK /(SO00/TxD0)/(TRDIOD0)	
(Omitted)					

Correct:

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
(Omitted)					
P10	8-3-8	I/O	Analog function	ANI20/SCK11/SCL11/TRDIOD1	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (EVDD tolerance). P10 to P14 can be set to analog input[Note]
P11	7-3-8			ANI21/SI11/SDA11/TRDIOC1	
P12	7-3-7			ANI22/SO11/TRDIOB1/(INTP5)	
P13	7-3-8			ANI23/TxD2/SO20/TRDIOA1 /IrTxD	
P14	8-3-8			ANI24/RxD2/SI20/SDA20/TRDI OD0/(SCLA0)/IrRxD	
P15	8-1-8	I/O	Input port	SCK20/SCL20/TRDIOB0 /(SDAA0)	
P16	8-1-7			TI01/TO01/INTP5/TRDIOC0 /(SI00/RxD0)/(TRDIOA1)	
P17	8-1-8			TI02/TO02/TRDIOA0/TRDCLK /(SO00/TxD0)/(TRDIOD0)	
(Omitted)					

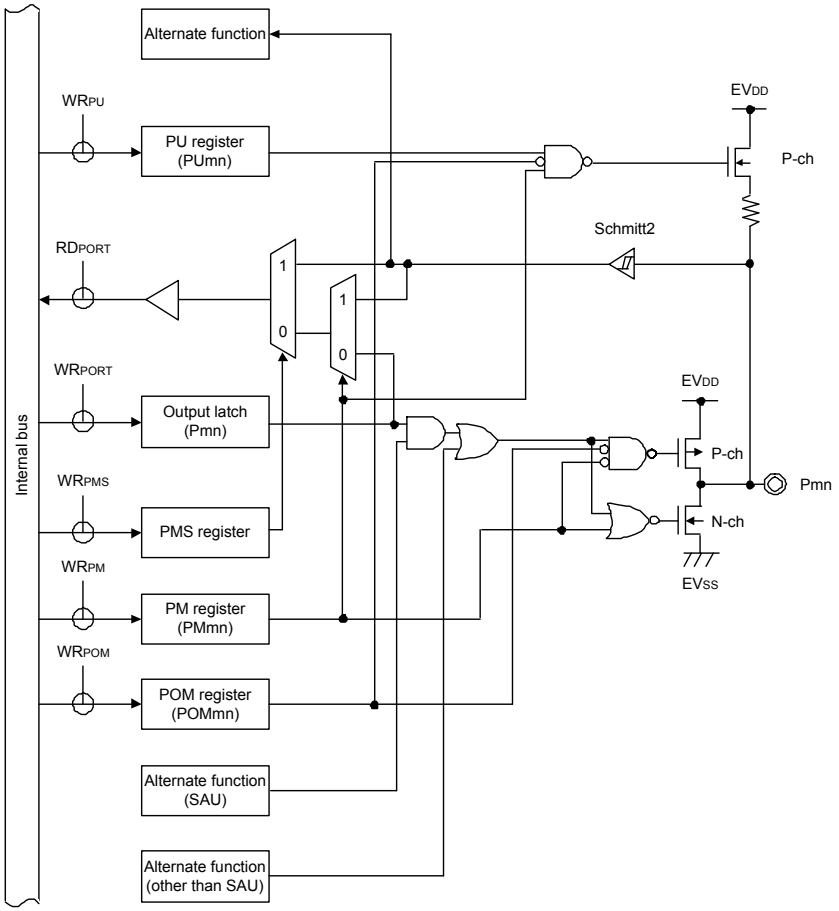
6. 2.4 Pin Block Diagrams
Figure 2-10 Pin Block Diagram of Pin Type 7-1-4 (Page 40)

Old:



Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

New:

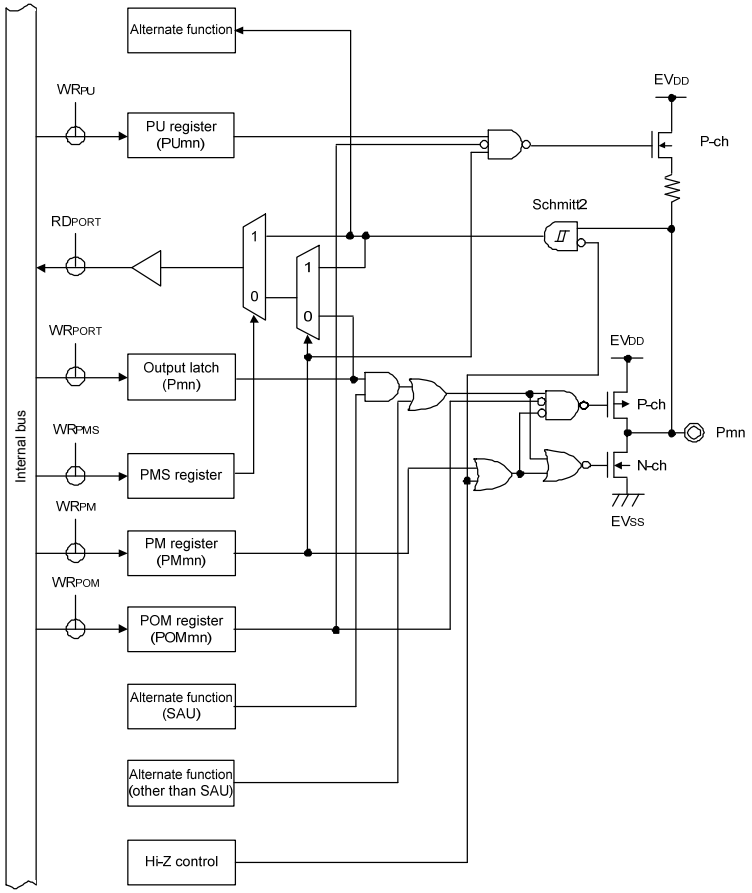


Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

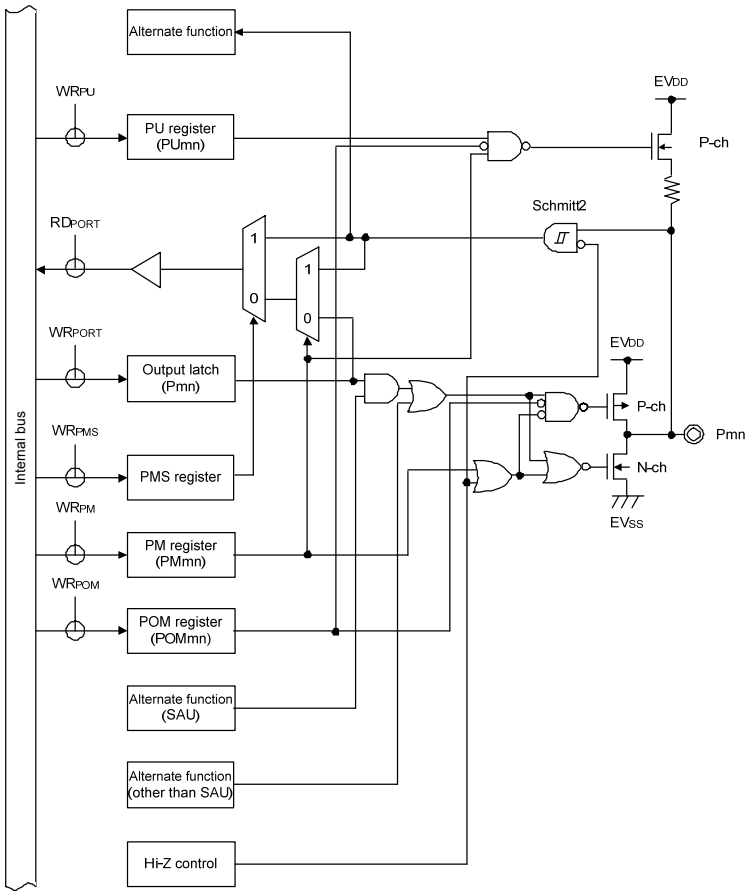
7. 2.4 Pin Block Diagrams
Figure 2-12 Pin Block Diagram of Pin Type 7-1-8 (Page 42)

Old:



Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

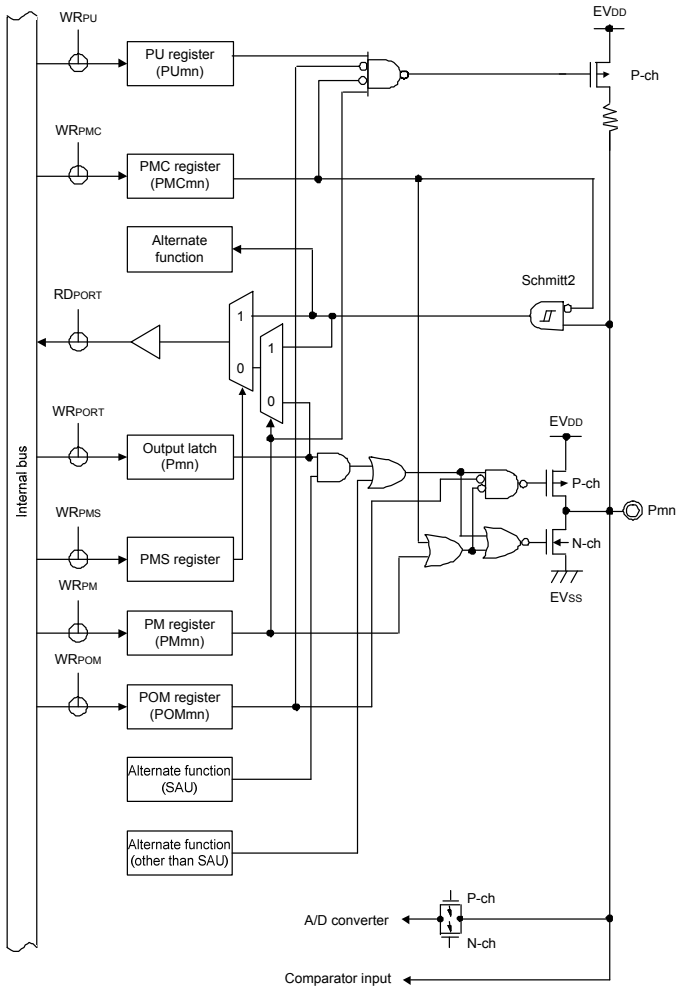
New:



Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).
Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

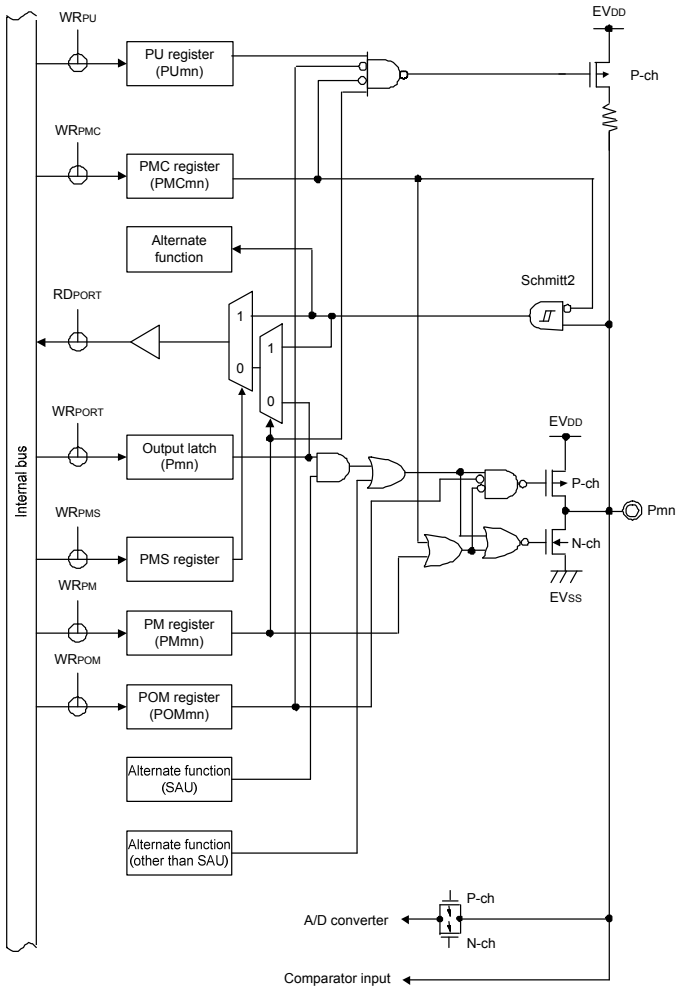
8. 2.4 Pin Block Diagrams
Figure 2-12 Pin Block Diagram of Pin Type 7-9-2 (Page 47)

Old:



Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

New:

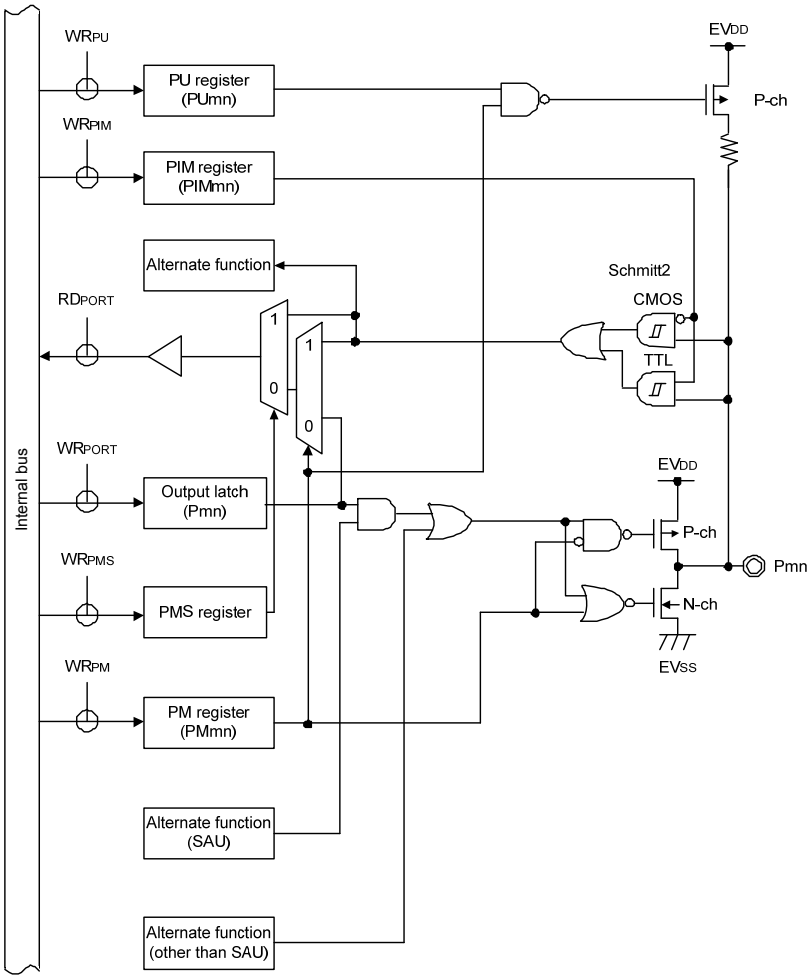


Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

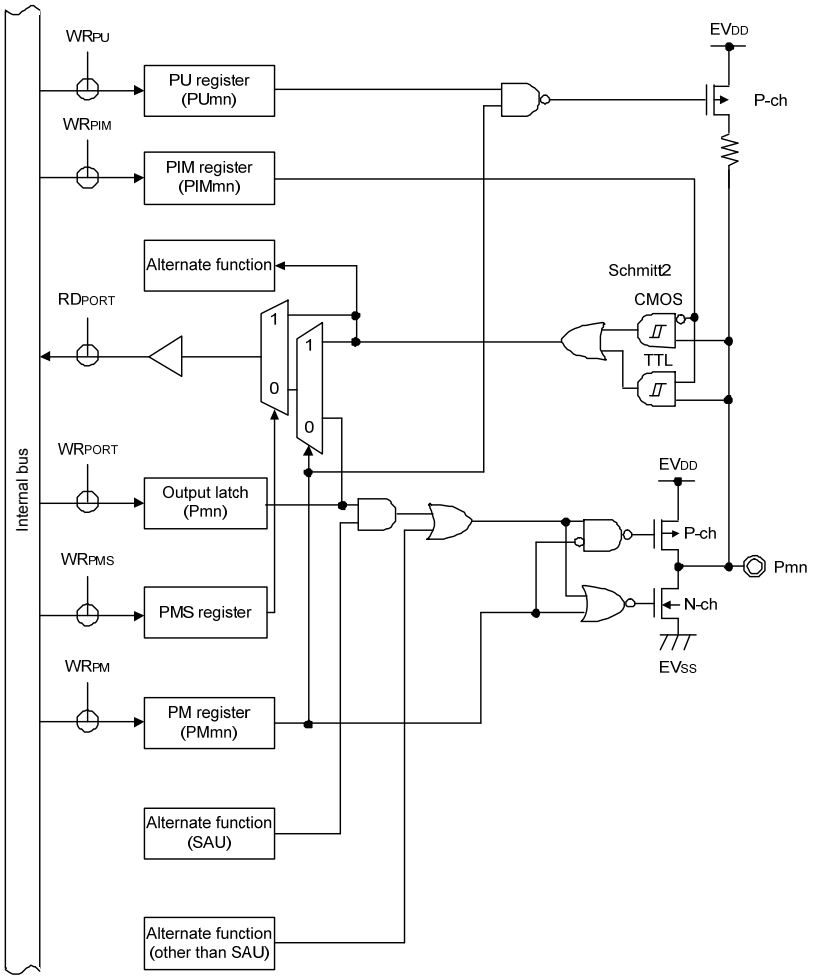
9. 2.4 Pin Block Diagrams
Figure 2-18 Pin Block Diagram of Pin Type 8-1-3 (Page 48)

Old:



Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

New:

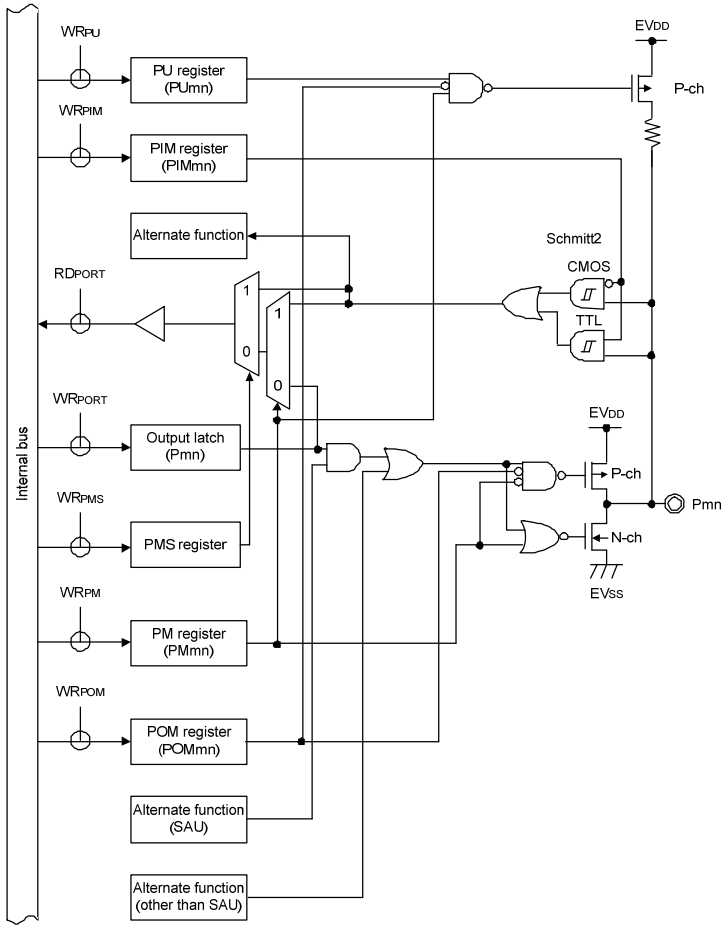


Caution Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

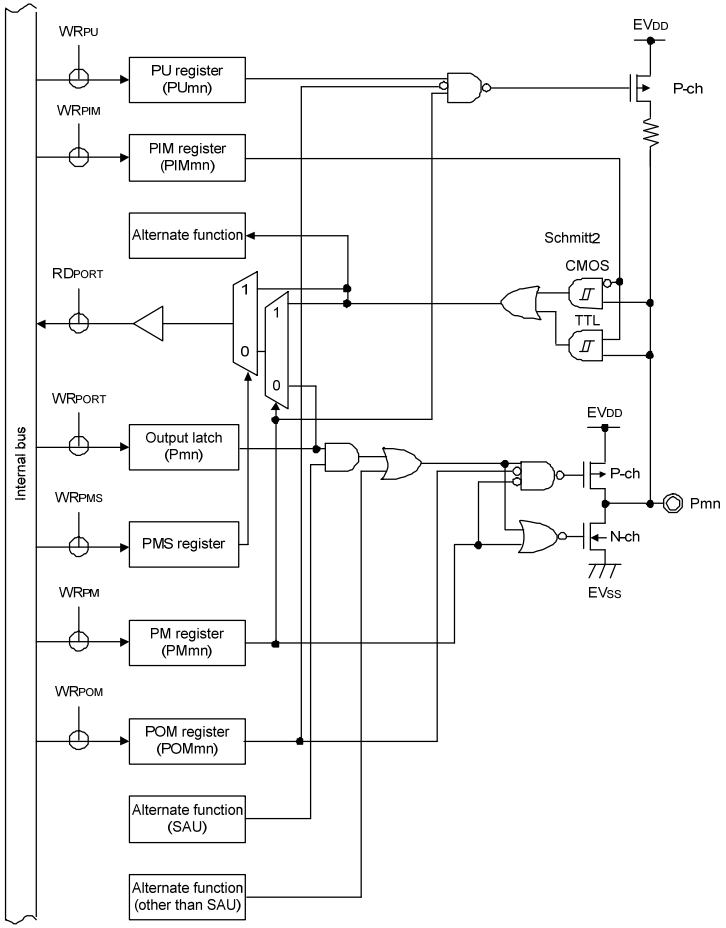
10. 2.4 Pin Block Diagrams
Figure 2-19 Pin Block Diagram of Pin Type 8-1-4 (Page 49)

Old:



Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

New:

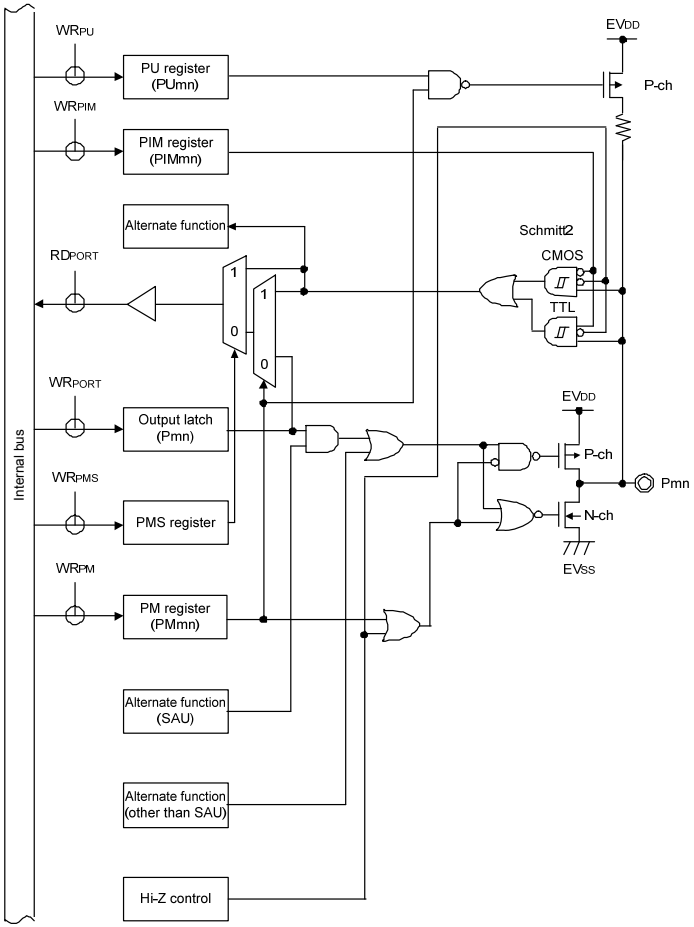


Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).
Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

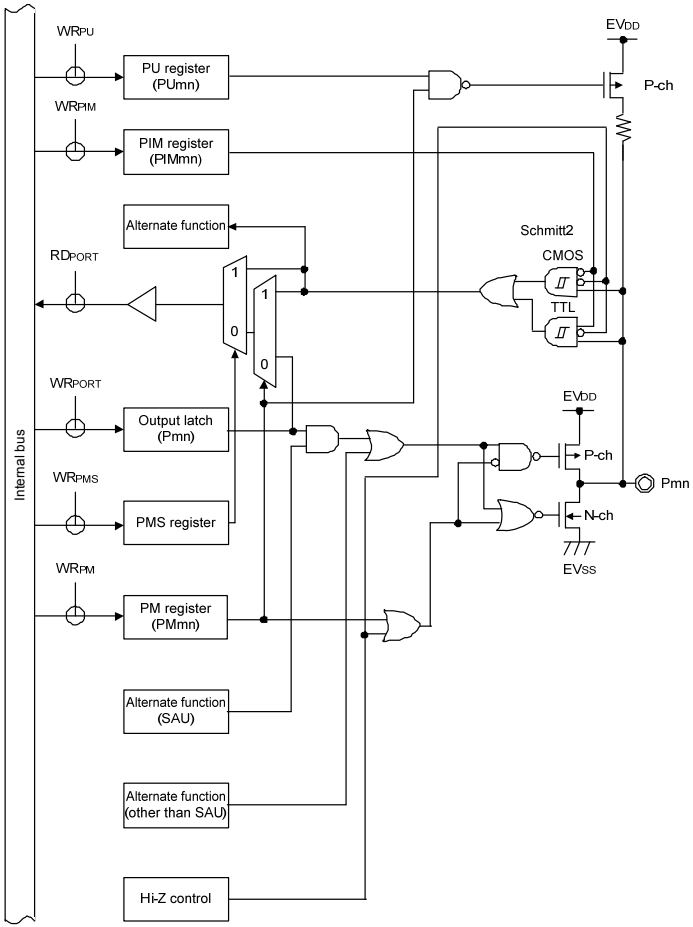
11. 2.4 Pin Block Diagrams
Figure 2-20 Pin Block Diagram of Pin Type 8-1-7 (Page 50)

Old:



Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

New:

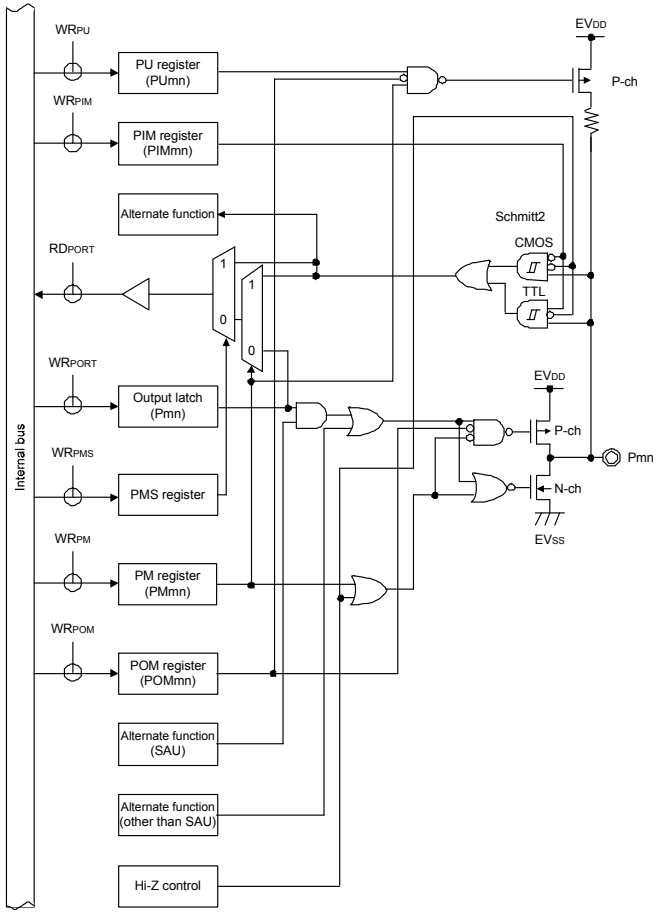


Caution Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

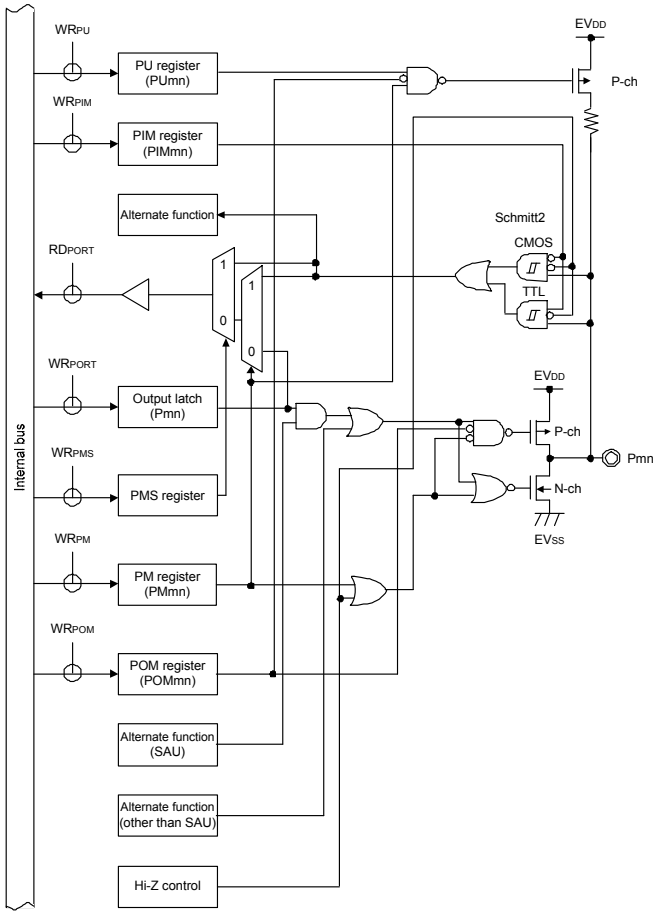
12. 2.4 Pin Block Diagrams
Figure 2-21 Pin Block Diagram of Pin Type 8-1-8 (Page 51)

Old:



Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

New:

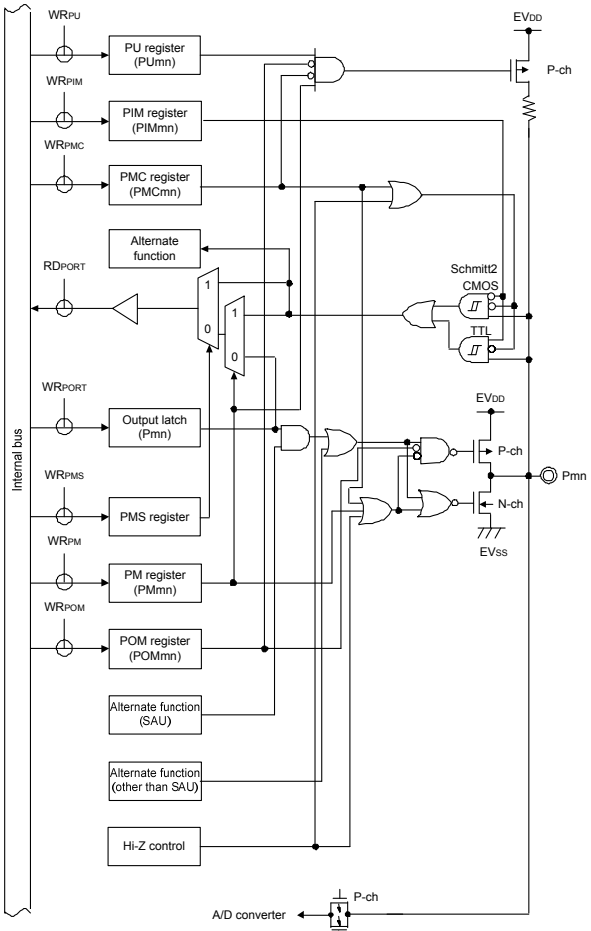


Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).
Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

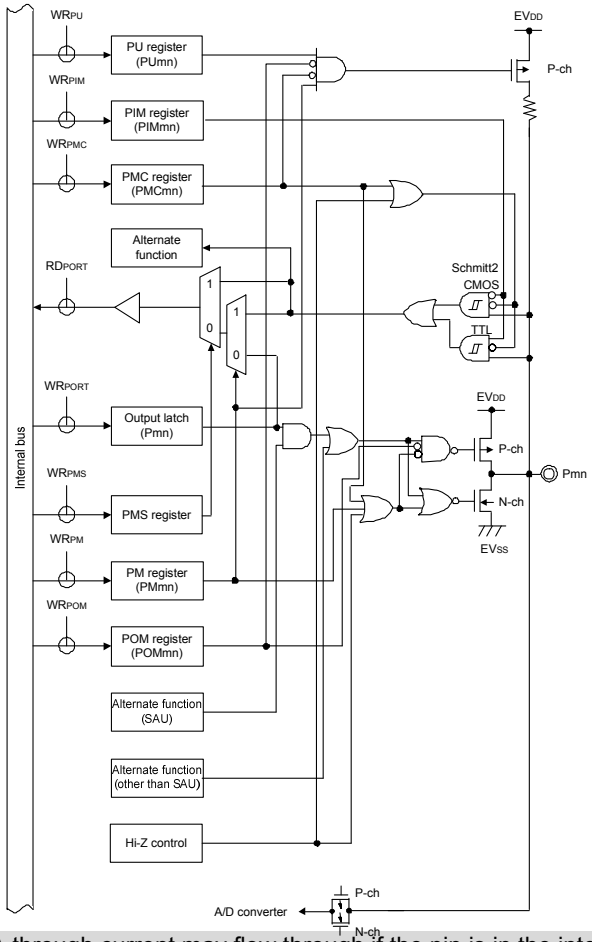
13. 2.4 Pin Block Diagrams
Figure 2-22 Pin Block Diagram of Pin Type 8-3-8 (Page 52)

Old:



Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

New:

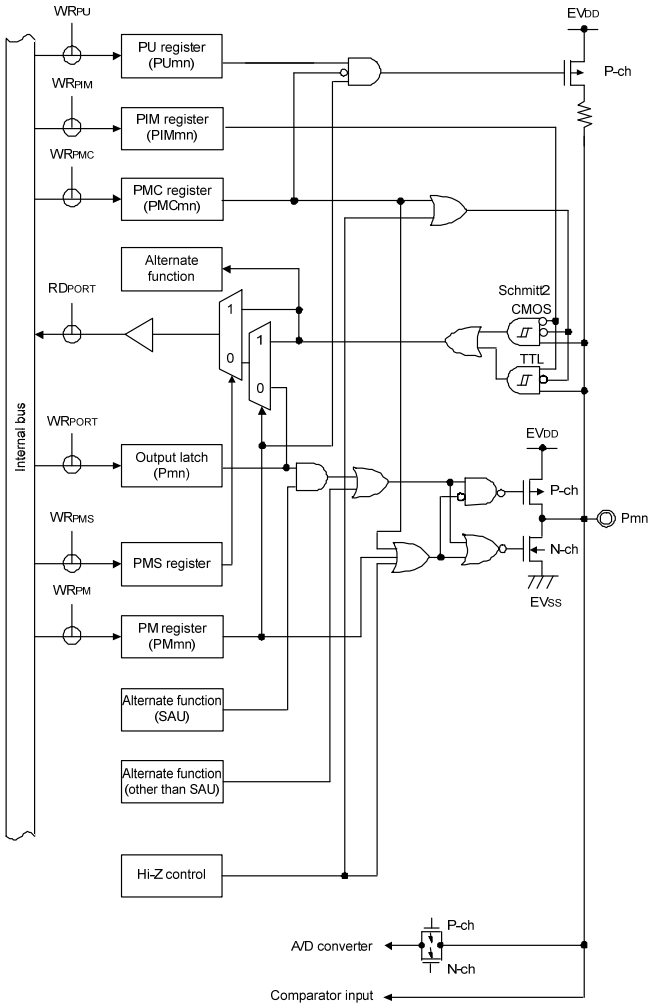


Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).
Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recom

Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

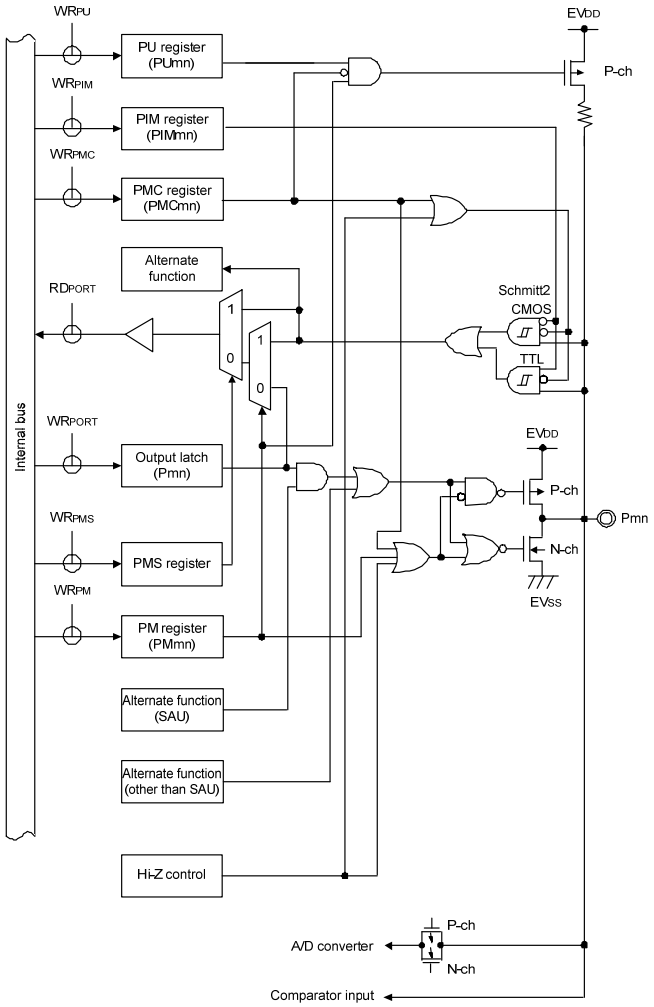
14. 2.4 Pin Block Diagrams
Figure 2-23 Pin Block Diagram of Pin Type 8-9-1 (Page 53)

Old:



Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

New:

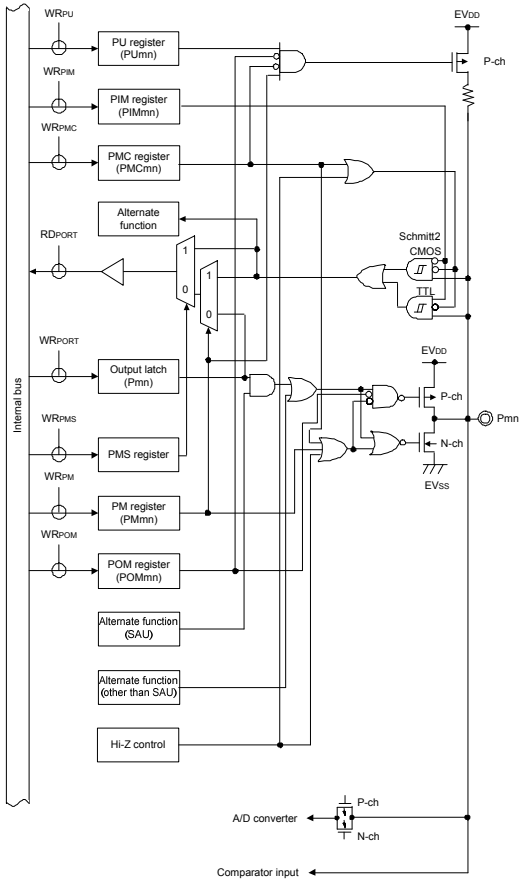


Caution Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

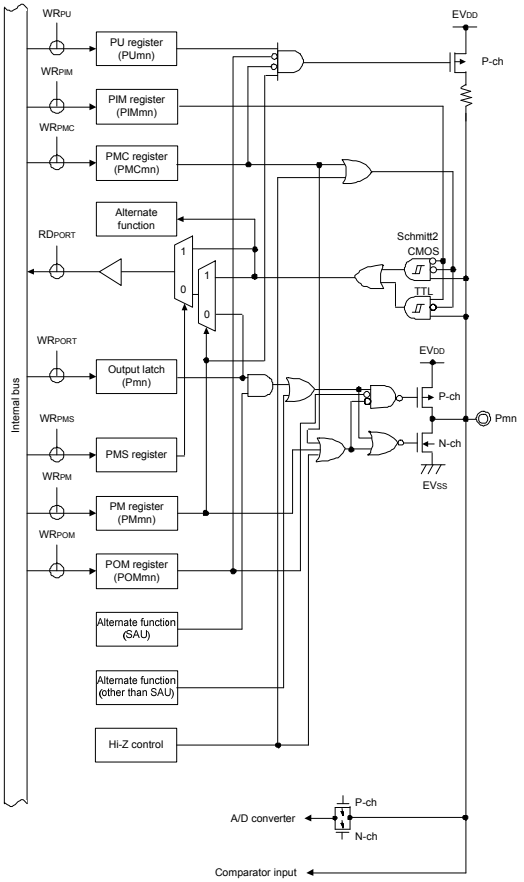
15. 2.4 Pin Block Diagrams
Figure 2-24 Pin Block Diagram of Pin Type 8-9-2 (Page 54)

Old:



Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

New:

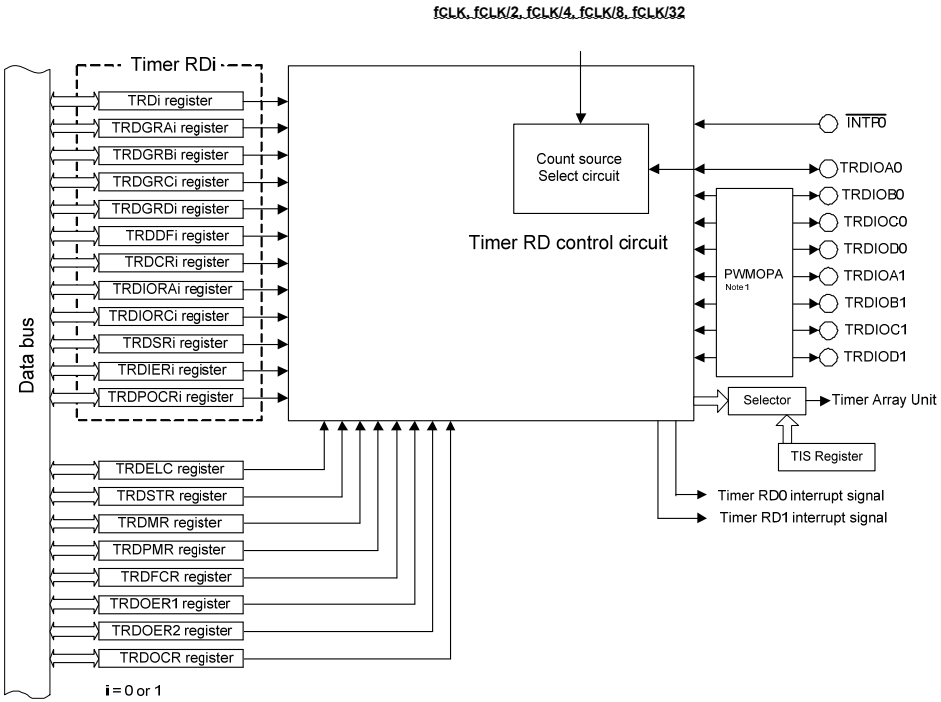


Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).
Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recom

Remark 1. Refer to 2.1 Port Functions for alternate functions.
Remark 2. SAU: Serial array unit

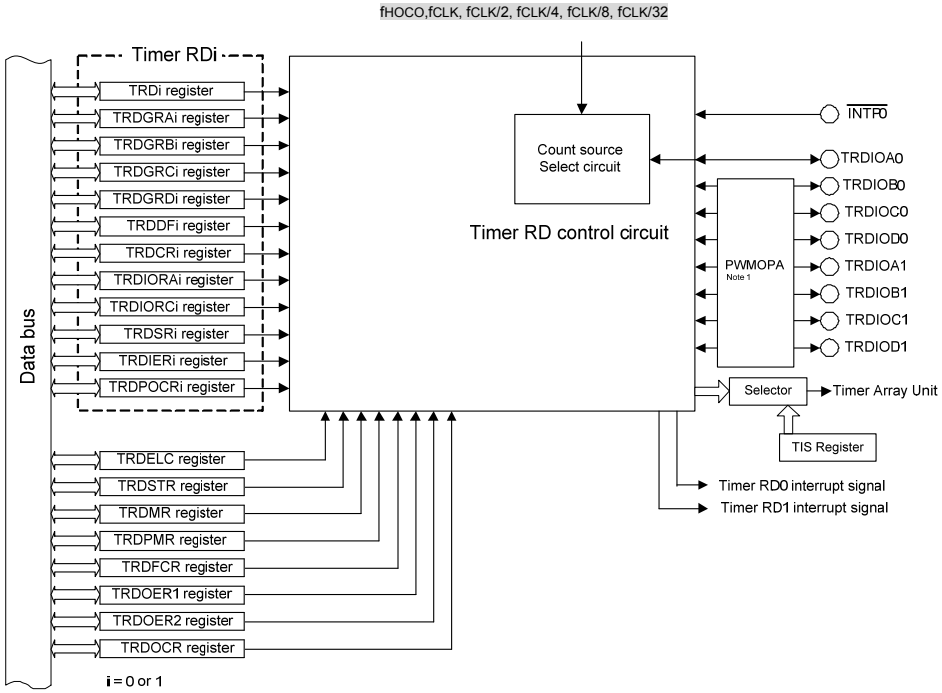
16. 8.2 Configuration of Timer RD
Figure 8-1 Timer RD Block Diagram (Page 327)

Incorrect:



Note 1. Output signals can be cut off, while input signals cannot.

Correct:



Note 1. Output signals can be cut off, while input signals cannot.

17. 8.3.9 Timer RD output control register (TRDOCR)
Figure 8-12 Format of Timer RD output control register (TRDOCR)
[Reset Synchronous PWM Mode, Complementary PWM Mode]

Old:

Nothing

New:

Figure 8 - 12 Format of Timer RD output control register (TRDOCR)
[Reset Synchronous PWM Mode, Complementary PWM Mode]

Address: F0269H After Reset: 00H Note 1 R/W

Symbol	7	6	5	4	3	2	1	0
TRDOCR	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0

TOD1,TOC1,TOB1, TOA1,TOD0, TOB0, TOA0	Setting these bits to 1 is invalid in the reset synchronous PWM mode and complementary PWM mode. Be sure to set these bits to 0. In the reset synchronous PWM mode and complementary PWM mode, the setting of the OLS1 and OLS0 bits in TRDFCR determine the initial level independently of the setting in these bits.

TOC0	TRDIOC1 initial output level select Note 2	
0	Initial output L	In the reset synchronous PWM mode, the output is inverted every PWM period. In complementary PWM mode, the output is inverted every 1/2 PWM period.
1	Initial output H	

Note 1. The value after reset is undefined when FRQSEL4 = 1 in the user option byte (000C2H) and TRD0EN = 0 in the PER1 register. If it is necessary to read the initial value, set fCLK to fIH and TRD0EN = 1 before reading.
Note 2. If the pin function is set for waveform output, the initial output level is output when the TRDOCR register is set.

18. 8.3.11 Timer RD control register i (TRDCRi) (i = 0 or 1)
Figure 8-18 Format of Timer RD control register 0 (TRDCR0)
[Complementary PWM Mode] (Page 346)

Incorrect:

Figure8-18 Format of Timer RD control register 0 (TRDCR0)
[Complementary PWM Mode]

Address: F0270H After Reset: 00H Note 1 R/W

Symbol	7	6	5	4	3	2	1	0
TRDCR0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0

(Omitted)

Correct:

Figure8-19 Format of Timer RD control register i (TRDCRi) (I = 0 or 1)
[Complementary PWM Mode]

Address: F0270H(TRDCR0), F0280H(TRDCR1) After Reset: 00H Note 1 R/W

Symbol	7	6	5	4	3	2	1	0
TRDCRi	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0

(Omitted)

19. 8.3.18 Timer RD counter i (TRDi) (i = 0 or 1)
Figure 8-31 Format of Timer RD counter i (TRDi) (i = 0 or 1)
[Reset Synchronous PWM Mode and PWM3 Mode](Page 362)

Incorrect:

Figure 8 - 31 Format of Timer RD counter i (TRDi) (i = 0 or 1)
[Reset Synchronous PWM Mode and PWM3 Mode]

Address: F0276H (TRD0), F0286H (TRD1) After Reset: 0000H Note R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDi																

(Omitted)

Correct:

Figure 8 - 32 Format of Timer RD counter 0 (TRD0)
[Reset Synchronous PWM Mode and PWM3 Mode]

Address: F0276H (TRD0) After Reset: 0000H Note R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRD0																

(Omitted)

20. 8.3.18 Timer RD counter i (TRDi) (i = 0 or 1)
Figure 8-32 Format of Timer RD counter i (TRDi) (i = 0 or 1) [Complementary PWM Mode (TRD0)] (Page 363)

Incorrect:

Figure 8 - 32 Format of Timer RD counter i (TRDi) (i = 0 or 1)
[Complementary PWM Mode (TRD0)]

Address: F0276H (TRD0), F0286H (TRD1) After Reset: 0000H Note R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDi																

(Omitted)

Correct:

Figure 8 - 33 Format of Timer RD counter 0 (TRD0)
[Complementary PWM Mode (TRD0)]

Address: F0276H (TRD0) After Reset: 0000H Note R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRD0																

(Omitted)

21. 8.3.18 Timer RD counter i (TRDi) (i = 0 or 1)
Figure 8-33 Format of Timer RD counter i (TRDi) (i = 0 or 1) [Complementary PWM Mode (TRD1)](Page 363)

Incorrect:

Figure 8 - 33 Format of Timer RD counter i (TRDi) (i = 0 or 1)
[Complementary PWM Mode (TRD1)]

Address: F0276H (TRD0), F0286H (TRD1) After Reset: 0000H Note R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRDi																

(Omitted)

Correct:

Figure 8 - 34 Format of Timer RD counter 1 (TRD1)
[Complementary PWM Mode (TRD1)]

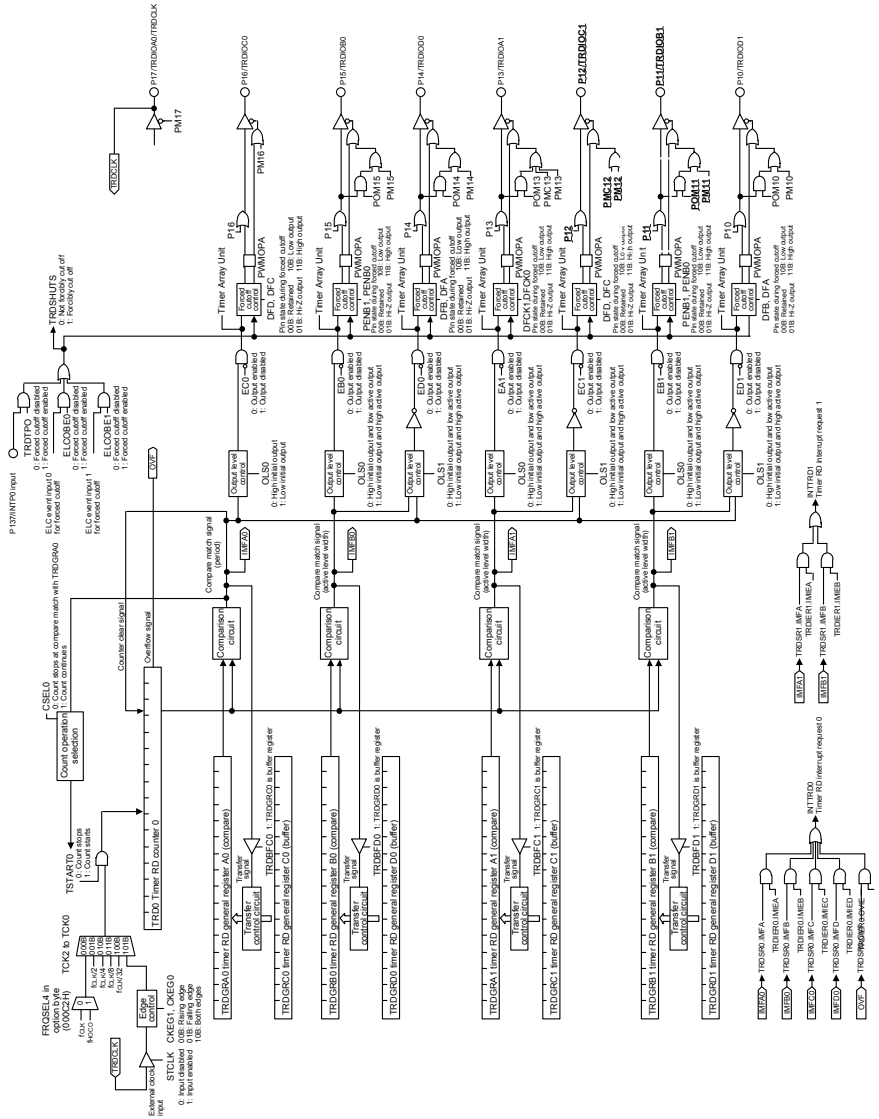
Address: F0286H (TRD1) After Reset: 0000H Note R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRD1																

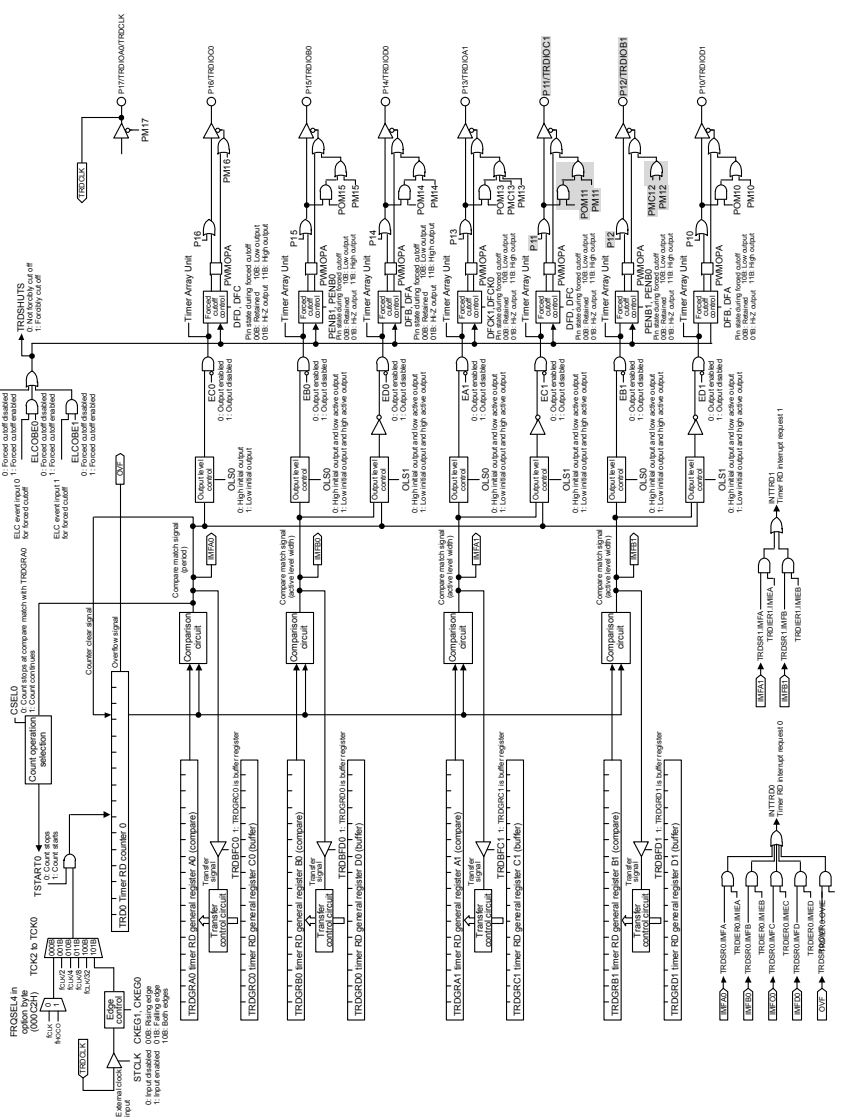
(Omitted)

22. 8.5.4 Reset Synchronous PWM Mode
Figure 8 - 56 Block Diagram of Reset Synchronous PWM Mode (For Timer RD0) (Page 401)

Incorrect:

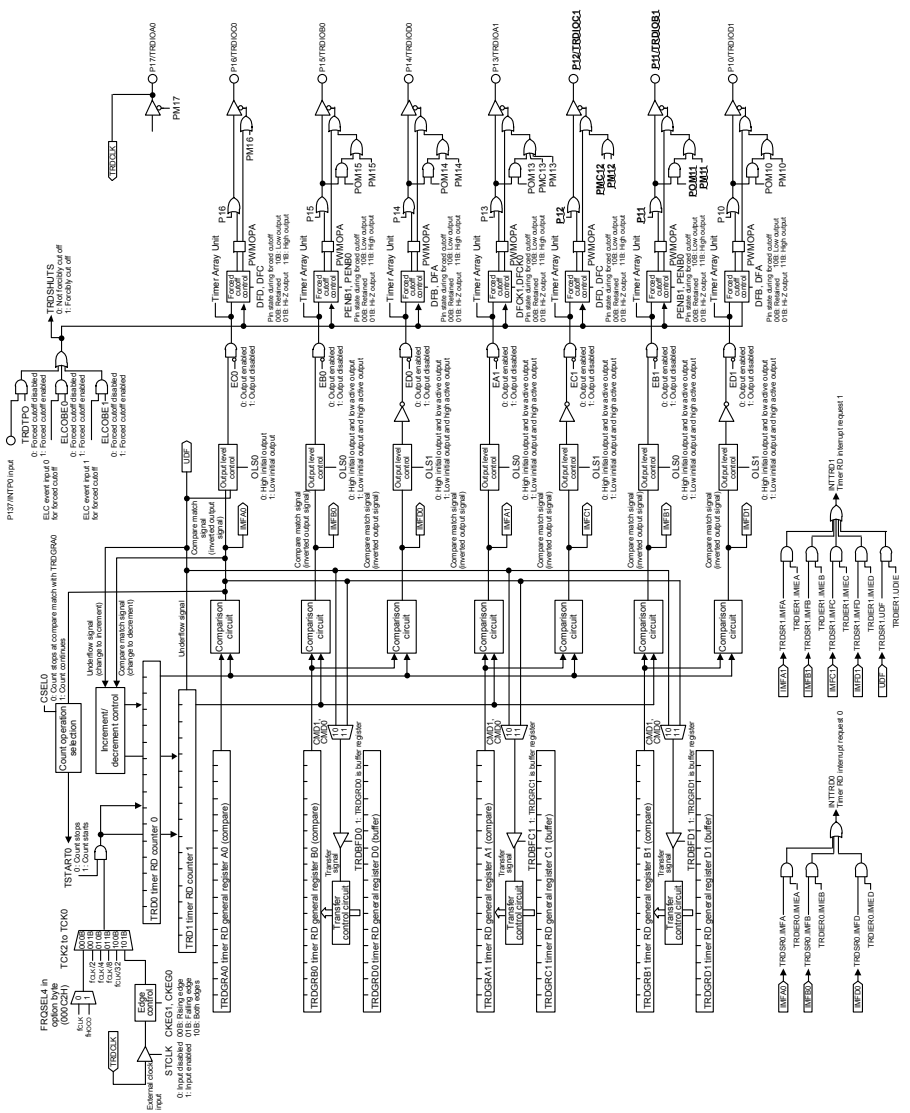


Correct:

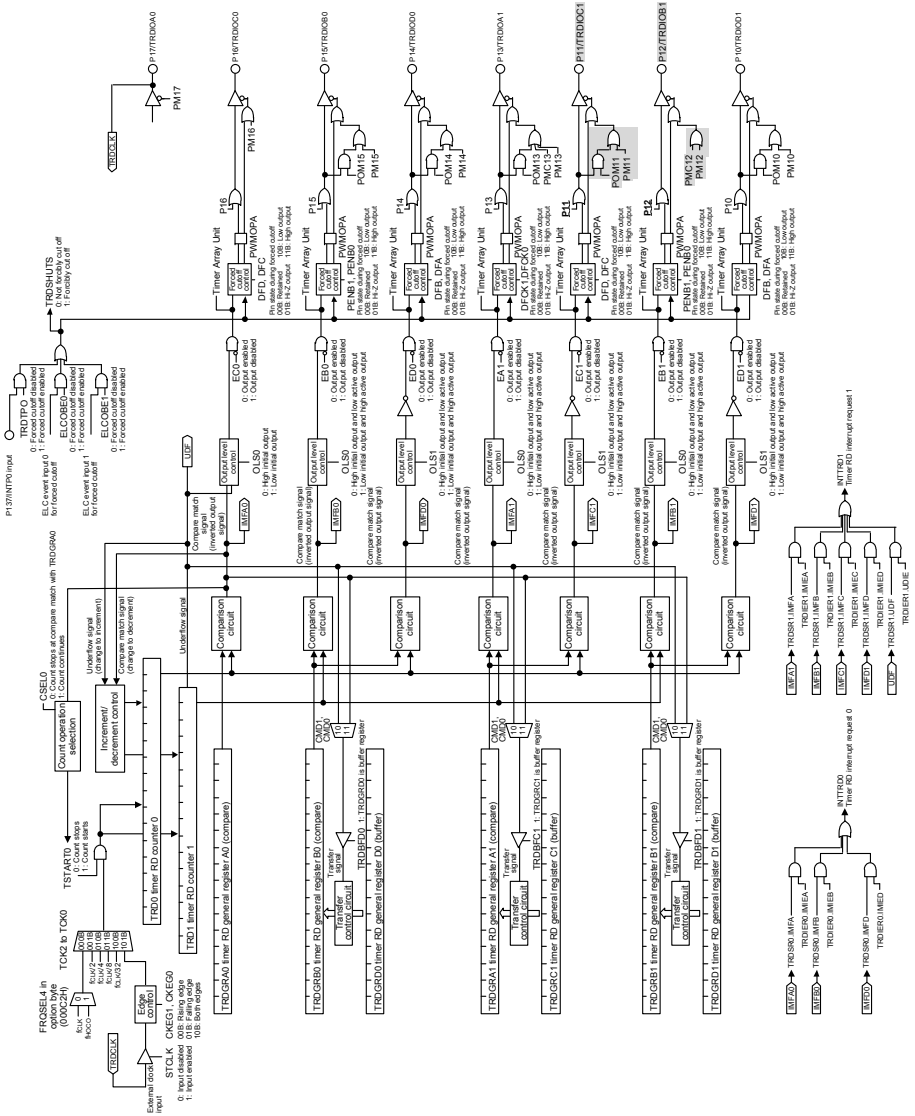


23. 8.5.5 Complementary PWM Mode
Figure 8 - 58 Block Diagram of Complementary PWM Mode (For Timer RD0) (Page 405)

Incorrect:

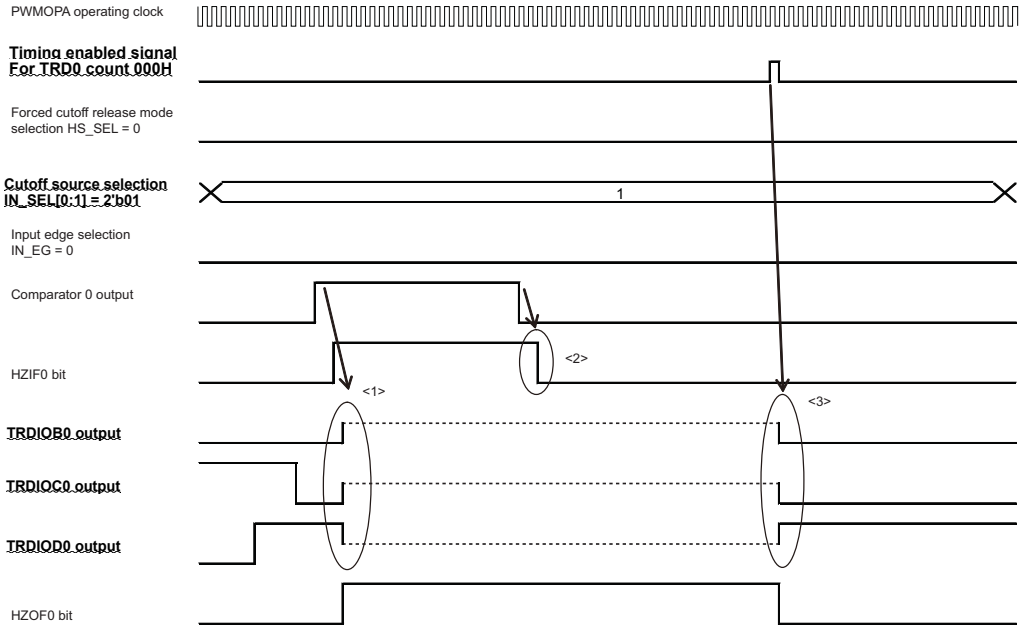


Correct:



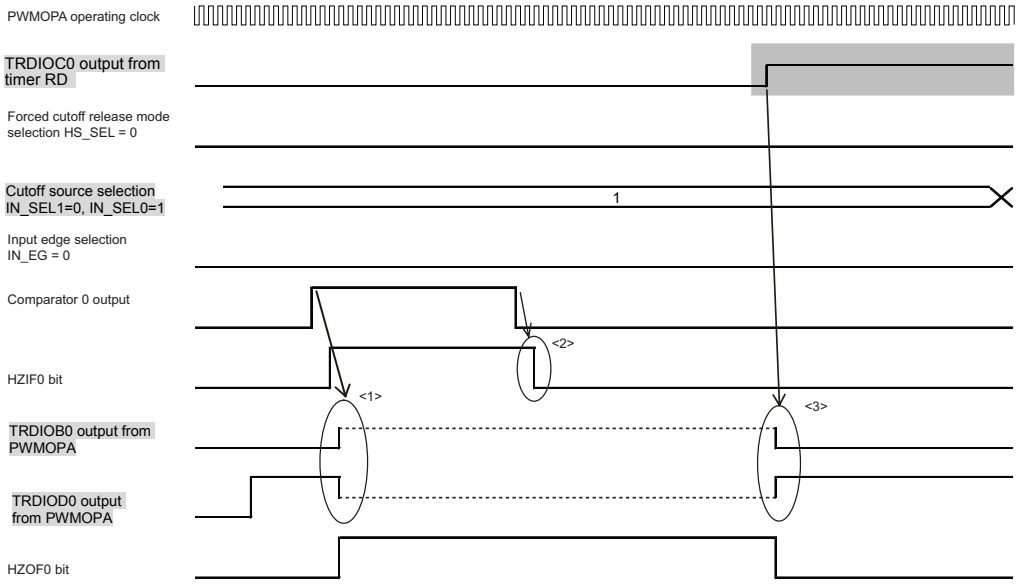
24. 8.8.3.2 Hardware release (HS_SEL = 0)
Figure 8 - 78 Operation example of hardware cutoff release function (an example of TRDIOB0 and TRDIOD0) (Page 435)

Incorrect:



(Omitted)

Correct:



(Omitted)

25. 8.8.3.3 Software cutoff release (HS_SEL = 1) (Page 440)

Incorrect:

8.8.3.3 Software cutoff release (HS_SEL = 1)

The timing of output forced cutoff release varies depending on the setting of the ACT bit of the OPCTL0 register.

(1) Immediate release via software (ACT = 0)
If ACT is set to 0, forced cutoff is released immediately when the HZ_REL bit of the OPCTL0 register is set to 1.
After forced cutoff, the HZ_REL bit automatically becomes 0.

(Omitted)

Correct:

8.8.3.3 Software cutoff release (HS_SEL = 1)

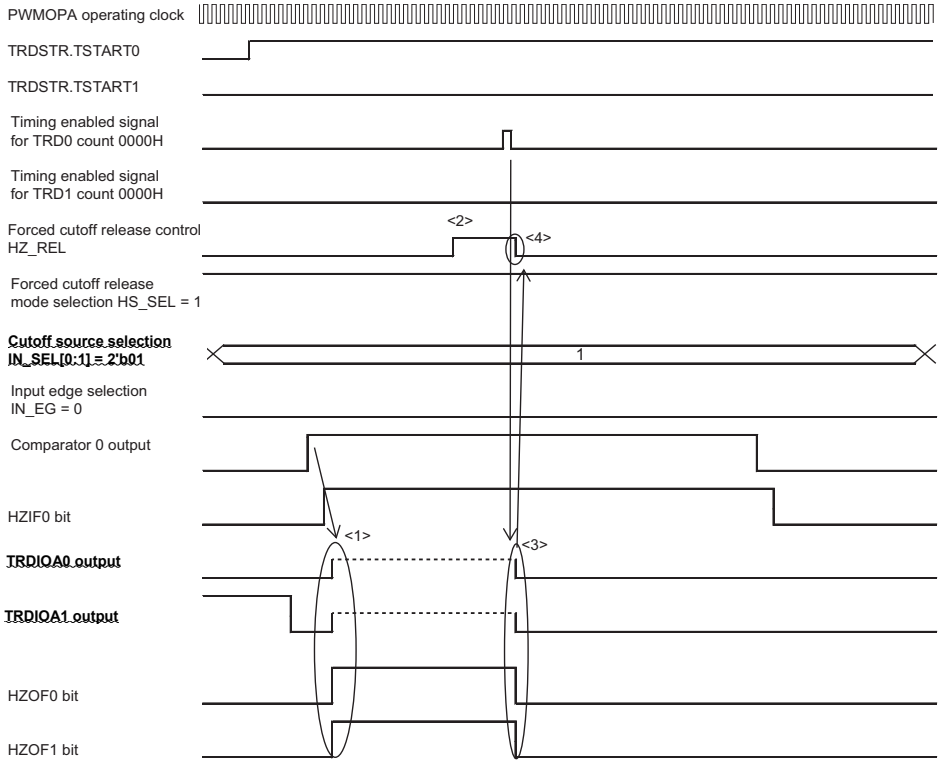
The timing of output forced cutoff release varies depending on the setting of the ACT bit of the OPCTL0 register.

(1) Immediate release via software (ACT = 0)
If ACT is set to 0, forced cutoff is released immediately when the HZ_REL bit of the OPCTL0 register is set to 1.
After forced cutoff is released, the HZ_REL bit automatically becomes 0.

(Omitted)

26. 8.8.3.3 Software cutoff release (HS_SEL = 1)
Figure 8 - 87 Operation example of output cutoff release by software (Page 444)

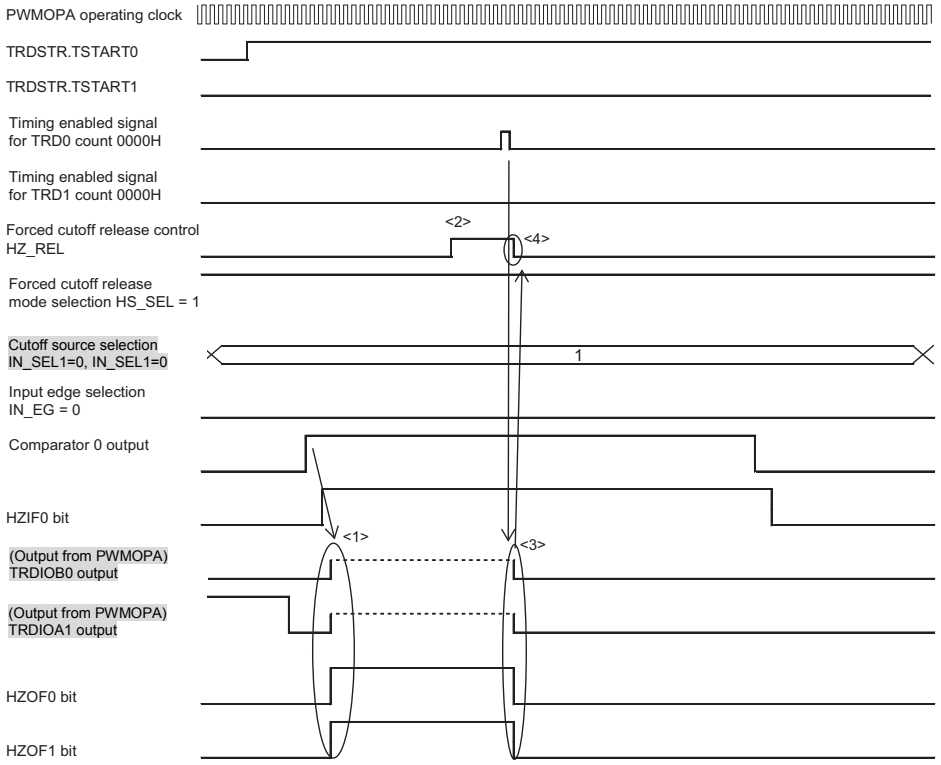
Incorrect:



<1> The **TRDIOA0** and TRDIOA1 pin outputs enter the cutoff state when the rising edge of the comparator 0 output signal is detected.
<2> After the HZ_REL bit is set to 1, it waits until the counter value of channel 0 of timer RD becomes 0000H.
<3> The **TRDIOA0** and TRDIOA1 forced cutoff states are released when the TRD0 count value becomes 0000H (Timer RD channel 1 operation is not affected).

(Omitted)

Correct:



<1> The TRDIOB0 and TRDIOA1 pin outputs enter the cutoff state when the rising edge of the comparator 0 output signal is detected.
<2> After the HZ_REL bit is set to 1, it waits until the counter value of channel 0 of timer RD becomes 0000H.
<3> The TRDIOB0 and TRDIOA1 forced cutoff states are released when the TRD0 count value becomes 0000H (Timer RD channel 1 operation is not affected).

(Omitted)

27. 17.1 Functions of Comparator
Table 17 - 1 CMP Function Overview (Page 621)

Incorrect:

Item	Description
CMP	• 2 channels available (Comparator 0 and Comparator 1) • The reference voltage can be selected in the negative side: Analog pin input, Comparator 0 internal reference voltage, or **internal reference voltage (BG2AD)** can be selected for the negative side of Comparator 0. •Analog pin inputs (4), Comparator 1 internal reference voltage, **internal reference voltage (BG2AD)** can be selected for the negative side of Comparator 1. : (Omitted) :

Correct:

Item	Description
CMP	• 2 channels available (Comparator 0 and Comparator 1) • The reference voltage can be selected in the negative side: Analog pin input, Comparator 0 internal reference voltage, or internal reference voltage (1.45V) can be selected for the negative side of Comparator 0. •Analog pin inputs (4), Comparator 1 internal reference voltage, internal reference voltage (1.45V) can be selected for the negative side of Comparator 1. : (Omitted) :