Date: Dec. 3, 2014

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A040A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G13 Descriptions in the Hardware User's Manual Rev. 3.20 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G13 R5F100xxx, R5F101xxx	Lot No. All lots	Reference Document	RL78/G13 User's Manual: Hardware Rev.3.20 R01UH0146EJ0320 (July. 2014)		

This document describes misstatements found in the RL78/G13 User's Manual: Hardware Rev.3.20 (R01UH0146EJ0320).

Corrections

Applicable Item	Applicable Page	Contents
Position of Index mark of 25-pin product.	Page 19 and 1053	Incorrect descriptions revised
6.3.3 Timer mode register mn Figure 6-11 the count clock selection of channel 7	Pages 288	Incorrect descriptions revised
12.3.12 Serial output register Figure 12-16 note.2 Reset value of serial output register m (SOm)	Page 511	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
		Document No.	English	R01UH0146EJ0320
1	Position of Index mark of 25-pin product.		Page 19 and 1053	Pages 3 and 4
2	6.3.3 Timer Mode Register mn Figure 6-11 the count clock selection of channel 7		Pages 288	Page 5
3	12.3.12 Serial output register m Figure 12-16 note.2 Reset value of serial output register m (SOm)		Page 511	Page 6

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

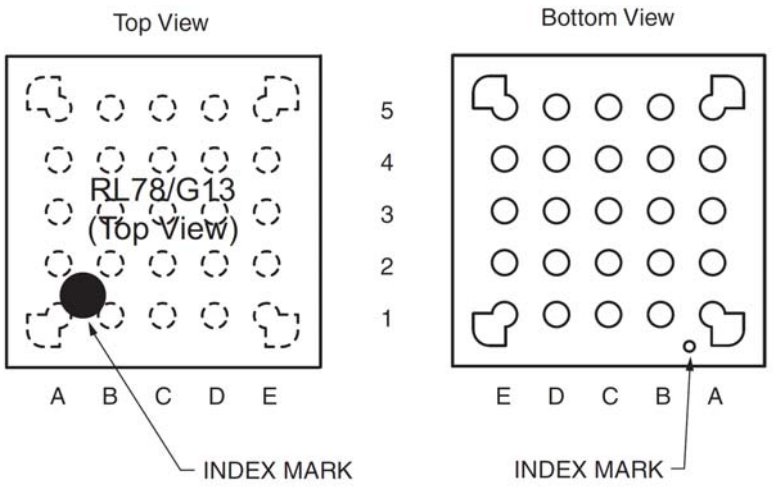
RL78/G13 User's Manual: Hardware Rev.3.20 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A040A/E	Dec. 3, 2014	First edition issued No.1 to 3 in corrections (This notice)

1. Position of Index mark of 25-pin product. (Page 19 and 1053)

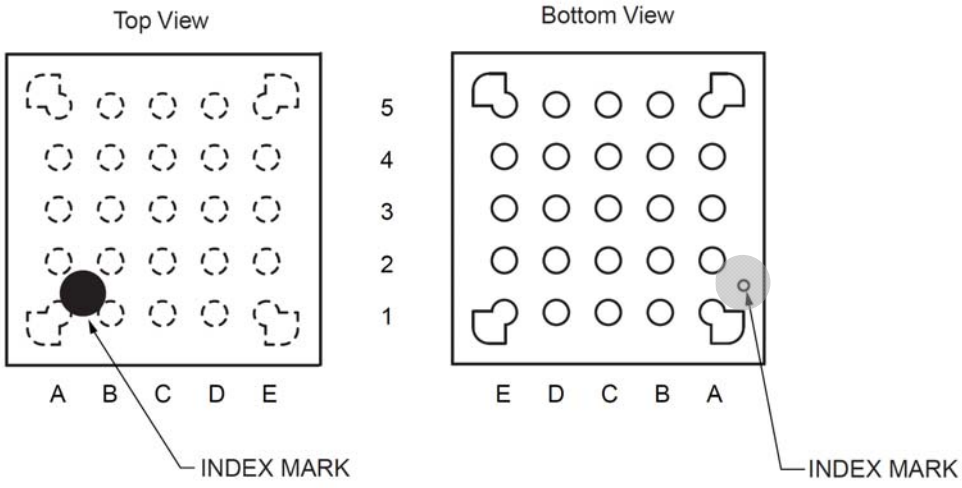
Correction for incorrect position of index mark of 25-pin product in bottom side. (p.19)

Incorrect:



(omitted)

Correct:

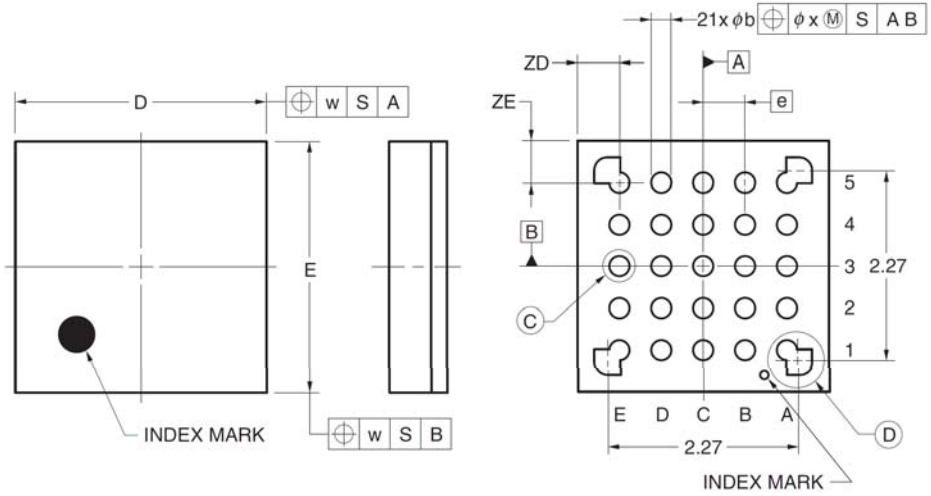


(omitted)

Correction for incorrect position of index mark of 25-pin product in bottom side. (p.1053)

Incorrect:

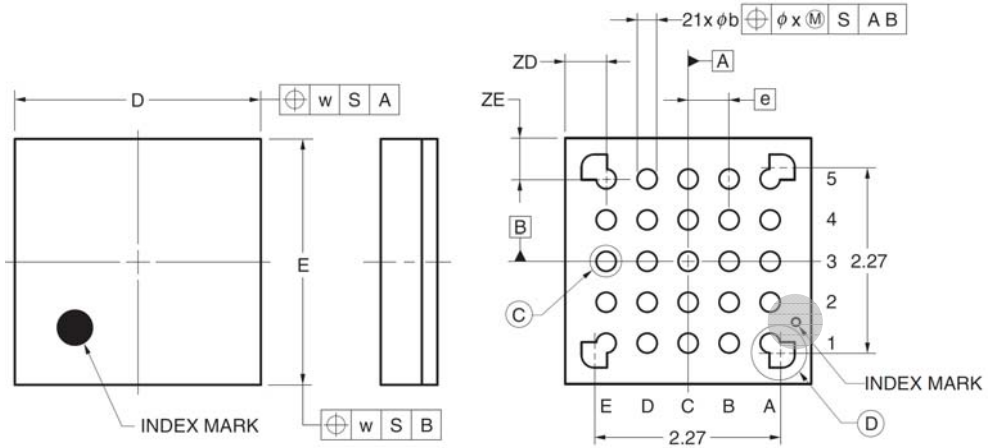
(omitted)



(omitted)

Correct:

(omitted)



(omitted)

2. 6.3.3 Timer Mode Register mn
Figure 6-11 the count clock selection of channel 7 (Page 288)

Incorrect:

Figure 6-11. Format of Timer Mode Register mn (TMRmn) (1/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W
F01D0H, F01D1H (TMR10) to F01DEH, F01DFH (TMR17)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n=2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MAS TERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

(omitted)

CCS mn	Selection of count clock (f_{TCLK}) of channel n
0	Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
1	Valid edge of input signal input from the TImn pin In channel 5, Valid edge of input signal selected by TIS0
Count clock (f_{TCLK}) is used for the counter, output controller, and interrupt controller.	

(omitted)

Correct:

Figure 6-11. Format of Timer Mode Register mn (TMRmn) (1/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W
F01D0H, F01D1H (TMR10) to F01DEH, F01DFH (TMR17)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n=2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MAS TERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

(omitted)

CCS mn	Selection of count clock (f_{TCLK}) of channel n
0	Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
1	Valid edge of input signal input from the TImn pin When using unit 0: In channel 5, Valid edge of input signal selected by TIS0 In channel7, Valid edge of input signal selected by ISC
Count clock (f_{TCLK}) is used for the counter, output controller, and interrupt controller.	

(omitted)

3. 12.3.12 Serial output register m Figure 12-16 note.2 Reset value of serial output register m (SOm) (Page 511)

Incorrect:

Figure 12-16. Format of Serial Output Register m (SOm)

Address: F0128H, F0129H (SO0) After reset: 0F0FH R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	CKO 03	CKO 02	CKO 01	CKO 00	0	0	0	0	SO 03	SO 02	SO 01	SO 00

Address: F0168H, F0169H (SO1) Note 1 After reset: 0F0FH Note 2 R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO1	0	0	0	0	CKO 13	CKO 12	CKO 11	CKO 10	0	0	0	0	SO 13	SO 12	SO 11	SO 10

Notes 1. 30 to 128-pin products only
2. The register value becomes **3030H** after a reset for the 30 to 64-pin products.

(omitted)

Correct:

Figure 12-16. Format of Serial Output Register m (SOm)

Address: F0128H, F0129H (SO0) After reset: 0F0FH R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO0	0	0	0	0	CKO 03	CKO 02	CKO 01	CKO 00	0	0	0	0	SO 03	SO 02	SO 01	SO 00

Address: F0168H, F0169H (SO1) Note 1 After reset: 0F0FH Note 2 R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SO1	0	0	0	0	CKO 13	CKO 12	CKO 11	CKO 10	0	0	0	0	SO 13	SO 12	SO 11	SO 10

Notes 1. 30 to 128-pin products only
2. The register value becomes 0303H after a reset for the 30 to 64-pin products.

(omitted)