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RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A0101A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G11 Descriptions in the User's Manual: Hardware Rev. 2.40 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G11 Group	Lot No. All lots	Reference Document	RL78/G11 User's Manual: Hardware Rev. 2.40 R01UH0637EJ0240 (Oct.2020)		

Precaution described below is added to the following products in the RL78/G11 User's Manual: Hardware Rev. 2.40 (R01UH0637EJ0240).

Precaution regarding the use of 16-bit timer KB0

When comparator 0 and 1 output is used as a trigger source of the timer KB0 timer restart function or forced output stop function 1 & 2, It require to be set the CiOE bit of the comparator output control register (COMPOCR) to 1. (i = 0, 1).

When the comparator i is used as the trigger signal of timer KB0, other output function that shared with the VCOUTi output pin cannot be used, but the input function can be used.

Corrections

Applicable Item	Applicable Page	Contents
10.3.4 16-bit timer KB operation control register n0 (TKBCTLn0)	Page 318	Caution added and Incorrect descriptions revised
10.3.17 Peripheral function switch register 0 (PFSEL0)	Page 330	Caution added
10.6.3.1 Forced output stop function control registers n0, n1 (TKBPACTLn0, TKBPACTLn1)	Page 384, Page 385	Caution added and Incorrect descriptions revised
Figure 19 - 1 Comparator Block Diagram	Page 766	Description added and Incorrect descriptions revised
19.3.5 Comparator output control register (COMPOCR)	Page 772	Caution added
19.5 Caution for Using Timer KB Simultaneous Operation Function	Page 780, Page 781	Description added and Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

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Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0637EJ0240	
1	10.3.4 16-bit timer KB operation control register n0 (TKBCTLn0)		Page 318	Page 3
2	10.3.17 Peripheral function switch register 0 (PFSEL0)		Page 330	Page 4
3	10.6.3.1 Forced output stop function control registers n0, n1 (TKBPACTLn0, TKBPACTLn1)		Page 384, Page385	Page 6
4	Figure 19 - 1 Comparator Block Diagram		Page 766	Page 8
5	19.3.5 Comparator output control register (COMPOCR)		Page 772	Page 9
6	19.5 Caution for Using Timer KB Simultaneous Operation Function		Page 780, Page 781	Page 11

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G11 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0101A/E	Jul. 11, 2022	First edition issued Corrections No.1 to No.6 revised (this document)

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1. **10.3.4 16-bit timer KB Operation Control Register n0 (TKBCTLn0) (Page 318)**

Incorrect:

· Figure 10 - 7 Format of 16-bit Timer KB Operation Control Register n0 (TKBCTLn0) (2/2)

TKBSTSn1	TKBSTSn0	Selection of timer KBn count start trigger
0	0	Does not use trigger input.
0	1	External interrupt signal (INTP10)
1	0	External interrupt signal (INTP11)
1	1	**Comparator detection signal specified by CTRGSEL1 and CTRGSEL0 bits of the PFSEL0 resister**

Caution 1. During timer operation, setting the other bits of the TKBCTLn0 register is prohibited. However, the TKBCTLn0 register can be refreshed (the same value is written).
Caution 2. Be sure to clear bits 15, 14, 11, 10, 6, and 3 to “0”.
Caution 3. For setting of INTP10/INTP11, see CHAPTER 19 COMPARATOR.

Remark n = 0, p = 0, 1

Correct:

· Figure 10 - 7 Format of 16-bit Timer KB Operation Control Register n0 (TKBCTLn0) (2/2)

TKBSTSn1	TKBSTSn0	Selection of timer KBn count start trigger
0	0	Does not use trigger input.
0	1	External interrupt signal (INTP10)
1	0	External interrupt signal (INTP11)
1	1	Comparator detection signal specified by CTRGSEL1 and CTRGSEL0 bits of the PFSEL0 resister Note

Note When comparator detection signal is used as a count start trigger, set the CiOE bit of the comparator output control register (COMPOCR) to 1. For detail, see 19.5 Caution for Using Timer KB Simultaneous Operation Function.

Caution 1. During timer operation, setting the other bits of the TKBCTLn0 register is prohibited. However, theTKBCTLn0 register can be refreshed (the same value is written).
Caution 2. Be sure to clear bits 15, 14, 11, 10, 6, and 3 to “0”.
Caution 3. For setting of INTP10/INTP11, see CHAPTER 19 COMPARATOR.

Remark i = 0, 1, n = 0, p = 0, 1

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2. 10.3.17 Peripheral function switch register 0 (PFSEL0) (Page 330)

Incorrect:

Figure 10 - 20 Format of Peripheral Function Switch Register 0 (PFSEL0)

Address: F0440H After reset: 00H R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
PFSEL0	CTRGSEL1	CTRGSEL0	INTPINV1	INTPINV0	PNFEN1	PNFEN0	TMRSTEN1	TMRSTEN0

CTRGSEL1	CTRGSEL0	Timer KB counter start trigger source
0	0	Use comparator 0 detection
0	1	Use comparator 1 detection
1	0	Use both of comparator 0 and comparator 1 detections
1	1	Setting prohibited (output signal is fixed to low level)

INTPINV1	Invert setting of INTP11 signal
0	Do not invert INTP11 signal
1	Invert INTP11 signal

INTPINV0	Invert setting of INTP10 signal
0	Do not invert INTP10 signal
1	Invert INTP10 signal

PNFEN1	Noise filter setting of external interrupt INTP11
0	Noise filter enable
1	Noise filter disable

PNFEN0	Noise filter setting of external interrupt INTP10
0	Noise filter enable
1	Noise filter disable

TMRSTEN1	Switch of external interrupt INTP11Note
0	External interrupt function is selected (stop mode release enabled, timer restart disabled)
1	Timer restart function is selected (stop mode release disabled, timer restart enabled).

TMRSTEN0	Switch of external interrupt INTP10Note
0	External interrupt function is selected (stop mode release enabled, timer restart disabled)
1	Timer restart function/forced output stop function 2 is selected (stop mode release disabled, timer restart enabled).

Correct:

Figure 10 - 20 Format of Peripheral Function Switch Register 0 (PFSEL0)

Address: F0440H After reset: 00H R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
PFSEL0	CTRGSEL1	CTRGSEL0	INTPINV1	INTPINV0	PNFEN1	PNFEN0	TMRSTEN1	TMRSTEN0

CTRGSEL1	CTRGSEL0	Timer KB counter start trigger source Note1
0	0	Use comparator 0 detection
0	1	Use comparator 1 detection
1	0	Use both of comparator 0 and comparator 1 detections
1	1	Setting prohibited (output signal is fixed to low level)

INTPINV1	Invert setting of INTP11 signal
0	Do not invert INTP11 signal
1	Invert INTP11 signal

INTPINV0	Invert setting of INTP10 signal
0	Do not invert INTP10 signal
1	Invert INTP10 signal

PNFEN1	Noise filter setting of external interrupt INTP11
0	Noise filter enable
1	Noise filter disable

PNFEN0	Noise filter setting of external interrupt INTP10
0	Noise filter enable
1	Noise filter disable

TMRSTEN1	Switch of external interruapt INTP11 Note2
0	External interrupt function is selected (stop mode release enabled, timer restart disabled)
1	Timer restart function is selected (stop mode release disabled, timer restart enabled).

TMRSTEN0	Switch of external interrupt INTP10 Note2
0	External interrupt function is selected (stop mode release enabled, timer restart disabled)
1	Timer restart function/forced output stop function 2 is selected (stop mode release disabled, timer restart enabled).

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Note When INTP10 or INTP11 is used as a trigger of the timer KB forced output stop function 2 or timer restart function, see 19.5 Caution for Using Timer KB Simultaneous Operation Function.

Remark See Figure 19 - 1 Comparator Block Diagram.

Note1. When comparator i detection signal is used as a counter start trigger source, set the CiOE bit of the comparator output control register (COMPOCR) to 1. For detail, see 19.5 Caution for Using Timer KB Simultaneous Operation Function.

Note 2. When INTP10 or INTP11 is used as a trigger of the timer KB forced output stop function 2 or timer restart function, see 19.5 Caution for Using Timer KB Simultaneous Operation Function.

Remark See Figure 19 - 1 Comparator Block Diagram.
i = 0, 1

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3. **10.6.3.1 Forced output stop function control registers n0, n1 (TKBPACTLn0, TKBPACTLn1) (Page 384, Page 385)**

Incorrect:

Figure 10 - 66 Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (1/2)

Address: F0430H (TKBPACTL00), F0432H (TKBPACTL01) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL0p	TKBPAFXS0p3	TKBPAFXS0p2	TKBPAFXS0p1	TKBPAFXS0p0	0	0	0	TKBPAFCM0p

7	6	5	4	3	2	1	0
0	0	TKBPAHZS0p1	TKBPAHZS0p0	TKBPAHCM0p1	TKBPAHCM0p0	TKBPAMD0p1	TKBPAMD0p0

TKBPAFXS0p3	External interruption trigger selection for forced output stop function 2
0	INTP11 can not be used as a trigger.
1	INTP11 can be used as a trigger.Note 1

TKBPAFXS0p2	External interruption trigger selection for forced output stop function 2
0	INTP10 can not be used as a trigger.
1	INTP10 can be used as a trigger.Note 1

TKBPAFXS0p1	Comparator trigger selection for forced output stop function 2
0	Comparator 1 can not be used as a trigger.
1	**Comparator 1 can be used as a trigger.**

TKBPAFXS0p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

TKBPAFCM0p	Operation mode selection for forced output stop function 2
0	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period.Note 2
1	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger.Note 2

TKBPAHZS0p1	Comparator trigger selection for forced output stop function 1
0	Comparator 1 can not be used as a trigger.
1	**Comparator 1 can be used as a trigger.**

TKBPAHZS0p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

Correct:

Figure 10 - 66 Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (1/2)

Address: F0430H (TKBPACTL00), F0432H (TKBPACTL01) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL0p	TKBPAFXS0p3	TKBPAFXS0p2	TKBPAFXS0p1	TKBPAFXS0p0	0	0	0	TKBPAFCM0p

7	6	5	4	3	2	1	0
0	0	TKBPAHZS0p1	TKBPAHZS0p0	TKBPAHCM0p1	TKBPAHCM0p0	TKBPAMD0p1	TKBPAMD0p0

TKBPAFXS0p3	External interruption trigger selection for forced output stop function 2
0	INTP11 can not be used as a trigger.
1	INTP11 can be used as a trigger.Note 1

TKBPAFXS0p2	External interruption trigger selection for forced output stop function 2
0	INTP10 can not be used as a trigger.
1	INTP10 can be used as a trigger.Note 1

TKBPAFXS0p1	Comparator trigger selection for forced output stop function 2
0	Comparator 1 can not be used as a trigger.
1	Comparator 1 can be used as a trigger.Note 3

TKBPAFXS0p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger.Note 3

TKBPAFCM0p	Operation mode selection for forced output stop function 2
0	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period.Note 2
1	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger.Note 2

TKBPAHZS0p1	Comparator trigger selection for forced output stop function 1
0	Comparator 1 can not be used as a trigger.
1	Comparator 1 can be used as a trigger.Note 3

TKBPAHZS0p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger.Note 3

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Figure 10 - 66 Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (2/2)

TKBPAHCM0p1TKBPAHCM0p0Clear condition

TKBPAHCM0p1	TKBPAHCM0p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT0p) = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT0p) = 1" is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT0p) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT0p) = 1 is written, regardless of the trigger signal level. Note 2
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT0p) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT0p) = 1 is written when the trigger signal is in its inactive period. Note 2

TKBPAMD0p1	TKBPAMD0p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Note 1. When INTP10 and INTP11 is used as the forced output stop function 2, see 14.5 Caution for Using Timer KB Simultaneous Operation Function.

Note 2. When timer KB is stopped (TKBCEn = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCEn = 1).

Caution 1. During timer operation, setting the other bits of the TKBPACTL0p register is prohibited. However, the TKBPACTL0p register can be refreshed (the same value is written).

Caution 2. Be sure to clear bits 11 to 9, 7 and 6to "0".

Remark n = 0, p = 0, 1

Figure 10 - 66 Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (2/2)

TKBPAHCM0p1TKBPAHCM0p0Clear condition

TKBPAHCM0p1	TKBPAHCM0p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT0p) = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT0p) = 1" is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT0p) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT0p) = 1 is written, regardless of the trigger signal level. Note 2
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT0p) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT0p) = 1 is written when the trigger signal is in its inactive period. Note 2

TKBPAMD0p1	TKBPAMD0p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Note 1. When INTP10 and INTP11 is used as the forced output stop function 2, see 14.5 Caution for Using Timer KB Simultaneous Operation Function.

Note 2. When timer KB is stopped (TKBCEn = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCEn = 1).

Note 3. When comparator i is used as the forced output stop function 1 and 2, set the CiOE bit of the comparator output control register (COMPOCR) to 1.

Caution 1. During timer operation, setting the other bits of the TKBPACTL0p register is prohibited. However, the TKBPACTL0p register can be refreshed (the same value is written).

Caution 2. Be sure to clear bits 11 to 9, 7 and 6to "0".

Remark i = 0, 1, n = 0, p = 0, 1

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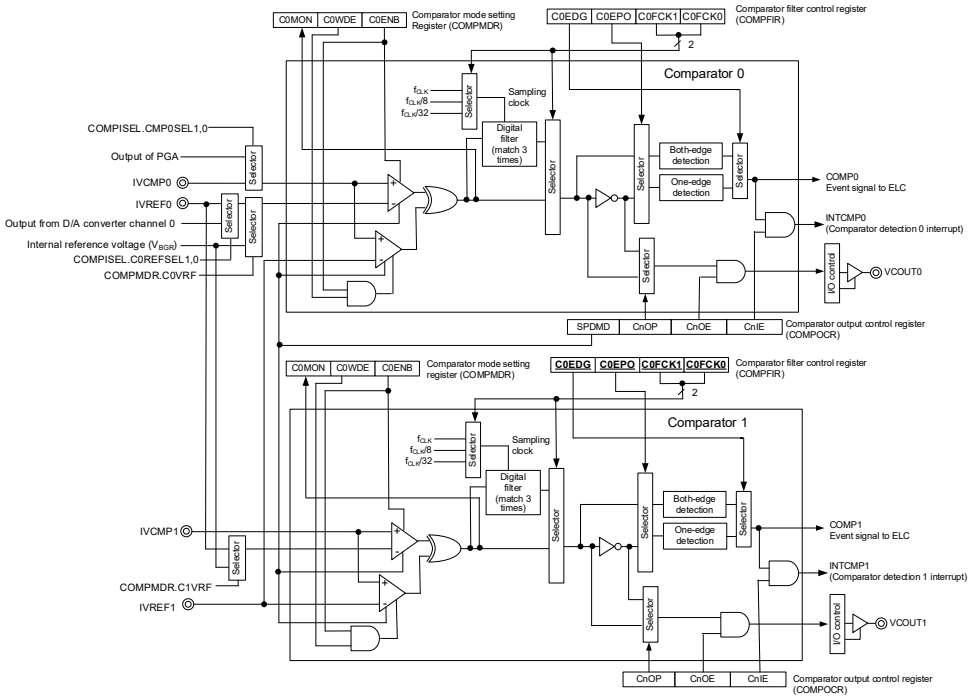
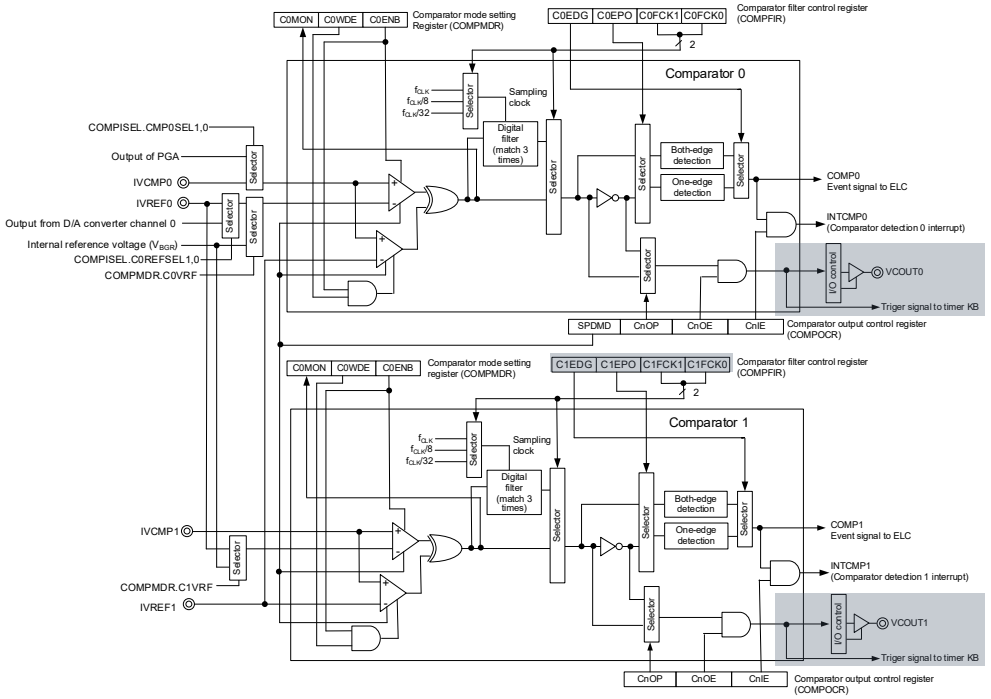
4. Figure 19 - 1 Comparator Block Diagram (Page 766)

Incorrect:
Figure 19 - 1 Comparator Block Diagram



Correct:
Figure 19 - 1 Comparator Block Diagram



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5. 19.3.5 Comparator output control register (COMPOCR) (Page 772)

Incorrect:

Figure 19 - 6 Format of Comparator output control register (COMPOCR)

Address: F0342H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
COMPOCR	SPDMD	C1OP	C1OE	C1IE	0	C0OP	C0OE	C0IE

SPDMD	Comparator speed selection Note 1
0	Comparator low-speed mode
1	Comparator high-speed mode

C1OP	VCOUT1 output polarity selection
0	Comparator 1 output is output to VCOUT1
1	Inverted comparator 1 output is output to VCOUT1

C1OE	VCOUT1 pin output enable
0	Comparator 1 VCOUT1 pin output disabled
1	**Comparator 1 VCOUT1 pin output enabled**

C1IE	Comparator 1 interrupt request enable Note 2
0	Comparator 1 interrupt request disabled
1	Comparator 1 interrupt request enabled

C0OP	VCOUT0 output polarity selection
0	Comparator 0 output is output to VCOUT0
1	Inverted comparator 0 output is output to VCOUT0

C0OE	VCOUT0 pin output enable
0	Comparator 0 VCOUT0 pin output disabled
1	**Comparator 0 VCOUT0 pin output enabled**

C0IE	Comparator 0 interrupt request enable Note 3
0	Comparator 0 interrupt request disabled
1	Comparator 0 interrupt request enabled

Correct:

Figure 19 - 6 Format of Comparator output control register (COMPOCR)

Address: F0342H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
COMPOCR	SPDMD	C1OP	C1OE	C1IE	0	C0OP	C0OE	C0IE

SPDMD	Comparator speed selection Note 1
0	Comparator low-speed mode
1	Comparator high-speed mode

C1OP	VCOUT1 output polarity selection
0	Comparator 1 output is output to VCOUT1
1	Inverted comparator 1 output is output to VCOUT1

C1OE	VCOUT1 pin output enable
0	Comparator 1 VCOUT1 pin output disabled
1	Comparator 1 VCOUT1 pin output enabled Note 4

C1IE	Comparator 1 interrupt request enable Note 2
0	Comparator 1 interrupt request disabled
1	Comparator 1 interrupt request enabled

C0OP	VCOUT0 output polarity selection
0	Comparator 0 output is output to VCOUT0
1	Inverted comparator 0 output is output to VCOUT0

C0OE	VCOUT0 pin output enable
0	Comparator 0 VCOUT0 pin output disabled
1	Comparator 0 VCOUT0 pin output enabled Note 4

C0IE	Comparator 0 interrupt request enable Note 3
0	Comparator 0 interrupt request disabled
1	Comparator 0 interrupt request enabled

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Note 1. **When rewriting the SPDMD bit, be sure to set the CiENB bit (i = 0 or 1) in the COMPMDR register to 0 in advance.**

Note 2. If C1IE is changed from 0 (interrupt request disabled) to 1 (interrupt request enabled), since bit 1 (CMPIF1) in interrupt request flag register 2L (IF2L) may set to 1 (interrupt requested), clear bit 1 (CMPIF1) in interrupt request flag register 2L (IF2L) to 0 before using an interrupt.

Note 3. If C0IE is changed from 0 (interrupt request disabled) to 1 (interrupt request enabled), since bit 0 (CMPIF0) in interrupt request flag register 2L (IF2L) may set to 1 (interrupt requested), clear bit 0 (CMPIF0) in interrupt request flag register 2L (IF2L) to 0 before using an interrupt.

Note 1. When rewriting the SPDMD bit, be sure to set the CiENB bit in the COMPMDR register to 0 in advance.

Note 2. If C1IE is changed from 0 (interrupt request disabled) to 1 (interrupt request enabled), since bit 1 (CMPIF1) in interrupt request flag register 2L (IF2L) may set to 1 (interrupt requested), clear bit 1 (CMPIF1) in interrupt request flag register 2L (IF2L) to 0 before using an interrupt.

Note 3. If C0IE is changed from 0 (interrupt request disabled) to 1 (interrupt request enabled), since bit 0 (CMPIF0) in interrupt request flag register 2L (IF2L) may set to 1 (interrupt requested), clear bit 0 (CMPIF0) in interrupt request flag register 2L (IF2L) to 0 before using an interrupt.

Note 4. When comparator i output is used as a trigger for functions that operate simultaneously with the timer KB, such as the forced output stop function and the timer restart function, set the CiOE bit to.1.

Remark i = 0, 1

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6. 19.5 Caution for Using Timer KB Simultaneous Operation Function (Page 780, Page 781)

Incorrect:

19.5 Caution for Using Timer KB Simultaneous Operation Function

In addition to their use as an external interrupt input, the INTP10, 11 pin output and the comparator output signal can be used as a trigger for functions that operate simultaneously with timer KB, such as the forced output stop function and timer restart function. **The settings in peripheral function switch register 0 (PFSEL0) and the edge selection registers must be specified according to the function used.** The width of the active signal required until each function starts operating differs.

Table 19 - 4 Relationship of Comparator 0 and 1 Functions, Register Settings, and Active Signal Width

Function	Peripheral Enable Resister Setting	Edge Setting Resister	Necessary Active Signal Width to Operate Each Function		
			Interrupt	Forced Output Stop	Timer Restart
External interrupt (STOP release is enabled) Note 1	-	CnEDG,CnEPO (n = 0,1)	Up to 1.2 ns Note 1		
Forced output stop	-	Note 4	Up to 1.2 ns Note 1	Up to 1.2 ns Note 1,5	
Timer Restart Note 6	-	CnEDG,CnEPO (n = 0,1)	Up to 1.2 ns Note 1		Up to 1.2 ns Note 1 + 2 to 3 clocks Note 3, 4

Correct:

19.5 Caution for Using Timer KB Simultaneous Operation Function

In addition to their use as an external interrupt input, the INTP10, 11 pin output and the comparator output signal can be used as a trigger for functions that operate simultaneously with timer KB, such as the forced output stop function and timer restart function. The settings in peripheral function switch register 0 (PFSEL0), the edge selection resisters and comparator output control resister (COMPOCR) must be specified according to the function used. The width of the active signal required until each function starts operating differs.

Table 19 - 4 Relationship of Comparator 0 and 1 Functions, Register Settings, and Active Signal Width

Function	Peripheral Enable Resister Setting	Edge Setting Resister	Comparator Output Control Resister Setting	Necessary Active Signal Width to Operate Each Function		
				Interrupt	Forced Output Stop	Timer Restart
External interrupt (STOP release is enabled) Note 1	-	CnEDG,CnEPO	-	Up to 1.2 ns Note 1		
Forced output stop	-	Note 4	CnOE = 1 Note 6	Up to 1.2 ns Note 1	Up to 1.2 ns Note 1,5	
Timer Restart Note 6	-	CnEDG,CnEPO	CnOE = 1 Note 6	Up to 1.2 ns Note 1		Up to 1.2 ns Note 1 + 2 to 3 clocks Note 3, 4

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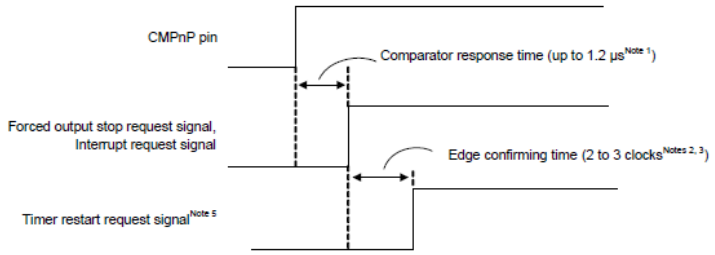
Figure 19 - 11 Generation Timing of Forced Output Stop Signal and Timer Restart Request Signal by INTP10, 11



Note 1. When noise filtering is set to “0, 0” by using the CnDFS1 and CnDFS0 bits in the comparator n control register (CnCTL).
If a setting other than “0, 0” is specified, the specified noise elimination width is added.

Note 2. For f_{CLK} or f_{HOCO}

Note 3. Until the timer restart function starts operating, an additional clock cycle is required after the timer restart request signal is received, and an additional output delay time (10 to 40 ns) is required until the level of the timer KB output changes.

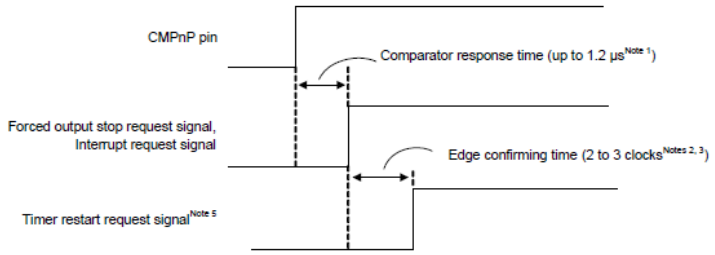
Note 4. The active level of the forced output stop function is high.

Note 5. An additional output delay time (10 to 40 ns) is required from when forced output stop function starts operating to when the level of the timer KB output changes.

Note 6. The timer restart function can be used for comparator 0 and 1 only.

Remark n = 0 and 1

Figure 19 - 11 Generation Timing of Forced Output Stop Signal and Timer Restart Request Signal by INTP10, 11



Note 1. When noise filtering is set to “0, 0” by using the CnDFS1 and CnDFS0 bits in the comparator n control register (CnCTL).
If a setting other than “0, 0” is specified, the specified noise elimination width is added.

Note 2. For f_{CLK} or f_{HOCO}

Note 3. Until the timer restart function starts operating, an additional clock cycle is required after the timer restart request signal is received, and an additional output delay time (10 to 40 ns) is required until the level of the timer KB output changes.

Note 4. The active level of the forced output stop function is high.

Note 5. An additional output delay time (10 to 40 ns) is required from when forced output stop function starts operating to when the level of the timer KB output changes.

Note 6. The trigger signal of the comparator to the timer KB0 is connected to internally. When the comparator n is used as the trigger signal of timer KB0, other output function that shared with the VCOUTn output pin cannot be used, but the input function can be used. When the input function that shared pin with VCOUTn is used, it requires setting the corresponding bit in the port mode register (PMxx) to 1.

Remark n = 0, 1

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