Precaution described below is added to the following products in the RL78/G11 User’s Manual: Hardware Rev. 2.40 (R01UH0637EJ0240).

Precaution regarding the use of 16-bit timer KB0

When comparator 0 and 1 output is used as a trigger source of the timer KB0 timer restart function or forced output stop function 1 & 2, It require to be set the CiOE bit of the comparator output control register (COMPOCR) to 1. (i = 0, 1).

When the comparator i is used as the trigger signal of timer KB0, other output function that shared with the VCOUIt output pin cannot be used, but the input function can be used.

Corrections

<table>
<thead>
<tr>
<th>Applicable Item</th>
<th>Applicable Page</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.3.4 16-bit timer KB operation control register n0 (TKBCTLn0)</td>
<td>Page 318</td>
<td>Caution added and Incorrect descriptions revised</td>
</tr>
<tr>
<td>10.3.17 Peripheral function switch register 0 (PFSELO)</td>
<td>Page 330</td>
<td>Caution added</td>
</tr>
<tr>
<td>10.6.3.1 Forced output stop function control registers n0, n1 (TKBPACTLn0, TKBPACTLn1)</td>
<td>Page 384, Page 385</td>
<td>Caution added and Incorrect descriptions revised</td>
</tr>
<tr>
<td>Figure 19 - 1 Comparator Block Diagram</td>
<td>Page 766</td>
<td>Description added and Incorrect descriptions revised</td>
</tr>
<tr>
<td>19.3.5 Comparator output control register (COMPOCR)</td>
<td>Page 772</td>
<td>Caution added</td>
</tr>
<tr>
<td>19.5 Caution for Using Timer KB Simultaneous Operation Function</td>
<td>Page 780, Page 781</td>
<td>Description added and Incorrect descriptions revised</td>
</tr>
</tbody>
</table>

Document Improvement

The above corrections will be made for the next revision of the User’s Manual: Hardware.
**Corrections in the User's Manual: Hardware**

<table>
<thead>
<tr>
<th>No.</th>
<th>Corrections and Applicable Items</th>
<th>Document No.</th>
<th>English</th>
<th>Pages in this document for corrections</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10.3.4 16-bit timer KB operation control register n0 (TKBCTLn0)</td>
<td>Page 318</td>
<td>Page 3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>10.3.17 Peripheral function switch register 0 (PFSEL0)</td>
<td>Page 330</td>
<td>Page 4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>10.6.3.1 Forced output stop function control registers n0, n1 (TKBPACTLn0, TKBPACTLn1)</td>
<td>Page 384, Page385</td>
<td>Page 6</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Figure 19 - 1 Comparator Block Diagram</td>
<td>Page 766</td>
<td>Page 8</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>19.3.5 Comparator output control register (COMPOCR)</td>
<td>Page 772</td>
<td>Page 9</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>19.5 Caution for Using Timer KB Simultaneous Operation Function</td>
<td>Page 780, Page 781</td>
<td>Page 11</td>
<td></td>
</tr>
</tbody>
</table>

Incorrect: **Bold with underline**; Correct: **Gray hatched**

**Revision History**

RL78/G11 Correction for incorrect description notice

<table>
<thead>
<tr>
<th>Document Number</th>
<th>Issue Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TN-RL*-A0101A/E</td>
<td>Jul. 11, 2022</td>
<td>First edition issued  Corrections No.1 to No.6 revised (this document)</td>
</tr>
</tbody>
</table>
1. **10.3.4 16-bit timer KB Operation Control Register n0 (TKBCTLn0)**  
(PAGE 318)

Incorrect:

- Figure 10 - 7 Format of 16-bit Timer KB Operation Control Register n0 (TKBCTLn0) (2/2)

<table>
<thead>
<tr>
<th>TKBSTSn1</th>
<th>TKBSTSn0</th>
<th>Selection of timer KBn count start trigger</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Does not use trigger input.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>External interrupt signal (INTP10)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>External interrupt signal (INTP11)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Comparator detection signal specified by CTRGSEL1 and CTRGSEL0 bits of the PFSEL0 register</td>
</tr>
</tbody>
</table>

Caution 1. During timer operation, setting the other bits of the TKBCTLn0 register is prohibited. However, the TKBCTLn0 register can be refreshed (the same value is written).

Caution 2. Be sure to clear bits 15, 14, 11, 10, 6, and 3 to “0”.

Caution 3. For setting of INTP10/INTP11, see CHAPTER 19 COMPARATOR.

Remark  \( n = 0, p = 0, 1 \)

Correct:

- Figure 10 - 7 Format of 16-bit Timer KB Operation Control Register n0 (TKBCTLn0) (2/2)

<table>
<thead>
<tr>
<th>TKBSTSn1</th>
<th>TKBSTSn0</th>
<th>Selection of timer KBn count start trigger</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Does not use trigger input.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>External interrupt signal (INTP10)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>External interrupt signal (INTP11)</td>
</tr>
</tbody>
</table>
| 1        | 1        | Comparator detection signal specified by CTRGSEL1 and CTRGSEL0 bits of the PFSEL0 register | Note

Note When comparator detection signal is used as a count start trigger, set the CiOE bit of the comparator output control register (COMPOCR) to 1. For detail, see \( 19.5 \) Caution for Using Timer KB Simultaneous Operation Function.

Caution 1. During timer operation, setting the other bits of the TKBCTLn0 register is prohibited. However, the TKBCTLn0 register can be refreshed (the same value is written).

Caution 2. Be sure to clear bits 15, 14, 11, 10, 6, and 3 to “0”.

Caution 3. For setting of INTP10/INTP11, see CHAPTER 19 COMPARATOR.

Remark  \( i = 0, 1, n = 0, p = 0, 1 \)
### 2. 10.3.17 Peripheral function switch register 0 (PFSEL0) (Page 330)

**Incorrect:**
Figure 10 - 20 Format of Peripheral Function Switch Register 0 (PFSEL0)

<table>
<thead>
<tr>
<th>PFSEL0</th>
<th>CTRGSEL1</th>
<th>CTRGOSEL0</th>
<th>INTPINV1</th>
<th>INTPINV0</th>
<th>PNFEN1</th>
<th>PNFEN0</th>
<th>TMRS1EN</th>
<th>TMRS0END</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CTROSEL1</td>
<td>CTROSEL0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td></td>
<td>Setting prohibited (output signal is fixed to low level)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INTPINV1</td>
<td>Invert setting of INTP11 signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Do not invert INTP11 signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Invert INTP11 signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INTPINV0</td>
<td>Invert setting of INTP10 signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Do not invert INTP10 signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Invert INTP10 signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PNFEN1</td>
<td>Noise filter setting of external interrupt INTP11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Noise filter enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Noise filter disable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PNFEN0</td>
<td>Noise filter setting of external interrupt INTP10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Noise filter enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Noise filter disable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMRS1EN</td>
<td>Switch of external interrupt INTP11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>External interrupt function is selected (stop mode release enabled, timer restart disabled)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Timer restart function is selected (stop mode release disabled, timer restart enabled)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Correct:**
Figure 10 - 20 Format of Peripheral Function Switch Register 0 (PFSEL0)

<table>
<thead>
<tr>
<th>PFSEL0</th>
<th>CTRGSEL1</th>
<th>CTRGOSEL0</th>
<th>INTPINV1</th>
<th>INTPINV0</th>
<th>PNFEN1</th>
<th>PNFEN0</th>
<th>TMRS1EN</th>
<th>TMRS0END</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CTROSEL1</td>
<td>CTROSEL0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td></td>
<td>Setting prohibited (output signal is fixed to low level)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INTPINV1</td>
<td>Invert setting of INTP11 signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Do not invert INTP11 signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Invert INTP11 signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INTPINV0</td>
<td>Invert setting of INTP10 signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Do not invert INTP10 signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Invert INTP10 signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PNFEN1</td>
<td>Noise filter setting of external interrupt INTP11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Noise filter enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Noise filter disable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PNFEN0</td>
<td>Noise filter setting of external interrupt INTP10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Noise filter enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Noise filter disable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMRS1EN</td>
<td>Switch of external interrupt INTP11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>External interrupt function is selected (stop mode release enabled, timer restart disabled)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Timer restart function is selected (stop mode release disabled, timer restart enabled)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMRS0END</td>
<td>Switch of external interrupt INTP10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>External interrupt function is selected (stop mode release enabled, timer restart disabled)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Timer restart function is selected (stop mode release disabled, timer restart enabled)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**Note**  When INTP10 or INTP11 is used as a trigger of the timer KB forced output stop function 2 or timer restart function, see 19.5 Caution for Using Timer KB Simultaneous Operation Function.

**Remark**  See Figure 19 - 1 Comparator Block Diagram.

---

**Note1.**  When comparator i detection signal is used as a counter start trigger source, set the CiOE bit of the comparator output control register (COMPOCR) to 1. For detail, see 19.5 Caution for Using Timer KB Simultaneous Operation Function.

**Note 2.**  When INTP10 or INTP11 is used as a trigger of the timer KB forced output stop function 2 or timer restart function, see 19.5 Caution for Using Timer KB Simultaneous Operation Function.

**Remark**  See Figure 19 - 1 Comparator Block Diagram.

\[ i = 0, 1 \]
3. 10.6.3.1 Forced output stop function control registers n0, n1 (TKBPACTLn0, TKBPACTLn1) (Page 384, Page 385)

Incorrect:
Figure 10 - 66 Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (1/2)

Correct:
Figure 10 - 66 Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (1/2)
Figure 10 - 66 Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (2/2)

Note 1. When INTP10 and INTP11 is used as the forced output stop function 2, see 14.5 Caution for Using Timer KB Simultaneous Operation Function.

Note 2. When timer KB is stopped (TKBCEn = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCEn = 1).

Caution 1. During timer operation, setting the other bits of the TKBPACTL0p register is prohibited. However, the TKBPACTL0p register can be refreshed (the same value is written).

Caution 2. Be sure to clear bits 11 to 9, 7 and 6 to "0".

Remark \( n = 0, p = 0, 1 \)

Note 1. When INTP10 and INTP11 is used as the forced output stop function 2, see 14.5 Caution for Using Timer KB Simultaneous Operation Function.

Note 2. When timer KB is stopped (TKBCEn = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCEn = 1).

Note 3. When comparator \( i \) is used as the forced output stop function 1 and 2, set the CiOE bit of the comparator output control register (COMPOCR) to 1.

Caution 1. During timer operation, setting the other bits of the TKBPACTL0p register is prohibited. However, the TKBPACTL0p register can be refreshed (the same value is written).

Caution 2. Be sure to clear bits 11 to 9, 7 and 6 to "0".

Remark \( i = 0, 1, n = 0, p = 0, 1 \)
4. Figure 19 - 1 Comparator Block Diagram (Page 766)

Incorrect:
Figure 19 - 1 Comparator Block Diagram

Correct:
Figure 19 - 1 Comparator Block Diagram
5. **Comparator output control register (COMPOCR)** (Page 772)

### Incorrect:

**Figure 19 - 6 Format of Comparator output control register (COMPOCR)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>(&lt;7&gt;)</th>
<th>(&lt;6&gt;)</th>
<th>(&lt;5&gt;)</th>
<th>(&lt;4&gt;)</th>
<th>(3)</th>
<th>(&lt;2&gt;)</th>
<th>(&lt;1&gt;)</th>
<th>(&lt;0&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMPOCR</td>
<td>SPDMD</td>
<td>C1OP</td>
<td>C1OE</td>
<td>C1IE</td>
<td>0</td>
<td>C0OP</td>
<td>C0OE</td>
<td>C0IE</td>
</tr>
<tr>
<td></td>
<td>Comparator speed selection Note 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator low-speed mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Comparator high-speed mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator 1 VCOUT1 output polarity selection</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator 1 output is output to VCOUT1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Inverted comparator 1 output is output to VCOUT1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator 1 VCOUT1 pin output enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator 1 VCOUT1 pin output disabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Comparator 1 VCOUT1 pin output enabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator 1 interrupt request enable Note 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator 1 interrupt request disabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Comparator 1 interrupt request enabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator 0 VCOUT0 output polarity selection</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator 0 output is output to VCOUT0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Inverted comparator 0 output is output to VCOUT0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator 0 VCOUT0 pin output enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator 0 VCOUT0 pin output disabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Comparator 0 VCOUT0 pin output enabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator 0 interrupt request enable Note 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator 0 interrupt request disabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Comparator 0 interrupt request enabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Correct:

**Figure 19 - 6 Format of Comparator output control register (COMPOCR)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>(&lt;7&gt;)</th>
<th>(&lt;6&gt;)</th>
<th>(&lt;5&gt;)</th>
<th>(&lt;4&gt;)</th>
<th>(3)</th>
<th>(&lt;2&gt;)</th>
<th>(&lt;1&gt;)</th>
<th>(&lt;0&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMPOCR</td>
<td>SPDMD</td>
<td>C1OP</td>
<td>C1OE</td>
<td>C1IE</td>
<td>0</td>
<td>C0OP</td>
<td>C0OE</td>
<td>C0IE</td>
</tr>
<tr>
<td></td>
<td>Comparator speed selection Note 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator low-speed mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Comparator high-speed mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator 1 VCOUT1 output polarity selection</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator 1 output is output to VCOUT1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Inverted comparator 1 output is output to VCOUT1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator 1 VCOUT1 pin output enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator 1 VCOUT1 pin output disabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Comparator 1 VCOUT1 pin output enabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator 1 interrupt request enable Note 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator 1 interrupt request disabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Comparator 1 interrupt request enabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator 0 VCOUT0 output polarity selection</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator 0 output is output to VCOUT0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Inverted comparator 0 output is output to VCOUT0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator 0 VCOUT0 pin output enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator 0 VCOUT0 pin output disabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Comparator 0 VCOUT0 pin output enabled Note 4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator 0 interrupt request enable Note 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 Comparator 0 interrupt request disabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 Comparator 0 interrupt request enabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Note 1. When rewriting the SPDMD bit, be sure to set the CiENB bit (i = 0 or 1) in the COMPMDR register to 0 in advance.

Note 2. If C1IE is changed from 0 (interrupt request disabled) to 1 (interrupt request enabled), since bit 1 (CMPIF1) in interrupt request flag register 2L (IF2L) may set to 1 (interrupt requested), clear bit 1 (CMPIF1) in interrupt request flag register 2L (IF2L) to 0 before using an interrupt.

Note 3. If C0IE is changed from 0 (interrupt request disabled) to 1 (interrupt request enabled), since bit 0 (CMPIF0) in interrupt request flag register 2L (IF2L) may set to 1 (interrupt requested), clear bit 0 (CMPIF0) in interrupt request flag register 2L (IF2L) to 0 before using an interrupt.

Note 4. When comparator i output is used as a trigger for functions that operate simultaneously with the timer KB, such as the forced output stop function and the timer restart function, set the CiOE bit to 1.

Remark \( i = 0, 1 \)
## 6. 19.5 Caution for Using Timer KB Simultaneous Operation Function (Page 780, Page 781)

**Incorrect:**
19.5 Caution for Using Timer KB Simultaneous Operation Function
In addition to their use as an external interrupt input, the INTP10, 11 pin output and the comparator output signal can be used as a trigger for functions that operate simultaneously with timer KB, such as the forced output stop function and timer restart function. The settings in peripheral function switch register 0 (PFSEL0) and the edge selection registers must be specified according to the function used. The width of the active signal required until each function starts operating differs.

---

**Correct:**
19.5 Caution for Using Timer KB Simultaneous Operation Function
In addition to their use as an external interrupt input, the INTP10, 11 pin output and the comparator output signal can be used as a trigger for functions that operate simultaneously with timer KB, such as the forced output stop function and timer restart function. The settings in peripheral function switch register 0 (PFSEL0), the edge selection registers and comparator output control register (COMPOCR) must be specified according to the function used. The width of the active signal required until each function starts operating differs.

---

### Table 19 - 4 Relationship of Comparator 0 and 1 Functions, Register Settings, and Active Signal Width

<table>
<thead>
<tr>
<th>Function</th>
<th>Peripheral Enable Resister Setting</th>
<th>Edge Setting Resister</th>
<th>Necessary Active Signal Width to Operate Each Function</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Interrupt</td>
</tr>
<tr>
<td>External interrupt</td>
<td>-</td>
<td>CnEDG,CnEPO (n = 0,1)</td>
<td>Up to 1.2 ns Note 1</td>
</tr>
<tr>
<td>Forced output stop</td>
<td>-</td>
<td>Note 4</td>
<td>Up to 1.2 ns Note 1</td>
</tr>
<tr>
<td>Timer Restart Note 4</td>
<td>-</td>
<td>CnEDG,CnEPO (n = 0,1)</td>
<td>Up to 1.2 ns Note 1, 2 to 3 clocks Note 3, 4</td>
</tr>
</tbody>
</table>
Figure 19 - 11 Generation Timing of Forced Output Stop Signal and Timer Restart Request Signal by INTP10, 11

Note 1. When noise filtering is set to “0, 0” by using the CnDFS1 and CnDFS0 bits in the comparator n control register (CnCTL).
   If a setting other than “0, 0” is specified, the specified noise elimination width is added.

Note 2. For fCLK or fHOCO

Note 3. Until the timer restart function starts operating, an additional clock cycle is required after the timer restart request signal is received, and an additional output delay time (10 to 40 ns) is required until the level of the timer KB output changes.

Note 4. The active level of the forced output stop function is high.

Note 5. An additional output delay time (10 to 40 ns) is required from when forced output stop function starts operating to when the level of the timer KB output changes.

Note 6. The timer restart function can be used for comparator 0 and 1 only.

Remark   $n = 0$ and 1