Date: Jan. 9, 2024

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A0132A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G23 Descriptions in the User's Manual: Hardware Rev. 1.21 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G23 Group	Lot No. All lots	Reference Document	RL78/G23 User's Manual: Hardware Rev. 1.21 R01UH0896EJ0121 (Nov. 2022)		

This document describes misstatements found in the RL78/G23 User's Manual: Hardware Rev. 1.21 (R01UH0896EJ0121).

Corrections

Applicable Item	Applicable Page	Contents
12.3.3 A/D converter mode register 0 (ADM0)	Page 547, Page 550 to Page 562	Incorrect descriptions revised
12.3.4 A/D converter mode register 1 (ADM1)	Page 564	Incorrect descriptions revised
12.3.5 A/D converter mode register 2 (ADM2)	Page 565, Page 566	Incorrect descriptions revised
20.2 Configuration of ELCL	Page 1035, Page 1037, Page 1039	Incorrect descriptions revised
20.3.1 Input signal select registers n (ELISELn) (n = 0 to 11)	Page 1042, Page 1046	Incorrect descriptions revised
20.6 Points for Caution when the ELCL is to be Used	Page 1081	Incorrect descriptions revised
29.3.3 Sequencer instruction registers p (SMSIp) (p = 0 to 31)	Page 1213, Page 1214	Incorrect descriptions revised
29.4 Operations of the SNOOZE Mode Sequencer	Page 1223	Incorrect descriptions revised
29.4.1 Internal operations of the SNOOZE mode sequencer	Page 1220	Incorrect descriptions revised
29.4.4 Procedures for running the SNOOZE mode sequencer	Page 1224	Incorrect descriptions revised
29.4.5 States of the SNOOZE mode sequencer	Page 1226	Incorrect descriptions revised
29.5.20 Interrupt plus termination	Page 1248	Incorrect descriptions revised
29.6 Operation in Standby Modes	Page 1250	Incorrect descriptions revised
37.4 AC Characteristics	Page 1431	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0896EJ0121	
1	8.3.4 Realtime clock control register 1 (RTCC1)		Page 473	Page 3
2	Figure 8-19 Procedure for Reading Realtime Clock		Page 485	Page 4
3	Figure 8-20 Procedure for Writing Realtime Clock		Page 486	Page 4
4	37.3.2 Supply current characteristics		Page 1410 to Page 1427	Page 5 to Page 18
5	37.6.4 Comparator characteristics		Page 1475	Page 19
6	12.3.3 A/D converter mode register 0 (ADM0)		Page 547, Page 550 to Page 562	Page 20 to Page 29
7	12.3.4 A/D converter mode register 1 (ADM1)		Page 564	Page 30
8	12.3.5 A/D converter mode register 2 (ADM2)		Page 565, Page 566	Page 31, Page 32
9	20.2 Configuration of ELCL		Page 1035, Page 1037, Page 1039	Page 33 to Page 35
10	20.3.1 Input signal select registers n (ELISELn) (n = 0 to 11)		Page 1042, Page 1046	Page 36, Page 37
11	20.6 Points for Caution when the ELCL is to be Used		Page 1081	Page 38
12	29.3.3 Sequencer instruction registers p (SMSIp) (p = 0 to 31)		Page 1213, Page 1214	Page 39 to Page 40
13	29.4 Operations of the SNOOZE Mode Sequencer		Page 1223	Page 41
14	29.4.1 Internal operations of the SNOOZE mode sequencer		Page 1220	Page 42
15	29.4.4 Procedures for running the SNOOZE mode sequencer		Page 1224	Page 43
16	29.4.5 States of the SNOOZE mode sequencer		Page 1226	Page 44
17	29.5.20 Interrupt plus termination		Page 1248	Page 45
18	29.6 Operation in Standby Modes		Page 1250	Page 46
19	37.4 AC Characteristics		Page 1431	Page 47

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G23 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0103A/E	Jan. 19, 2023	First edition issued Corrections No.1 to No.5 revised
TN-RL*-A0132A/E	Jan. 9, 2024	Corrections No.6 to No.19 revised (this document)

1. 8.3.4 Realtime clock control register 1 (RTCC1) (Page 473)

Incorrect:

Figure 8 - 5 Format of Realtime Clock Control Register 1 (RTCC1) (2/2)

RWAIT	Wait control of real-time clock
0	Counting proceeds.
1	Stops the SEC to YEAR counters. Counter values are readable and writable.

This bit controls the operation of the counter.
Be sure to write 1 to this bit to read or write the counter value.
So that the 16-bit internal counter continues to run, return the value of this bit to 0 on completion of reading or writing within one second.
After setting this bit to 1, it takes up to one cycle of f_{RTCCK} until the counter value can be actually read or written (RWST = 1).Notes 1, 2
When the internal counter (16 bits) overflows while the setting of this bit is 1, an indicator of the counter having overflowed is retained after RWAIT has become 0, after which counting up continues.
Note that, when the second count register has been written to, the overflow is not retained

Correct:

Figure 8 - 5 Format of Realtime Clock Control Register 1 (RTCC1) (2/2)

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value

This bit controls the operation of the counter.
Be sure to write 1 to this bit to read or write the counter value.
So that the 16-bit internal counter continues to run, return the value of this bit to 0 on completion of reading or writing within one second. When reading or writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.
After setting this bit to 1, it takes up to one cycle of f_{RTCCK} until the counter value can be actually read or written (RWST = 1).Notes 1, 2
When the internal counter (16 bits) overflows while the setting of this bit is 1, an indicator of the counter having overflowed is retained after RWAIT has become 0, after which counting up continues.
Note that, when the second count register has been written to, the overflow is not retained

2. Figure 8-19 Procedure for Reading Realtime Clock (Page 485)

Incorrect:

Note Be sure to confirm that RWST = 0 before setting STOP mode.

Caution Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), day-of-week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence. All the registers do not have to read and only some registers may be read.

Correct:

Note Be sure to confirm that RWST = 0 before setting STOP mode.

Caution Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), day-of-week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence. All the registers do not have to read and only some registers may be read.

3. Figure 8-20 Procedure for Writing Realtime Clock (Page 486)

Incorrect:

Note Be sure to confirm that RWST = 0 before setting STOP mode.

Cautions 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

Cautions 2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counting is in progress (RTCE = 1), rewrite the values of the MIN register after disabling interrupt processing of INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), day-of-week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence. All the registers do not have to be set and only some registers may be written.

Correct:

Note Be sure to confirm that RWST = 0 before setting STOP mode.

Cautions 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.

Cautions 2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counting is in progress (RTCE = 1), rewrite the values of the MIN register after disabling interrupt processing of INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), day-of-week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence. All the registers do not have to be set and only some registers may be written.

4. 37.3.2 Supply current characteristics (Page 1410 to Page 1427)

Incorrect:

37.3.2 Supply current characteristics

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) **(1/4)**

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.3	—	mA
						V_{DD} = 1.8 V		1.3	—	
					Normal operation	V_{DD} = 5.0 V		3.0	5.0	mA
						V_{DD} = 1.8 V		3.0	5.0	
				f_{MX} = 8 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V		0.8	1.3	mA
						V_{DD} = 1.8 V		0.7	1.3	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	1.4	mA
						V_{DD} = 1.8 V		0.8	1.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. **The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

Correct:

37.3.2 Supply current characteristics

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) **(1/4)**

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.3	—	mA
						V_{DD} = 1.8 V		1.3	—	
					Normal operation	V_{DD} = 5.0 V		3.0	5.0	mA
						V_{DD} = 1.8 V		3.0	5.0	
				f_{MX} = 8 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V		0.8	1.3	mA
						V_{DD} = 1.8 V		0.7	1.3	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	1.4	mA
						V_{DD} = 1.8 V		0.8	1.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 2, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		3.2	5.5	μA
						T_A = +25°C		3.5	5.8	
						T_A = +85°C		5.2	20.9	
						T_A = +105°C		7.7	38.5	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. **The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. **They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 2, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		3.2	5.5	μA
						T_A = +25°C		3.5	5.8	
						T_A = +85°C		5.2	20.9	
						T_A = +105°C		7.7	38.5	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. In the subsystem clock operation mode, the currents in both the “Typ.” and “Max.” columns do not include the operating currents of the peripheral modules.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.54	1.93	mA
					V_{DD} = 1.8 V		0.53	1.92	
				f_{MX} = 8 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.12	0.47	mA
					V_{DD} = 1.8 V		0.10	0.44	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.21	0.58	mA
					V_{DD} = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. **The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.54	1.93	mA
					V_{DD} = 1.8 V		0.53	1.92	
				f_{MX} = 8 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.12	0.47	mA
					V_{DD} = 1.8 V		0.10	0.44	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.21	0.58	mA
					V_{DD} = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (4/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 3, Low-speed on-chip oscillator operation	T_A = -40°C		0.53	2.31	μA
					T_A = +25°C		0.65	2.38	
					T_A = +50°C		0.80	4.95	
					T_A = +105°C		3.40	30.20	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. **The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped. **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 6. The listed currents with this setting allow retention of the contents of the entire RAM area. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. **They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.** For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.

Note 7. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 8. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (4/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 3, Low-speed on-chip oscillator operation	T_A = -40°C		0.53	2.31	μA
					T_A = +25°C		0.65	2.38	
					T_A = +50°C		0.80	4.95	
					T_A = +105°C		3.40	30.20	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. In the subsystem clock operation mode or the STOP mode, the currents in both the “Typ.” and “Max.” columns do not include the operating currents of the peripheral modules.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).

Note 6. The listed currents with this setting allow retention of the contents of the entire RAM area. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.

Note 7. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped.

Note 8. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). The current flowing into the RTC is included.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.4	—	mA
						V_{DD} = 1.8 V		1.4	—	
					Normal operation	V_{DD} = 5.0 V		3.0	5.0	mA
						V_{DD} = 1.8 V		3.0	5.0	
				f_{MX} = 8 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V		0.8	1.3	mA
						V_{DD} = 1.8 V		0.7	1.3	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	1.4	mA
						V_{DD} = 1.8 V		0.8	1.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. **The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.4	—	mA
						V_{DD} = 1.8 V		1.4	—	
					Normal operation	V_{DD} = 5.0 V		3.0	5.0	mA
						V_{DD} = 1.8 V		3.0	5.0	
				f_{MX} = 8 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V		0.8	1.3	mA
						V_{DD} = 1.8 V		0.7	1.3	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	1.4	mA
						V_{DD} = 1.8 V		0.8	1.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 2, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		3.3	6.1	μA
						T_A = +25°C		3.6	6.3	
						T_A = +85°C		5.3	25.6	
						T_A = +105°C		7.9	55.3	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. **The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. **They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 2, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		3.3	6.1	μA
						T_A = +25°C		3.6	6.3	
						T_A = +85°C		5.3	25.6	
						T_A = +105°C		7.9	55.3	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. In the subsystem clock operation mode, the currents in both the “Typ.” and “Max.” columns do not include the operating currents of the peripheral modules.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current[Note 1]	I_{DD2} [Note 2]	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz[Note 3]	V_{DD} = 5.0 V		0.57	1.97	mA
					V_{DD} = 1.8 V		0.56	1.96	
				f_{MX} = 8 MHz[Note 5], Square wave input	V_{DD} = 5.0 V		0.12	0.47	mA
					V_{DD} = 1.8 V		0.10	0.44	
				f_{MX} = 8 MHz[Note 5], Resonator connection	V_{DD} = 5.0 V		0.21	0.58	mA
					V_{DD} = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. **The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current[Note 1]	I_{DD2} [Note 2]	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz[Note 3]	V_{DD} = 5.0 V		0.57	1.97	mA
					V_{DD} = 1.8 V		0.56	1.96	
				f_{MX} = 8 MHz[Note 5], Square wave input	V_{DD} = 5.0 V		0.12	0.47	mA
					V_{DD} = 1.8 V		0.10	0.44	
				f_{MX} = 8 MHz[Note 5], Resonator connection	V_{DD} = 5.0 V		0.21	0.58	mA
					V_{DD} = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) **(4/4)**

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 3, Low-speed on-chip oscillator operation	T_A = -40°C		0.62	2.94	μA
					T_A = +25°C		0.74	3.00	
					T_A = +50°C		0.88	6.00	
					T_A = +105°C		4.16	45.16	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. **The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped. **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 6. The listed currents with this setting allow retention of the contents of the entire RAM area. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. **They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.** For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.

Note 7. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 8. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) **(4/4)**

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 3, Low-speed on-chip oscillator operation	T_A = -40°C		0.62	2.94	μA
					T_A = +25°C		0.74	3.00	
					T_A = +50°C		0.88	6.00	
					T_A = +105°C		4.16	45.16	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. In the subsystem clock operation mode or the STOP mode, the currents in both the “Typ.” and “Max.” columns do not include the operating currents of the peripheral modules.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).

Note 6. The listed currents with this setting allow retention of the contents of the entire RAM area. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.

Note 7. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped.

Note 8. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). The current flowing into the RTC is included.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.6	—	mA
						V_{DD} = 1.8 V		1.5	—	
					Normal operation	V_{DD} = 5.0 V		3.5	5.6	mA
						V_{DD} = 1.8 V		3.5	5.6	
				f_{MX} = 8 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V		0.9	1.5	mA
						V_{DD} = 1.8 V		0.9	1.5	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.0	1.6	mA
						V_{DD} = 1.8 V		1.0	1.6	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. **The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V		1.6	—	mA
						V_{DD} = 1.8 V		1.5	—	
					Normal operation	V_{DD} = 5.0 V		3.5	5.6	mA
						V_{DD} = 1.8 V		3.5	5.6	
				f_{MX} = 8 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V		0.9	1.5	mA
						V_{DD} = 1.8 V		0.9	1.5	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.0	1.6	mA
						V_{DD} = 1.8 V		1.0	1.6	

Note 1. The listed currents are the total currents flowing into V_{DD}, EV_{DD0} and EV_{DD1}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, EV_{DD1} or V_{SS}, EV_{SS0}, EV_{SS1}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 2, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		3.8	7.7	μA
						T_A = +25°C		4.1	8.0	
						T_A = +85°C		6.8	39.8	
						T_A = +105°C		10.8	87.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. **The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. **They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 2, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		3.8	7.7	μA
						T_A = +25°C		4.1	8.0	
						T_A = +85°C		6.8	39.8	
						T_A = +105°C		10.8	87.4	

Note 1. The listed currents are the total currents flowing into V_{DD}, EV_{DD0} and EV_{DD1}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, EV_{DD1} or V_{SS}, EV_{SS0}, EV_{SS1}. In the subsystem clock operation mode, the currents in both the “Typ.” and “Max.” columns do not include the operating currents of the peripheral modules.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.60	2.00	mA
					V_{DD} = 1.8 V		0.59	1.99	
				f_{MX} = 8 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.13	0.48	mA
					V_{DD} = 1.8 V		0.11	0.45	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.22	0.59	mA
					V_{DD} = 1.8 V		0.21	0.58	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. **The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.60	2.00	mA
					V_{DD} = 1.8 V		0.59	1.99	
				f_{MX} = 8 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.13	0.48	mA
					V_{DD} = 1.8 V		0.11	0.45	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.22	0.59	mA
					V_{DD} = 1.8 V		0.21	0.58	

Note 1. The listed currents are the total currents flowing into V_{DD}, EV_{DD0} and EV_{DD1}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, EV_{DD1} or V_{SS}, EV_{SS0}, EV_{SS1}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (4/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 3, Low-speed on-chip oscillator operation	T_A = -40°C		0.62	3.95	μA
					T_A = +25°C		0.78	4.00	
					T_A = +50°C		1.03	9.16	
					T_A = +105°C		4.64	70.14	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. **The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.**

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped. **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 6. The listed currents with this setting allow retention of the contents of the entire RAM area. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. **They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.** For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.

Note 7. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

Note 8. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). **They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.**

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (4/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 3, Low-speed on-chip oscillator operation	T_A = -40°C		0.62	3.95	μA
					T_A = +25°C		0.78	4.00	
					T_A = +50°C		1.03	9.16	
					T_A = +105°C		4.64	70.14	

Note 1. The listed currents are the total currents flowing into V_{DD}, EV_{DD0} and EV_{DD1}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, EV_{DD1} or V_{SS}, EV_{SS0}, EV_{SS1}. In the subsystem clock operation mode or the STOP mode, the currents in both the “Typ.” and “Max.” columns do not include the operating currents of the peripheral modules.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).

Note 6. The listed currents with this setting allow retention of the contents of the entire RAM area. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.

Note 7. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped.

Note 8. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). The current flowing into the RTC is included.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

5. 37.6.4 Comparator characteristics (Page 1475)

Incorrect:
37.6.4 Comparator characteristics

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage range	I_{VREF}	Input to the IVREF0 and IVREF1 pins C0LVL = 0, C1LVL = 0		0		V_{DD} - 1.4 and EV_{DD0}	V
		Input to the IVREF0 and IVREF1 pins C0LVL = 1, C1LVL = 1		1.4		EV_{DD0}	V
	I_{VCMP}	Input to the IVCMP0 and IVCMP1 pins		-0.3		EV_{DD0} + 0.3	V
Output delay	td	V_{DD} = 3.0 V, Input slew rate > 1 V/μs	High-speed mode			1.5	μs
			Low-speed mode		3.0		μs
Offset voltage	—	High-speed mode				50	mV
		Low-speed mode				40	mV
Operation stabilization wait time	t_{CMP}			30			μs
Internal reference voltage	V_{BGR2}			1.4		1.6	V

Correct:
37.6.4 Comparator characteristics

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage range	I_{VREF}	Input to the IVREF0 and IVREF1 pins C0LVL = 0, C1LVL = 0		0		V_{DD} - 1.4 and EV_{DD0}	V
		Input to the IVREF0 and IVREF1 pins C0LVL = 1, C1LVL = 1		1.4		EV_{DD0}	V
	I_{VCMP}	Input to the IVCMP0 and IVCMP1 pins		-0.3		EV_{DD0} + 0.3	V
Output delay	td	V_{DD} = 3.0 V, Input slew rate > 1 V/μs	High-speed mode			1.5	μs
			Low-speed mode		3.0		μs
Offset voltage	—	High-speed mode				50	mV
		Low-speed mode				40	mV
Operation stabilization wait time	t_{CMP}			30			μs
Internal reference voltage[Note]	V_{BGR2}			1.4		1.6	V

Note The internal reference voltage can be selected as comparator reference voltage only when 1.8 V ≤ V_{DD} ≤ 5.5 V.

6. 12.3.3 A/D converter mode register 0 (ADM0) (Page 547, Page 550 to Page 562)

Incorrect:

(Page 547)

ADCE	A/D voltage comparator operation control[Note 2]
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Note 1. For details of the FR2 to FR0, LV1, LV0 bits, and A/D conversion, see Table 12 - 3 A/D Conversion Time Selection (1/8).

Note 2. While in the software trigger no-wait mode or hardware trigger no-wait mode, the operation of the A/D voltage comparator is controlled by the ADCS and ADCE bits, and it takes 1 μs + 2 cycles of the conversion clock (f_{AD}) from the start of operation for the operation to stabilize. Therefore, immediately after the ADCS bit is set to 1 after at least 1 μs + 2 cycles of the conversion clock (f_{AD}) have elapsed from the time ADCE bit is set to 1, the conversion result becomes valid. When ADCS is set to 1 while ADCE = 0, A/D conversion starts after the stabilization wait time has passed. If ADCS is set before at least 1 μs + 2 cycles of the conversion clock (f_{AD}) have elapsed, ignore data of the first conversion.

Caution 1. Change the ADMD, FR2 to FR0, LV1, and LV0 bits while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 2. Setting change from ADCS = 1 and ADCE = 1 to ADCS = 1 and ADCE = 0 is prohibited.

Caution 3. Do not change the ADCS and ADCE bits from 0 to 1 at the same time by using an 8-bit manipulation instruction. Be sure to follow the procedure described in 12.7 A/D Converter Setup Flowchart.

Correct:

ADCE	A/D voltage comparator operation control[Note 2]
0	Stops A/D voltage comparator operation
1	Enables A/D voltage comparator operation

Note 1. For details of the FR2 to FR0, LV1, LV0 bits, and A/D conversion, see Table 12 - 3 A/D Conversion Time Selection (1/8).

Note 2. While in the software trigger no-wait mode or hardware trigger no-wait mode, the operation of the A/D voltage comparator is controlled by the ADCS and ADCE bits, and it takes 1 μs + 2 cycles of the conversion clock (f_{AD}) from the start of operation for the operation to stabilize. Therefore, immediately after the ADCS bit is set to 1 after at least 1 μs + 2 cycles of the conversion clock (f_{AD}) have elapsed from the time ADCE bit is set to 1, the conversion result becomes valid. When ADCS is set to 1 while ADCE = 0, A/D conversion starts after the stabilization wait time has passed. If ADCS is set before at least 1 μs + 2 cycles of the conversion clock (f_{AD}) have elapsed, ignore data of the first conversion.

Caution 1. Change the ADMD, FR2 to FR0, LV1, and LV0 bits while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 2. Setting change from ADCS = 1 and ADCE = 1 to ADCS = 1 and ADCE = 0 is prohibited.

Caution 3. Do not change the ADCS and ADCE bits from 0 to 1 at the same time by using an 8-bit manipulation instruction. Be sure to follow the procedure described in 12.7 A/D Converter Setup Flowchart.

Caution 4. Following stoppage of conversion by setting the ADCS and ADCE bits to 0 from the conversion standby or conversion state, wait for at least 5 μs before restoring the values of the bits to 1. Note that, when changing the settings of bits ADMD, FR2 to FR0, LV1, and LV0, start by setting the ADCS and ADCE bits to 0, then wait for at least 0.2 μs before changing the rest of the bits.

(Page 550)

ADM1	ADM0			Conversion Clock (f_{AD})	Conversion Start Time (Number of f_{CLK} Clock)	
ADLSP	FR2	FR1	FR0		Software Trigger No-wait Mode/Hardware Trigger No-wait Mode	Software trigger wait mode/ Hardware trigger wait mode
0	0	0	0	$f_{CLK}/32$	31	1
0	0	0	1	$f_{CLK}/16$	15	1
0	0	1	0	$f_{CLK}/8$	7	1
0	0	1	1	$f_{CLK}/4$	3	1
0	1	0	0	$f_{CLK}/2$	1	1
0	1	0	1	f_{CLK}	1	1
1	0	1	1	$f_{CLK}/4$	3	1
1	1	0	0	$f_{CLK}/2$	1	1
1	1	0	1	f_{CLK}	1	1

However, for the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and stabilization wait time for A/D power supply do not occur after a hardware trigger is detected.

Caution 1. If using the hardware trigger wait mode, setting the ADCS bit to 1 is prohibited (but the bit is automatically switched to 1 when the hardware trigger signal is detected). However, it is possible to clear the ADCS bit to 0 to specify the A/D conversion standby state.

Caution 2. While in the one-shot conversion mode of the hardware trigger no-wait mode, the ADCS bit is not automatically cleared to 0 when A/D conversion ends. Instead, 1 is retained.

Caution 3. Only rewrite the value of the ADCE bit when ADCS = 0 (while in the conversion stopped/conversion standby state).

Caution 4. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no wait mode: 2 f_{CLK} clock cycles + conversion start time + A/D conversion time

Hardware trigger wait mode: **2 f_{CLK} clock cycles + conversion start time + A/D power supply stabilization wait time + A/D conversion time**

ADM1	ADM0			Conversion Clock (f_{AD})	Conversion Start Time (Number of f_{CLK} Clock)	
ADLSP	FR2	FR1	FR0		Software Trigger No-wait Mode/Hardware Trigger No-wait Mode	Software trigger wait mode/ Hardware trigger wait mode
0	0	0	0	$f_{CLK}/32$	31	1
0	0	0	1	$f_{CLK}/16$	15	1
0	0	1	0	$f_{CLK}/8$	7	1
0	0	1	1	$f_{CLK}/4$	3	1
0	1	0	0	$f_{CLK}/2$	1	1
0	1	0	1	f_{CLK}	1	1
1	0	1	1	$f_{CLK}/4$	3	1
1	1	0	0	$f_{CLK}/2$	1	1
1	1	0	1	f_{CLK}	1	1

However, for the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and stabilization wait time for A/D power supply do not occur after a hardware trigger is detected.

Caution 1. If using the hardware trigger wait mode, setting the ADCS bit to 1 is prohibited (but the bit is automatically switched to 1 when the hardware trigger signal is detected). However, it is possible to clear the ADCS bit to 0 to specify the A/D conversion standby state.

Caution 2. While in the one-shot conversion mode of the hardware trigger no-wait mode, the ADCS bit is not automatically cleared to 0 when A/D conversion ends. Instead, 1 is retained.

Caution 3. Only rewrite the value of the ADCE bit when ADCS = 0 (while in the conversion stopped/conversion standby state).

Caution 4. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no wait mode: 2 f_{CLK} clock cycles + conversion start time + A/D conversion time

Hardware trigger wait mode: 2 f_{CLK} clock cycles + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 5µs

(Page 551)

Table 12 - 3 A/D Conversion Time Selection (1/8)

1. When there is no A/D power supply stabilization wait time

Normal mode 1 and 2 (for software trigger no-wait select mode and hardware trigger no-wait select mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	$f_{CLK}/32$	1 f_{AD}	64 f_{AD}	1 f_{AD}	2112/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	66 µs
0	0	0	1				$f_{CLK}/16$	1 f_{AD}	64 f_{AD}	1 f_{AD}	1056/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	66 µs	33 µs
1	1	0	1				f_{CLK}	1 f_{AD}	181 f_{AD}	1 f_{AD}	183/f_{CLK}	183 µs	45.75 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. Use normal mode 2 when the internal reference voltage or temperature sensor output voltage is selected as the target for A/D conversion.

Caution 5. When the internal reference voltage is selected as the + side reference voltage, normal modes 1 and 2 cannot be used. Use low-voltage mode 1 or 2.

Table 12 - 3 A/D Conversion Time Selection (1/8)

1. When there is no A/D power supply stabilization wait time

Normal mode 1 and 2 (for software trigger no-wait select mode and hardware trigger no-wait select mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	$f_{CLK}/32$	1 f_{AD}	64 f_{AD}	1 f_{AD}	2112/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	66 µs
0	0	0	1				$f_{CLK}/16$	1 f_{AD}	64 f_{AD}	1 f_{AD}	1056/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	66 µs	33 µs
1	1	0	1				f_{CLK}	1 f_{AD}	181 f_{AD}	1 f_{AD}	183/f_{CLK}	183 µs	45.75 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting bits FR2 to FR0, LV1, and LV0.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. Use normal mode 2 when the internal reference voltage or temperature sensor output voltage is selected as the target for A/D conversion.

Caution 5. When the internal reference voltage is selected as the + side reference voltage, normal modes 1 and 2 cannot be used. Use low-voltage mode 1 or 2.

(Page 552)

Table 12 - 3 A/D Conversion Time Selection (2/8)

2. When there is no A/D power supply stabilization wait time

Low-voltage mode 1 and 2 (for software trigger no-wait select mode and hardware trigger no-wait select mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.8 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	1	0	Low voltage 1	f_{CLK}/32	1 f_{AD}	80 f_{AD}	1 f_{AD}	2624/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	82 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	80 f_{AD}	1 f_{AD}	1312/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	41 µs
1	1	0	1				f_{CLK}	1 f_{AD}	107 f_{AD}	1 f_{AD}	109/f_{CLK}	109 µs	27.25 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or temperature sensor output voltage is selected as the target for A/D conversion, use low-voltage mode 2 and use a conversion clock (f_{AD}) with a frequency no greater than 16 MHz.

Caution 5. When the internal reference voltage is selected as the + side reference voltage, the conversion clock (f_{AD}) must be in the range from 1 to 2 MHz.

Table 12 - 3 A/D Conversion Time Selection (2/8)

2. When there is no A/D power supply stabilization wait time

Low-voltage mode 1 and 2 (for software trigger no-wait select mode and hardware trigger no-wait select mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.8 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	1	0	Low voltage 1	f_{CLK}/32	1 f_{AD}	80 f_{AD}	1 f_{AD}	2624/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	82 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	80 f_{AD}	1 f_{AD}	1312/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	82 µs	41 µs
1	1	0	1				f_{CLK}	1 f_{AD}	107 f_{AD}	1 f_{AD}	109/f_{CLK}	109 µs	27.25 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting bits FR2 to FR0, LV1, and LV0.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or temperature sensor output voltage is selected as the target for A/D conversion, use low-voltage mode 2 and use a conversion clock (f_{AD}) with a frequency no greater than 16 MHz.

Caution 5. When the internal reference voltage is selected as the + side reference voltage, the conversion clock (f_{AD}) must be in the range from 1 to 2 MHz.

(Page 553 to Page 554)

Table 12 - 3 A/D Conversion Time Selection (3/8)

3. When there is A/D power supply stabilization wait time

Normal mode 1 and 2 (for software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay Note 2	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	4 f_{AD}	64 f_{AD}	4 f_{AD}	2304/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	72 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	64 f_{AD}	4 f_{AD}	1152/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	72 µs	36 µs
1	1	0	1				f_{CLK}	6 f_{AD}	181 f_{AD}	4 f_{AD}	191/f_{CLK}	191 µs	47.75 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected (see Table 12 - 3 A/D Conversion Time Selection (1/8)).

Note 2. The value in this column is applicable when the one-shot conversion mode is selected. When the sequential conversion mode is selected, the number of clock cycles is shortened by 3 cycles of the conversion clock (f_{AD}).

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. The conversion times in hardware trigger wait mode include the A/D power supply stabilization wait time from the time the hardware trigger is detected. The conversion times in software trigger wait mode include the A/D power supply stabilization wait time from the time the ADCS bit is set to 1.

Table 12 - 3 A/D Conversion Time Selection (3/8)

3. When there is A/D power supply stabilization wait time

Normal mode 1 and 2 (for software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay Note 2	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)					
(ADM1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V				
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	4 f_{AD}	64 f_{AD}	4 f_{AD}	2304/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	72 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	64 f_{AD}	4 f_{AD}	1152/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	72 µs	36 µs
1	1	0	1				f_{CLK}	6 f_{AD}	181 f_{AD}	4 f_{AD}	191/f_{CLK}	191 µs	47.75 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected (see Table 12 - 3 A/D Conversion Time Selection (1/8)).

Note 2. The value in this column is applicable when the one-shot conversion mode is selected. When the sequential conversion mode is selected, the number of clock cycles is shortened by 3 cycles of the conversion clock (f_{AD}).

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting bits FR2 to FR0, LV1, and LV0.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. The conversion times in hardware trigger wait mode include the A/D power supply stabilization wait time from the time the hardware trigger is detected. The conversion times in software trigger wait mode include the A/D power supply stabilization wait time from the time the ADCS bit is set to 1.

(Page 555 to Page 556)

Table 12 - 3 A/D Conversion Time Selection (4/8)

4. When there is A/D power supply stabilization wait time

Low-voltage mode 1 and 2 (for software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay Note 2	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.8 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	1	0	Low voltage 1	f_{CLK}/32	4 f_{AD}	80 f_{AD}	4 f_{AD}	2816/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	88 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	80 f_{AD}	4 f_{AD}	1408/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	88 µs	44 µs
1	1	0	1				f_{CLK}	6 f_{AD}	107 f_{AD}	4 f_{AD}	117/f_{CLK}	117 µs	29.25 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected (see Table 12 - 3 A/D Conversion Time Selection (2/8)).

Note 2. The value in this column is applicable when the one-shot conversion mode is selected. When the sequential conversion mode is selected, the number of clock cycles is shortened by 3 cycles of the conversion clock (f_{AD}).

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. The conversion times in hardware trigger wait mode include the A/D power supply stabilization wait time from the time the hardware trigger is detected. The conversion times in software trigger wait mode include the A/D power supply stabilization wait time from the time the ADCS bit is set to 1.

Table 12 - 3 A/D Conversion Time Selection (4/8)

4. When there is A/D power supply stabilization wait time

Low-voltage mode 1 and 2 (for software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay Note 2	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.8 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	1	0	Low voltage 1	f_{CLK}/32	4 f_{AD}	80 f_{AD}	4 f_{AD}	2816/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	88 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	80 f_{AD}	4 f_{AD}	1408/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	88 µs	44 µs
1	1	0	1				f_{CLK}	6 f_{AD}	107 f_{AD}	4 f_{AD}	117/f_{CLK}	117 µs	29.25 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected (see Table 12 - 3 A/D Conversion Time Selection (2/8)).

Note 2. The value in this column is applicable when the one-shot conversion mode is selected. When the sequential conversion mode is selected, the number of clock cycles is shortened by 3 cycles of the conversion clock (f_{AD}).

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting bits FR2 to FR0, LV1, and LV0.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. The conversion times in hardware trigger wait mode include the A/D power supply stabilization wait time from the time the hardware trigger is detected. The conversion times in software trigger wait mode include the A/D power supply stabilization wait time from the time the ADCS bit is set to 1.

(Page 557)

Table 12 - 3 A/D Conversion Time Selection (5/8)

5. When there is no A/D power supply stabilization wait time

Normal mode 1 and 2 (for software trigger no-wait scan mode and hardware trigger no-wait scan mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time × 4 + Interrupt Output Delay Time)					
(AD M1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V				
ADL SP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	1 f_{AD}	64 f_{AD}	1 f_{AD}	8256/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	258 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	64 f_{AD}	1 f_{AD}	4128/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	258 µs	129 µs
1	1	0	1				f_{CLK}	1 f_{AD}	181 f_{AD}	1 f_{AD}	726/f_{CLK}	726 µs	181.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. Use normal mode 2 when the internal reference voltage or temperature sensor output voltage is selected as the target for A/D conversion.

Caution 5. When the internal reference voltage is selected as the + side reference voltage, normal modes 1 and 2 cannot be used. Use low-voltage mode 1 or 2.

Table 12 - 3 A/D Conversion Time Selection (5/8)

5. When there is no A/D power supply stabilization wait time

Normal mode 1 and 2 (for software trigger no-wait scan mode and hardware trigger no-wait scan mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time × 4 + Interrupt Output Delay Time)					
(AD M1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V				
ADL SP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	1 f_{AD}	64 f_{AD}	1 f_{AD}	8256/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	258 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	64 f_{AD}	1 f_{AD}	4128/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	258 µs	129 µs
1	1	0	1				f_{CLK}	1 f_{AD}	181 f_{AD}	1 f_{AD}	726/f_{CLK}	726 µs	181.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting bits FR2 to FR0, LV1, and LV0.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. Use normal mode 2 when the internal reference voltage or temperature sensor output voltage is selected as the target for A/D conversion.

Caution 5. When the internal reference voltage is selected as the + side reference voltage, normal modes 1 and 2 cannot be used. Use low-voltage mode 1 or 2.

(Page 558)

Table 12 - 3 A/D Conversion Time Selection (6/8)

6. When there is no A/D power supply stabilization wait time

Low-voltage mode 1 and 2 (for software trigger no-wait scan mode and hardware trigger no-wait scan mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.8 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	1	0	Low voltage 1	f_{CLK}/32	1 f_{AD}	80 f_{AD}	1 f_{AD}	10304/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	322 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	80 f_{AD}	1 f_{AD}	5152/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	322 µs	161 µs
1	1	0	1				f_{CLK}	1 f_{AD}	107 f_{AD}	1 f_{AD}	430/f_{CLK}	430 µs	107.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or temperature sensor output voltage is selected as the target for A/D conversion, use low-voltage mode 2 and use a conversion clock (f_{AD}) with a frequency no greater than 16 MHz.

Caution 5. When the internal reference voltage is selected as the + side reference voltage, the conversion clock (f_{AD}) must be in the range from 1 to 2 MHz.

Table 12 - 3 A/D Conversion Time Selection (6/8)

6. When there is no A/D power supply stabilization wait time

Low-voltage mode 1 and 2 (for software trigger no-wait scan mode and hardware trigger no-wait scan mode)

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for Conversion Start Delay	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay	A/D Conversion Time (Conversion Start Delay Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.8 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	1	0	Low voltage 1	f_{CLK}/32	1 f_{AD}	80 f_{AD}	1 f_{AD}	10304/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	322 µs
0	0	0	1				f_{CLK}/16	1 f_{AD}	80 f_{AD}	1 f_{AD}	5152/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	322 µs	161 µs
1	1	0	1				f_{CLK}	1 f_{AD}	107 f_{AD}	1 f_{AD}	430/f_{CLK}	430 µs	107.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting bits FR2 to FR0, LV1, and LV0.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. When the internal reference voltage or temperature sensor output voltage is selected as the target for A/D conversion, use low-voltage mode 2 and use a conversion clock (f_{AD}) with a frequency no greater than 16 MHz.

Caution 5. When the internal reference voltage is selected as the + side reference voltage, the conversion clock (f_{AD}) must be in the range from 1 to 2 MHz.

(Page 559 to Page 560)

Table 12 - 3 A/D Conversion Time Selection (7/8)

7. When there is A/D power supply stabilization wait time

Normal mode 1 and 2 (for software trigger wait scan mode and hardware trigger wait scan mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay Note 2	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V			
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	4 f_{AD}	64 f_{AD}	4 f_{AD}	8448/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	264 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	64 f_{AD}	4 f_{AD}	4224/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	264 µs	132 µs
1	1	0	1				f_{CLK}	6 f_{AD}	181 f_{AD}	4 f_{AD}	734/f_{CLK}	734 µs	183.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected (see Table 12 - 3 A/D Conversion Time Selection (1/8)).

Note 2. The value in this column is applicable when the one-shot conversion mode is selected. When the sequential conversion mode is selected, the number of clock cycles is shortened by 3 cycles of the conversion clock (f_{AD}).

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. The conversion times in hardware trigger wait mode include the A/D power supply stabilization wait time from the time the hardware trigger is detected. The conversion times in software trigger wait mode include the A/D power supply stabilization wait time from the time the ADCS bit is set to 1.

Table 12 - 3 A/D Conversion Time Selection (7/8)

7. When there is A/D power supply stabilization wait time

Normal mode 1 and 2 (for software trigger wait scan mode and hardware trigger wait scan mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay Note 2	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V			
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	4 f_{AD}	64 f_{AD}	4 f_{AD}	8448/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	264 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	64 f_{AD}	4 f_{AD}	4224/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	264 µs	132 µs
1	1	0	1				f_{CLK}	6 f_{AD}	181 f_{AD}	4 f_{AD}	734/f_{CLK}	734 µs	183.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected (see Table 12 - 3 A/D Conversion Time Selection (1/8)).

Note 2. The value in this column is applicable when the one-shot conversion mode is selected. When the sequential conversion mode is selected, the number of clock cycles is shortened by 3 cycles of the conversion clock (f_{AD}).

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting bits FR2 to FR0, LV1, and LV0.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. The conversion times in hardware trigger wait mode include the A/D power supply stabilization wait time from the time the hardware trigger is detected. The conversion times in software trigger wait mode include the A/D power supply stabilization wait time from the time the ADCS bit is set to 1.

(Page 561 to Page 562)

Table 12 - 3 A/D Conversion Time Selection (8/8)

8. When there is A/D power supply stabilization wait time

Low-voltage mode 1 and 2 (for software trigger wait scan mode and hardware trigger wait scan mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay Note 2	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.8 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	1	0	Low voltage 1	$f_{CLK}/32$	4 f_{AD}	80 f_{AD}	4 f_{AD}	10496/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	328 µs
0	0	0	1				$f_{CLK}/16$	4 f_{AD}	80 f_{AD}	4 f_{AD}	5248/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	328 µs	164 µs
1	1	0	1				f_{CLK}	6 f_{AD}	107 f_{AD}	4 f_{AD}	438/f_{CLK}	438 µs	109.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected (see Table 12 - 3 A/D Conversion Time Selection (2/8)).

Note 2. The value in this column is applicable when the one-shot conversion mode is selected. When the sequential conversion mode is selected, the number of clock cycles is shortened by 3 cycles of the conversion clock (f_{AD}).

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. The conversion times in hardware trigger wait mode include the A/D power supply stabilization wait time from the time the hardware trigger is detected. The conversion times in software trigger wait mode include the A/D power supply stabilization wait time from the time the ADCS bit is set to 1.

Table 12 - 3 A/D Conversion Time Selection (8/8)

8. When there is A/D power supply stabilization wait time

Low-voltage mode 1 and 2 (for software trigger wait scan mode and hardware trigger wait scan mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay Note 2	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time × 4 + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	1.8 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V	2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	1	0	Low voltage 1	$f_{CLK}/32$	4 f_{AD}	80 f_{AD}	4 f_{AD}	10496/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	328 µs
0	0	0	1				$f_{CLK}/16$	4 f_{AD}	80 f_{AD}	4 f_{AD}	5248/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	328 µs	164 µs
1	1	0	1				f_{CLK}	6 f_{AD}	107 f_{AD}	4 f_{AD}	438/f_{CLK}	438 µs	109.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above							Setting prohibited									

Note 1. For the second and subsequent conversion in sequential conversion mode and for conversion of the channels specified for scan 1, 2, and 3 in scan mode, the conversion start time and A/D power supply stabilization wait time do not occur after a hardware trigger is detected (see Table 12 - 3 A/D Conversion Time Selection (2/8)).

Note 2. The value in this column is applicable when the one-shot conversion mode is selected. When the sequential conversion mode is selected, the number of clock cycles is shortened by 3 cycles of the conversion clock (f_{AD}).

Caution 1. The A/D conversion time must be selected within the relevant ranges of the conversion clock (f_{AD}) and conversion times (t_{CONV}) described in 37.6.1 A/D converter characteristics.

Caution 2. Rewrite the FR2 to FR0, LV1, and LV0 bits to different values while conversion is stopped (ADCS = 0, ADCE = 0). When conversion is to be stopped while the A/D converter is on standby or is operating, wait for at least 0.2 µs before setting bits FR2 to FR0, LV1, and LV0.

Caution 3. The above conversion times do not include the conversion start time. Add the conversion start time to obtain the time for the first conversion. Additionally, the conversion times do not include clock frequency errors. Consider clock frequency errors when selecting the conversion time.

Caution 4. The conversion times in hardware trigger wait mode include the A/D power supply stabilization wait time from the time the hardware trigger is detected. The conversion times in software trigger wait mode include the A/D power supply stabilization wait time from the time the ADCS bit is set to 1.

7. 12.3.4 A/D converter mode register 1 (ADM1) (Page 564)

Incorrect:

Caution 1. Only rewrite the value of the ADM1 register while conversion operation is stopped (ADCS = 0, ADCE = 0).

Caution 2. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no wait mode: 2 f_{CLK} clock cycles + conversion start time + A/D conversion time

Hardware trigger wait mode: **2 f_{CLK} clock cycles + conversion start time + A/D power supply stabilization wait time + A/D conversion time**

Caution 3. In modes other than the SNOOZE mode, input of the next INTRTC or INTITL will not be recognized as a valid hardware trigger for up to four f_{CLK} cycles after the first INTRTC or INTITL is input.

Correct:

Caution 1. Only rewrite the value of the ADM1 register while conversion operation is stopped (ADCS = 0, ADCE = 0).

Caution 2. To complete A/D conversion, specify at least the following time as the hardware trigger interval:

Hardware trigger no wait mode: 2 f_{CLK} clock cycles + conversion start time + A/D conversion time

Hardware trigger wait mode: 2 f_{CLK} clock cycles + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 5μs

Caution 3. In modes other than the SNOOZE mode, input of the next INTRTC or INTITL will not be recognized as a valid hardware trigger for up to four f_{CLK} cycles after the first INTRTC or INTITL is input.

8. 12.3.5 A/D converter mode register 2 (ADM2) (Page 565, Page 566)

Incorrect:

(Page 565)

Figure 12 - 8 Format of A/D Converter Mode Register 2 (ADM2) (1/2)

Address: F0010H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	ADTYP1	ADTYP0

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from VDD
0	1	Supplied from P20/AVREFP/ANI0
1	0	Supplied from the internal reference voltage (1.48 V (typ.))
1	1	Discharged

- Use the following procedures to rewrite the ADREFP1 and ADREFP0 bits.
  1. Set ADCE = 0
  2. Set both ADREFP1 and ADREFP0 to 1.
     This step is only necessary when the values of ADREFP1 and ADREFP0 are changed to 1 and 0, respectively.
  3. Reference voltage discharge time: 1 µs
     This step is only necessary when the values of ADREFP1 and ADREFP0 are changed to 1 and 0, respectively.
  4. Change the values of ADREFP1 and ADREFP0
  5. Reference voltage stabilization wait time count A
  6. Set ADCE = 1
  7. Reference voltage stabilization wait time count B
     When ADREFP1 and ADREFP0 are set to 1 and 0, A = 5 µs and B = 1 µs + 2 cycles of the conversion clock (f_{AD}).
     When ADREFP1 and ADREFP0 are set to 0 and 0 or 0 and 1, **A needs no wait** and B = 1 µs + 2 cycles of the conversion clock (f_{AD}).
  After 7. stabilization time, start the A/D conversion.
- When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the temperature sensor output voltage and internal reference voltage (1.48 V (typ.)).

Be sure to perform A/D conversion while ADISS = 0.

Correct:

Figure 12 - 8 Format of A/D Converter Mode Register 2 (ADM2) (1/2)

Address: F0010H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	ADTYP1	ADTYP0

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from VDD
0	1	Supplied from P20/AVREFP/ANI0
1	0	Supplied from the internal reference voltage (1.48 V (typ.))
1	1	Discharged

- Use the following procedures to rewrite the ADREFP1 and ADREFP0 bits.
  1. Set ADCE = 0
  2. Wait for at least 0.2 µs.
  3. Set both ADREFP1 and ADREFP0 to 1.
     This step is only necessary when the values of ADREFP1 and ADREFP0 are changed to 1 and 0, respectively.
  4. Reference voltage discharge time: 1 µs
     This step is only necessary when the values of ADREFP1 and ADREFP0 are changed to 1 and 0, respectively.
  5. Change the values of ADREFP1 and ADREFP0
  6. Reference voltage stabilization wait time count A
  7. Set ADCE = 1
  8. Reference voltage stabilization wait time count B
     When ADREFP1 and ADREFP0 are set to 1 and 0, A = 5 µs and B = 1 µs + 2 cycles of the conversion clock (f_{AD}).
     When ADREFP1 and ADREFP0 are set to 0 and 0 or 0 and 1, A = 4.8 µs and B = 1 µs + 2 cycles of the conversion clock (f_{AD}).
  After 8. stabilization time, start the A/D conversion.
- When ADREFP1 and ADREFP0 are set to 1 and 0, respectively, A/D conversion cannot be performed on the temperature sensor output voltage and internal reference voltage (1.48 V (typ.)).

Be sure to perform A/D conversion while ADISS = 0.

(Page 566)

AWC	Specification of the SNOOZE mode
0	Do not use the SNOOZE mode.
1	Use the SNOOZE mode.

When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode).

- The SNOOZE mode can only be specified when the high-speed on-chip oscillator clock or medium-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (f_{CLK}). If any other clock is selected, specifying this mode is prohibited.
- When using the SNOOZE mode, set AWC to 0 in software trigger wait mode, and set AWC to 1 in hardware trigger wait mode.
- Using the SNOOZE mode in the software trigger no-wait mode or hardware trigger no-wait mode is prohibited.
- Using the SNOOZE mode in hardware trigger no-wait mode in sequential conversion mode is prohibited.
- When using the SNOOZE mode, specify a hardware trigger interval of at least "**shift time to SNOOZE mode[Note] + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 2 f_{CLK} clock cycles**".
- Even when using the SNOOZE mode, be sure to set the AWC bit to 0 in normal operation and change it to 1 just before shifting to STOP mode.
  Also, be sure to change the AWC bit to 0 after returning from STOP mode to normal operation.
  If the AWC bit is left set to 1, A/D conversion will not start normally in spite of the subsequent SNOOZE mode or normal operation.

AWC	Specification of the SNOOZE mode
0	Do not use the SNOOZE mode.
1	Use the SNOOZE mode.

When there is a hardware trigger signal in the STOP mode, the STOP mode is exited, and A/D conversion is performed without operating the CPU (the SNOOZE mode).

- The SNOOZE mode can only be specified when the high-speed on-chip oscillator clock or medium-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (f_{CLK}). If any other clock is selected, specifying this mode is prohibited.
- When using the SNOOZE mode, set AWC to 0 in software trigger wait mode, and set AWC to 1 in hardware trigger wait mode.
- Using the SNOOZE mode in the software trigger no-wait mode or hardware trigger no-wait mode is prohibited.
- Using the SNOOZE mode in hardware trigger no-wait mode in sequential conversion mode is prohibited.
- When using the SNOOZE mode, specify a hardware trigger interval of at least "shift time to SNOOZE mode[Note] + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 2 f_{CLK} clock cycles + 5µs".
- Even when using the SNOOZE mode, be sure to set the AWC bit to 0 in normal operation and change it to 1 just before shifting to STOP mode.
  Also, be sure to change the AWC bit to 0 after returning from STOP mode to normal operation.
  If the AWC bit is left set to 1, A/D conversion will not start normally in spite of the subsequent SNOOZE mode or normal operation.

9. 20.2 Configuration of ELCL (Page 1035, Page 1037, Page 1039)

Incorrect:

(Page 1035)

Table 20 - 1 Connections in Logic Cell Block L1 (1)

Signal selection block n of event link L1	Input Signal	Destination of the signal to be output from signal selection block n of event link L1
Signal selection block 0 of event link L1Note 1	• Signals selected by the ELISEL0 to ELISEL11 registers Use the ELL1SEL0 register to select one signal to be input to logic cell block L1 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input) • Flip-flop 1 (input) Use the ELL1LNK0 register to select one of the above destinations.
Signal selection block 1 of event link L1Note 1	• Signals selected by the ELISEL0 to ELISEL11 registers Use the ELL1SEL1 register to select one signal to be input to logic cell block L1 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input) • Flip-flop 1 (input) Use the ELL1LNK1 register to select one of the above destinations.
Signal selection block 2 of event link L1Note 1	• Signals selected by the ELISEL0 to ELISEL11 registers Use the ELL1SEL2 register to select one signal to be input to logic cell block L1 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input) • Flip-flop 1 (input) Use the ELL1LNK2 register to select one of the above destinations.
Signal selection block 3 of event link L1Note 1	• Signals selected by the ELISEL0 to ELISEL11 registers Use the ELL1SEL3 register to select one signal to be input to logic cell block L1 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input) • Flip-flop 1 (input) Use the ELL1LNK3 register to select one of the above destinations.
Signal selection block 4 of event link L1Note 2	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL1SEL4 register to select one signal to be input to logic cell block L1 from among the signals selectable by the above registers.	• Flip-flop 0 (set or reset) • Flip-flop 1 (set or reset) Use the ELL1LNK4 register to select a destination.
Signal selection block 5 of event link L1Note 2	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL1SEL5 register to select one signal to be input to logic cell block L1 from among the signals selectable by the above registers.	• Flip-flop 0 (set or reset) • Flip-flop 1 (set or reset) Use the ELL1LNK5 register to select a destination.
Signal selection block 6 of event link L1	• ~~f_{CLK} ($f_{CLK} \leq 16$ MHz) Use the ELISEL6 to ELISEL11 registers and the ELL1SEL6 register to select f_{CLK}.~~	• Flip-flop 0 (clock) • Flip-flop 1 (clock) Use the ELL1LNK6 register to select a destination.

Note 1. Select different destination of the signal to be output from signal selection blocks 0 to 6 of event link L1; do not connect two or more signals to a single destination.

Note 2. Do not connect a single signal to both the set and reset control of flip-flop 0 or 1. Make sure that there is no period during which the signals for set and for reset are both high at the same time.

Correct:

Table 20 - 1 Connections in Logic Cell Block L1 (1)

Signal selection block n of event link L1	Input Signal	Destination of the signal to be output from signal selection block n of event link L1
Signal selection block 0 of event link L1Note 1	• Signals selected by the ELISEL0 to ELISEL11 registers Use the ELL1SEL0 register to select one signal to be input to logic cell block L1 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input) • Flip-flop 1 (input) Use the ELL1LNK0 register to select one of the above destinations.
Signal selection block 1 of event link L1Note 1	• Signals selected by the ELISEL0 to ELISEL11 registers Use the ELL1SEL1 register to select one signal to be input to logic cell block L1 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input) • Flip-flop 1 (input) Use the ELL1LNK1 register to select one of the above destinations.
Signal selection block 2 of event link L1Note 1	• Signals selected by the ELISEL0 to ELISEL11 registers Use the ELL1SEL2 register to select one signal to be input to logic cell block L1 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input) • Flip-flop 1 (input) Use the ELL1LNK2 register to select one of the above destinations.
Signal selection block 3 of event link L1Note 1	• Signals selected by the ELISEL0 to ELISEL11 registers Use the ELL1SEL3 register to select one signal to be input to logic cell block L1 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input) • Flip-flop 1 (input) Use the ELL1LNK3 register to select one of the above destinations.
Signal selection block 4 of event link L1Note 2	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL1SEL4 register to select one signal to be input to logic cell block L1 from among the signals selectable by the above registers.	• Flip-flop 0 (set or reset) • Flip-flop 1 (set or reset) Use the ELL1LNK4 register to select a destination.
Signal selection block 5 of event link L1Note 2	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL1SEL5 register to select one signal to be input to logic cell block L1 from among the signals selectable by the above registers.	• Flip-flop 0 (set or reset) • Flip-flop 1 (set or reset) Use the ELL1LNK5 register to select a destination.
Signal selection block 6 of event link L1	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL1SEL6 register to select one signal to be input to logic cell block L1 from among the signals selectable by the above registers.	• Flip-flop 0 (clock) • Flip-flop 1 (clock) Use the ELL1LNK6 register to select a destination.

Note 1. Select different destination of the signal to be output from signal selection blocks 0 to 6 of event link L1; do not connect two or more signals to a single destination.

Note 2. Do not connect a single signal to both the set and reset control of flip-flop 0 or 1. Make sure that there is no period during which the signals for set and for reset are both high at the same time.

(Page 1037)

Table 20 - 3 Connections in Logic Cell Block L2 (1)

Signal selection block n of event link L2	Input Signal	Destination of the signal to be output from signal selection block n of event link L2
Signal selection block 0 of event link L2Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L1 Use the ELL2SEL0 register to select one signal to be input to logic cell block L2 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL2LNK0 register to select one of the above destinations.
Signal selection block 1 of event link L2Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L1 Use the ELL2SEL1 register to select one signal to be input to logic cell block L2 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL2LNK1 register to select one of the above destinations.
Signal selection block 2 of event link L2Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L1 Use the ELL2SEL2 register to select one signal to be input to logic cell block L2 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL2LNK2 register to select one of the above destinations.
Signal selection block 3 of event link L2Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L1 Use the ELL2SEL3 register to select one signal to be input to logic cell block L2 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL2LNK3 register to select one of the above destinations.
Signal selection block 4 of event link L2Note 2	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL2SEL4 register to select one signal to be input to logic cell block L2 from among the signals selectable by the above registers.	• Flip-flop 1 (set) Use the ELL2LNK4 register to select one of the above destinations.
Signal selection block 5 of event link L2Note 2	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL2SEL5 register to select one signal to be input to logic cell block L2 from among the signals selectable by the above registers.	• Flip-flop 1 (reset) Use the ELL2LNK5 register to select one of the above destinations.
Signal selection block 6 of event link L2	• ~~f_{CLK} ($f_{CLK} \leq 16$ MHz) Use the ELISEL6 to ELISEL11 registers and the ELL2SEL6 register to select f_{CLK}.~~	• Flip-flop 0 (clock) • Flip-flop 1 (clock) Use the ELL2LNK6 register to select one of the above destinations.

Note 1. Select different destination of the signal to be output from signal selection blocks 0 to 6 of event link L2; do not connect two or more signals to a single destination.

Note 2. Do not connect a single signal to both the set and reset control of flip-flop 0 or 1. Make sure that there is no period during which the signals for set and for reset are both high at the same time.

Table 20 - 3 Connections in Logic Cell Block L2 (1)

Signal selection block n of event link L2	Input Signal	Destination of the signal to be output from signal selection block n of event link L2
Signal selection block 0 of event link L2Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L1 Use the ELL2SEL0 register to select one signal to be input to logic cell block L2 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL2LNK0 register to select one of the above destinations.
Signal selection block 1 of event link L2Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L1 Use the ELL2SEL1 register to select one signal to be input to logic cell block L2 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL2LNK1 register to select one of the above destinations.
Signal selection block 2 of event link L2Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L1 Use the ELL2SEL2 register to select one signal to be input to logic cell block L2 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL2LNK2 register to select one of the above destinations.
Signal selection block 3 of event link L2Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L1 Use the ELL2SEL3 register to select one signal to be input to logic cell block L2 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL2LNK3 register to select one of the above destinations.
Signal selection block 4 of event link L2Note 2	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL2SEL4 register to select one signal to be input to logic cell block L2 from among the signals selectable by the above registers.	• Flip-flop 1 (set) Use the ELL2LNK4 register to select one of the above destinations.
Signal selection block 5 of event link L2Note 2	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL2SEL5 register to select one signal to be input to logic cell block L2 from among the signals selectable by the above registers.	• Flip-flop 1 (reset) Use the ELL2LNK5 register to select one of the above destinations.
Signal selection block 6 of event link L2	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL2SEL6 register to select one signal to be input to logic cell block L2 from among the signals selectable by the above registers.	• Flip-flop 0 (clock) • Flip-flop 1 (clock) Use the ELL2LNK6 register to select one of the above destinations.

Note 1. Select different destination of the signal to be output from signal selection blocks 0 to 6 of event link L2; do not connect two or more signals to a single destination.

Note 2. Do not connect a single signal to both the set and reset control of flip-flop 0 or 1. Make sure that there is no period during which the signals for set and for reset are both high at the same time.

(Page 1039)

Table 20 - 5 Connections in Logic Cell Block L3 (1)

Signal selection block n of event link L3	Input Signal	Destination of the signal to be output from signal selection block n of event link L3
Signal selection block 0 of event link L3Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L2 Use the ELL3SEL0 register to select one signal to be input to logic cell block L3 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL3LNK0 register to select one of the above destinations.
Signal selection block 1 of event link L3Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L2 Use the ELL3SEL1 register to select one signal to be input to logic cell block L3 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL3LNK1 register to select one of the above destinations.
Signal selection block 2 of event link L3Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L2 Use the ELL3SEL2 register to select one signal to be input to logic cell block L3 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL3LNK2 register to select one of the above destinations.
Signal selection block 3 of event link L3Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L2 Use the ELL3SEL3 register to select one signal to be input to logic cell block 3 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL3LNK3 register to select one of the above destinations.
Signal selection block 4 of event link L3Note 2	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL3SEL4 register to select one signal to be input to logic cell block L3 from among the signals selectable by the above registers.	• Flip-flop 1 (set) Use the ELL3LNK4 register to select one of the above destinations.
Signal selection block 5 of event link L3Note 2	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL3SEL5 register to select one signal to be input to logic cell block L3 from among the signals selectable by the above registers.	• Flip-flop 1 (reset) Use the ELL3LNK5 register to select one of the above destinations.
Signal selection block 6 of event link L3	• f_{CLK} ($f_{CLK} \leq 16$ MHz) Use the ELISEL6 to ELISEL11 registers and the ELL3SEL6 register to select f_{CLK}.	• Flip-flop 0 (clock) • Flip-flop 1 (clock) Use the ELL3LNK6 register to select one of the above destinations.

Note 1. Select different destination of the signal to be output from signal selection blocks 0 to 6 of event link L3; do not connect two or more signals to a single destination.

Note 2. Do not connect a single signal to both the set and reset control of flip-flop 0 or 1. Make sure that there is no period during which the signals for set and for reset are both high at the same time.

Table 20 - 5 Connections in Logic Cell Block L3 (1)

Signal selection block n of event link L3	Input Signal	Destination of the signal to be output from signal selection block n of event link L3
Signal selection block 0 of event link L3Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L2 Use the ELL3SEL0 register to select one signal to be input to logic cell block L3 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL3LNK0 register to select one of the above destinations.
Signal selection block 1 of event link L3Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L2 Use the ELL3SEL1 register to select one signal to be input to logic cell block L3 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL3LNK1 register to select one of the above destinations.
Signal selection block 2 of event link L3Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L2 Use the ELL3SEL2 register to select one signal to be input to logic cell block L3 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL3LNK2 register to select one of the above destinations.
Signal selection block 3 of event link L3Notes 1, 2	• Signals selected by the ELISEL0 to ELISEL11 registers • Signals 0 to 4 output from logic cell block L2 Use the ELL3SEL3 register to select one signal to be input to logic cell block 3 from among the signals selectable by the above registers.	• Logic cell 0 (input 0 or input 1) • Logic cell 1 (input 0 or input 1) • Selector (selection, input 0 or input 1) • Flip-flop 0 (input, set, or reset) • Flip-flop 1 (input) Use the ELL3LNK3 register to select one of the above destinations.
Signal selection block 4 of event link L3Note 2	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL3SEL4 register to select one signal to be input to logic cell block L3 from among the signals selectable by the above registers.	• Flip-flop 1 (set) Use the ELL3LNK4 register to select one of the above destinations.
Signal selection block 5 of event link L3Note 2	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL3SEL5 register to select one signal to be input to logic cell block L3 from among the signals selectable by the above registers.	• Flip-flop 1 (reset) Use the ELL3LNK5 register to select one of the above destinations.
Signal selection block 6 of event link L3	• Signals selected by the ELISEL6 to ELISEL11 registers Use the ELL3SEL6 register to select one signal to be input to logic cell block L3 from among the signals selectable by the above registers.	• Flip-flop 0 (clock) • Flip-flop 1 (clock) Use the ELL3LNK6 register to select one of the above destinations.

Note 1. Select different destination of the signal to be output from signal selection blocks 0 to 6 of event link L3; do not connect two or more signals to a single destination.

Note 2. Do not connect a single signal to both the set and reset control of flip-flop 0 or 1. Make sure that there is no period during which the signals for set and for reset are both high at the same time.

10. 20.3.1 Input signal select registers n (ELISELn) (n = 0 to 11) (Page 1042, Page 1046)

Incorrect:

(Page 1042)

Figure 20 - 5 Format of Input Signal Select Registers n (ELISELn) (n = 0 to 11) (1/3)

Address: F0680H (ELISEL0) to F068BH (ELISEL11)
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
ELISELn	0	0	0	ELISEL n4	ELISEL n3	ELISEL n2	ELISEL n1	ELISEL n0

Correct:

Figure 20 - 5 Format of Input Signal Select Registers n (ELISELn) (n = 0 to 11) (1/3)

Address: F0680H (ELISEL0) to F068BH (ELISEL11)
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
ELISELn	0	0	0	ELISEL n4	ELISEL n3	ELISEL n2	ELISEL n1	ELISEL n0

Caution Setting of bits 4 to 0 of the ELISEL6 register to 11010B is prohibited.

(Page 1046)

Note 4. The interrupt sources that are selectable as event sources for INTC4 to INTC9 depend on which of the ELISELn (n = 6 to 11) registers is being set. Use the interrupt request signals as the hardware triggers for event-receiving peripheral functions.

Register	Event Source					
	INTC4	INTC5	INTC6	INTC7	INTC8	INTC9
ELISEL6	INTP0	INTTM00	INTTM06	INTST2/ INTCSI20/ INTIIC20	INTSR1/ INTCSI11/ INTIIC11	INTSMSE
ELISEL7	INTP1	INTTM01	INTITL	INTSR2/ INTCSI21/ INTIIC21	INTSRE1	INTP10
					INTTM03H	INTCMP0
ELISEL8	INTP2	INTTM02	INTWDTI	INTSRE2	INTREMC	INTP11
				INTTM11H		INTCMP1
ELISEL9	INTP3	INTTM03	INTRTC	INTST0/ INTCSI00/ INTIIC00	INTSR0/ INTCSI01/ INTIIC01	INTCTSUWR
ELISEL10	INTP4	INTTM04	INTTM07	INTSRE0	INTLVI	INTCTSURD
				INTTM01H		
ELISEL11	INTP5	INTTM05	INTIICA0	INTST1/ INTCSI10/ INTIIC10	INTAD	INTCTSUFN

Note 4. The interrupt sources that are selectable as event sources for INTC4 to INTC9 depend on which of the ELISELn (n = 6 to 11) registers is being set. Use the interrupt request signals as the hardware triggers for event-receiving peripheral functions.

Register	Event Source					
	INTC4	INTC5	INTC6	INTC7	INTC8	INTC9
ELISEL6	INTP0	INTTM00	INTTM06	INTST2/ INTCSI20/ INTIIC20	INTSR1/ INTCSI11/ INTIIC11	Setting prohibited
ELISEL7	INTP1	INTTM01	INTITL	INTSR2/ INTCSI21/ INTIIC21	INTSRE1	INTP10
					INTTM03H	INTCMP0
ELISEL8	INTP2	INTTM02	INTWDTI	INTSRE2	INTREMC	INTP11
				INTTM11H		INTCMP1
ELISEL9	INTP3	INTTM03	INTRTC	INTST0/ INTCSI00/ INTIIC00	INTSR0/ INTCSI01/ INTIIC01	INTCTSUWR
ELISEL10	INTP4	INTTM04	INTTM07	INTSRE0	INTLVI	INTCTSURD
				INTTM01H		
ELISEL11	INTP5	INTTM05	INTIICA0	INTST1/ INTCSI10/ INTIIC10	INTAD	INTCTSUFN

11. 20.6 Points for Caution when the ELCL is to be Used (Page 1081)

Incorrect:

4. The ELCL outputs signals with the use of multiple input signals, logic cell blocks, and output controllers. **Note that deviations in the timing between these elements may lead to the generation of glitches or expected outputs not being obtained.** If an expected output not being obtained may create serious problems for a user system, stop attempting to use the ELCL or employ an external circuit as a workaround.

Correct:

4. The ELCL outputs signals with the use of multiple input signals, logic cell blocks, and output controllers. The logic cell blocks L1, L2, and L3 produce outputs with some delay with respect to inputs. The output signals from the flip-flops are delayed by up to one cycle of the clock selected for synchronization of clock signals by the signal selection blocks 6 of event links L1 to L3. Furthermore, deviations in the timing of input signals may lead to the generation of glitches or expected outputs not being obtained. If an expected output not being obtained may create serious problems for a user system, stop attempting to use the ELCL or employ an external circuit as a workaround.

12. 29.3.3 Sequencer instruction registers p (SMSIp) (p = 0 to 31) (Page 1213, Page 1214)

Incorrect:

(Page 1213)

Table 29 - 1 Correspondences between the Memory Addresses of the SMSIp Registers and Values of the SMSCV0 to SMSCV4 Bits

SMSIp	Address	SMSCV[4:0]
SMSI15	F039EH, F039FH	01111B
SMSI14	F039CH, F039DH	01110B
SMSI13	F039AH, F039BH	01101B
SMSI12	F0398H, F0399H	01100B
SMSI11	F0396H, F0397H	01011B
SMSI10	F0394H, F0395H	01010B
SMSI9	F0392H, F0393H	01001B
SMSI8	F0390H, F0391H	01000B
SMSI7	F038EH, F038FH	00111B
SMSI6	F038CH, F038DH	00110B
SMSI5	F038AH, F038BH	00101B
SMSI4	F0388H, F0389H	00100B
SMSI3	F0386H, F0387H	00011B
SMSI2	F0384H, F0385H	00010B
SMSI1	F0382H, F0383H	00001B
SMSI0	F0380H, F0381H	00000B

SMSIp	Address	SMSCV[4:0]
SMSI31	F03BEH, F03BFH	11111B
SMSI30	F03BCH, F03BDH	11110B
SMSI29	F03BAH, F03BBH	11101B
SMSI28	F03B8H, F03B9H	11100B
SMSI27	F03B6H, F03B7H	11011B
SMSI26	F03B4H, F03B5H	11010B
SMSI25	F03B2H, F03B3H	11001B
SMSI24	F03B0H, F03B1H	11000B
SMSI23	F03AEH, F03AFH	10111B
SMSI22	F03ACH, F03ADH	10110B
SMSI21	F03AAH, F03ABH	10101B
SMSI20	F03A8H, F03A9H	10100B
SMSI19	F03A6H, F03A7H	10011B
SMSI18	F03A4H, F03A5H	10010B
SMSI17	F03A2H, F03A3H	10001B
SMSI16	F03A0H, F03A1H	10000B

Caution 1. Only set the SMSIp registers while the operation of the sequencer is stopped. Re-writing the SMSIp registers while the sequencer is handling the commands results in an undefined operation of the sequencer.

Caution 2. No register follows the SMSI31 register once the processing it defines has finished. **Therefore, set the SMSI31 register for processing for termination command or interrupt plus termination command to stop processing by the sequencer, or for branch processing so that the processing at the branch destination register is run.**

Correct:

Table 29 - 1 Correspondences between the Memory Addresses of the SMSIp Registers and Values of the SMSCV0 to SMSCV4 Bits

SMSIp	Address	SMSCV[4:0]
SMSI15	F039EH, F039FH	01111B
SMSI14	F039CH, F039DH	01110B
SMSI13	F039AH, F039BH	01101B
SMSI12	F0398H, F0399H	01100B
SMSI11	F0396H, F0397H	01011B
SMSI10	F0394H, F0395H	01010B
SMSI9	F0392H, F0393H	01001B
SMSI8	F0390H, F0391H	01000B
SMSI7	F038EH, F038FH	00111B
SMSI6	F038CH, F038DH	00110B
SMSI5	F038AH, F038BH	00101B
SMSI4	F0388H, F0389H	00100B
SMSI3	F0386H, F0387H	00011B
SMSI2	F0384H, F0385H	00010B
SMSI1	F0382H, F0383H	00001B
SMSI0	F0380H, F0381H	00000B

SMSIp	Address	SMSCV[4:0]
SMSI31	F03BEH, F03BFH	11111B
SMSI30	F03BCH, F03BDH	11110B
SMSI29	F03BAH, F03BBH	11101B
SMSI28	F03B8H, F03B9H	11100B
SMSI27	F03B6H, F03B7H	11011B
SMSI26	F03B4H, F03B5H	11010B
SMSI25	F03B2H, F03B3H	11001B
SMSI24	F03B0H, F03B1H	11000B
SMSI23	F03AEH, F03AFH	10111B
SMSI22	F03ACH, F03ADH	10110B
SMSI21	F03AAH, F03ABH	10101B
SMSI20	F03A8H, F03A9H	10100B
SMSI19	F03A6H, F03A7H	10011B
SMSI18	F03A4H, F03A5H	10010B
SMSI17	F03A2H, F03A3H	10001B
SMSI16	F03A0H, F03A1H	10000B

Caution 1. Only set the SMSIp registers while the operation of the sequencer is stopped. Re-writing the SMSIp registers while the sequencer is handling the commands results in an undefined operation of the sequencer.

Caution 2. No register follows the SMSI31 register once the processing it defines has finished. If the command for terminating processing of commands or branch processing is not set in the SMSI31 register, the processing for termination is automatically executed once the processing defined in the SMSI31 register has finished.

(Page 1214)

Table 29 - 2 Types of Processing Specified by the SMSIp Registers

Name of Processing	Operation[Note 4]	Sequencer Code	First Operand (4 Bits)	Second Operand (4 Bits)	Additional Byte (4 Bits)
8-bit data transfer 1	[SMSGn + Byte] ← SMSGm	0000	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	Byte[Note 2]
8-bit data transfer 2	SMSGm ← [SMSGn + Byte]	0001	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	Byte[Note 2]
16-bit data transfer 1	[SMSGn + Byte] ← SMSGm	0010	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	Byte[Note 2]
16-bit data transfer2	SMSGm ← [SMSGn + Byte]	0011	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	Byte[Note 2]
1-bit data setting	[SMSGn + Byte].bit ← 1	0100	nth of SMSGn [Note 1]	bit[Note 2]	Byte[Note 2]
1-bit data clearing	[SMSGn + Byte].bit ← 0	0101	nth of SMSGn [Note 1]	bit[Note 2]	Byte[Note 2]
1-bit data transfer	SCY ← [SMSGn + Byte].bit	0110	nth of SMSGn [Note 1]	bit[Note 2]	Byte[Note 2]
Word addition	SMSGn, SCY ← SMSGn + SMSGm	0111	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	0000
Word subtraction	SMSGn, SCY ← SMSGn - SMSGm	0111	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	0001
Word comparison	SMSGn - SMSGm	0111	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	0010
Logical shift right	SCY ← SMSGn.0, SMSGm.15 ← 0, SMSGn.m-1 ← SMSGn.m	0111	nth of SMSGn [Note 1]	0000	0011
Branch 1 (SCY = 1)	SMSS[4:0] ← SMSS[4:0] + jdisp8 if SCY = 1	1000	$addr5[Note 3]		0000
Branch 2 (SCY = 0)	SMSS[4:0] ← SMSS[4:0] + jdisp8 if SCY = 0	1000	$addr5[Note 3]		0001
Branch 3 (SZ = 1)	SMSS[4:0] ← SMSS[4:0] + jdisp8 if SZ = 1	1000	$addr5[Note 3]		0010
Branch 4 (SZ = 0)	SMSS[4:0] ← SMSS[4:0] + jdisp8 if SZ = 0	1000	$addr5[Note 3]		0011
Wait	Holding processing pending for a certain period	1001	IM1		IM2
Conditional wait 1 (bit = 1)	SMSS[4:0] ← SMSS[4:0] if [SMSGn + Byte].bit = 1	1010	nth of SMSGn [Note 1]	Bit[Note 2]	Byte[Note 2]
Conditional wait 2 (bit = 0)	SMSS[4:0] ← SMSS[4:0] if [SMSGn + Byte].bit = 0	1011	nth of SMSGn [Note 1]	Bit[Note 2]	Byte[Note 2]
Termination	SMSS[4:0] ← 0, Stopping the sequencer	1111	0000	0000	0000
~~Interrupt plus termination~~	~~SMSS[4:0] ← 0, Stopping the sequencer after issuing an interrupt~~	~~1111~~	~~0000~~	~~0000~~	~~0001~~
DTC activation	Output of a DTC activating source signal	1111	0000	0000	0010

Note 1. Specify values in the range from 0 to 15 (from 0000B to 1111B) for n and m.

Note 2. Specify values in the range from 0 to 7 (from 0000B to 0111B) for the bytes.

Note 3. This is an 8-bit displacement value. Specify a relative address in the ranges from -31 to -1 and 1 to 31 (0000 0001B to 0001 1111B, 1111 1111B to 1110 0001B).

Note 4. For details on the terms, see 29.5 Commands for Use in Processing by the Sequencer.

Table 29 - 2 Types of Processing Specified by the SMSIp Registers

Name of Processing	Operation[Note 4]	Sequencer Code	First Operand (4 Bits)	Second Operand (4 Bits)	Additional Byte (4 Bits)
8-bit data transfer 1	[SMSGn + Byte] ← SMSGm	0000	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	Byte[Note 2]
8-bit data transfer 2	SMSGm ← [SMSGn + Byte]	0001	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	Byte[Note 2]
16-bit data transfer 1	[SMSGn + Byte] ← SMSGm	0010	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	Byte[Note 2]
16-bit data transfer2	SMSGm ← [SMSGn + Byte]	0011	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	Byte[Note 2]
1-bit data setting	[SMSGn + Byte].bit ← 1	0100	nth of SMSGn [Note 1]	bit[Note 2]	Byte[Note 2]
1-bit data clearing	[SMSGn + Byte].bit ← 0	0101	nth of SMSGn [Note 1]	bit[Note 2]	Byte[Note 2]
1-bit data transfer	SCY ← [SMSGn + Byte].bit	0110	nth of SMSGn [Note 1]	bit[Note 2]	Byte[Note 2]
Word addition	SMSGn, SCY ← SMSGn + SMSGm	0111	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	0000
Word subtraction	SMSGn, SCY ← SMSGn - SMSGm	0111	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	0001
Word comparison	SMSGn - SMSGm	0111	nth of SMSGn [Note 1]	mth of SMSGm[Note 1]	0010
Logical shift right	SCY ← SMSGn.0, SMSGm.15 ← 0, SMSGn.m-1 ← SMSGn.m	0111	nth of SMSGn [Note 1]	0000	0011
Branch 1 (SCY = 1)	SMSS[4:0] ← SMSS[4:0] + jdisp8 if SCY = 1	1000	$addr5[Note 3]		0000
Branch 2 (SCY = 0)	SMSS[4:0] ← SMSS[4:0] + jdisp8 if SCY = 0	1000	$addr5[Note 3]		0001
Branch 3 (SZ = 1)	SMSS[4:0] ← SMSS[4:0] + jdisp8 if SZ = 1	1000	$addr5[Note 3]		0010
Branch 4 (SZ = 0)	SMSS[4:0] ← SMSS[4:0] + jdisp8 if SZ = 0	1000	$addr5[Note 3]		0011
Wait	Holding processing pending for a certain period	1001	IM1		IM2
Conditional wait 1 (bit = 1)	SMSS[4:0] ← SMSS[4:0] if [SMSGn + Byte].bit = 1	1010	nth of SMSGn [Note 1]	Bit[Note 2]	Byte[Note 2]
Conditional wait 2 (bit = 0)	SMSS[4:0] ← SMSS[4:0] if [SMSGn + Byte].bit = 0	1011	nth of SMSGn [Note 1]	Bit[Note 2]	Byte[Note 2]
Termination	SMSS[4:0] ← 0, Stopping the sequencer	1111	0000	0000	0000
DTC activation	Output of a DTC activating source signal	1111	0000	0000	0010

Note 1. Specify values in the range from 0 to 15 (from 0000B to 1111B) for n and m.

Note 2. Specify values in the range from 0 to 7 (from 0000B to 0111B) for the bytes.

Note 3. This is an 8-bit displacement value. Specify a relative address in the ranges from -31 to -1 and 1 to 31 (0000 0001B to 0001 1111B, 1111 1111B to 1110 0001B).

Note 4. For details on the terms, see 29.5 Commands for Use in Processing by the Sequencer.

13. 29.4 Operations of the SNOOZE Mode Sequencer (Page 1223)

Incorrect:

29.4.3 Sequencer flags

The sequencer has flags that are set or reset in response to the results of operations.

a) Sequencer zero flag (SZ)
The SZ flag is an internal flag of the sequencer. The flag is set to 1 when the result of addition, subtraction, or comparison is 0. Otherwise, the flag is cleared to 0. The flag is only for use in the internal processing by the sequencer. For details, see 29.5 Commands for Use in Processing by the Sequencer.

b) Sequencer carry flag (SCY)
The SCY flag reflects the state of addition or subtraction producing an overflow or underflow, the value of the shifted-out bit in logical shifting processing, or the result of 1-bit data transfer. The flag is only for use in the internal processing by the sequencer. For details, see 29.5 Commands for Use in Processing by the Sequencer.

The values of the SZ and SCY flags of the sequencer can be read from the corresponding bits of the SMSS register. See 29.3.6 Sequencer status register (SMSS).

Correct:

29.4.3 Sequencer flags

The sequencer has flags that are set or reset in response to the results of operations.

a) Sequencer zero flag (SZ)
The SZ flag is an internal flag of the sequencer. The flag is set to 1 when the result of addition, subtraction, or comparison is 0. Otherwise, the flag is cleared to 0. The flag is only for use in the internal processing by the sequencer. For details, see 29.5 Commands for Use in Processing by the Sequencer.

b) Sequencer carry flag (SCY)
The SCY flag reflects the state of addition or subtraction producing an overflow or underflow, the value of the shifted-out bit in logical shifting processing, or the result of 1-bit data transfer. The flag is only for use in the internal processing by the sequencer. For details, see 29.5 Commands for Use in Processing by the Sequencer.

The values of the SZ and SCY flags of the sequencer can be read from the corresponding bits of the SMSS register. See 29.3.6 Sequencer status register (SMSS).

29.4.4 Interrupt from the SNOOZE Mode Sequencer

The SMSEMK bit controls generation of the INTSMSE interrupt from the SNOOZE mode sequencer. Before starting the SNOOZE mode sequencer operation (by setting SMSSTART to 1), use the CPU to set the SMSEMK and SMSEIF bits to 1. The SMSEIF and SMSEMK bits are respectively set to 1 and 0 by setting the SMSEMK bit to 0 within the SNOOZE mode sequencer processing, which leads to generation of the INTSMSE interrupt. When the interrupt is disabled (DI), the SMSEMK bit being 0 indicates the end of the sequencer operation.

Caution 1. Do not use a CPU instruction to set the SMSEMK bit in the MK0H register or SMSEIF bit in the IF0H register to 0 while the setting of the SMSSTART bit in the SMSC register is 1.

Caution 2. If processing by the SNOOZE mode sequencer and that for the INTSMSE interrupt involve access to the same area in the SFR or RAM, ensure that the two types of processing do not run at the same time.

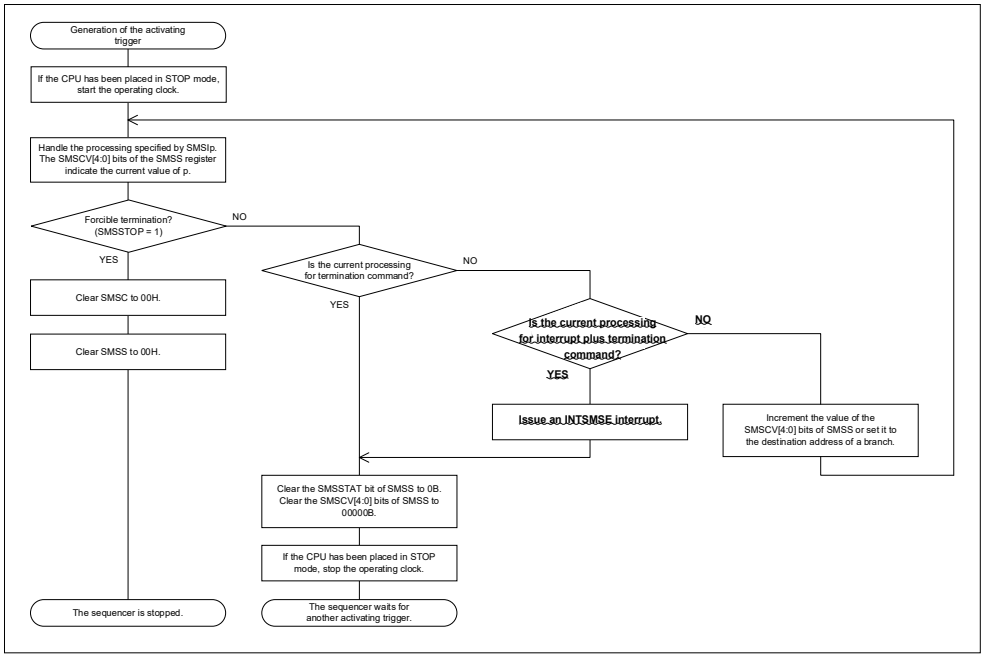
14. 29.4.1 Internal operations of the SNOOZE mode sequencer (Page 1220)

Incorrect:

29.4.1 Internal operations of the SNOOZE mode sequencer

Sequencing by the SNOOZE mode sequencer starts in response to the activating trigger specified by the SMSTRGSEL0 to SMSTRGSEL4 bits of the SMSC register. Following activation, the sequencer handles the processing specified by the SMSI0 register, and then handles the processing specified by the SMSIp register indicated by the SMSCV0 to SMSCV4 bits of the SMSS register. After execution of the processing for termination command **or interrupt plus termination command,** the sequencer has finished one round of processing and waits for another activating trigger. Moreover, setting the SMSSTOP bit of the SMSC register to 1 to generate a trigger for forcible termination leads to the sequencer being stopped. Figure 29 - 8 shows the flow of internal operations of the SNOOZE mode sequencer.

Figure 29 - 8 Flow of Internal Operations of the SNOOZE Mode Sequencer

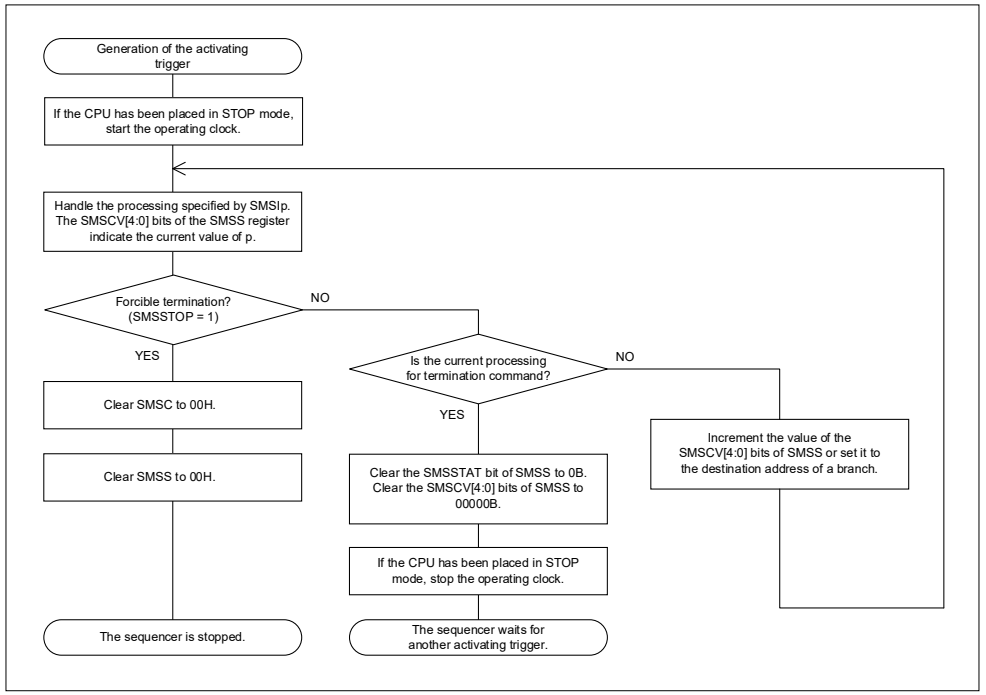


Correct:

29.4.1 Internal operations of the SNOOZE mode sequencer

Sequencing by the SNOOZE mode sequencer starts in response to the activating trigger specified by the SMSTRGSEL0 to SMSTRGSEL4 bits of the SMSC register. Following activation, the sequencer handles the processing specified by the SMSI0 register, and then handles the processing specified by the SMSIp register indicated by the SMSCV0 to SMSCV4 bits of the SMSS register. After execution of the processing for termination command, the sequencer has finished one round of processing and waits for another activating trigger. Moreover, setting the SMSSTOP bit of the SMSC register to 1 to generate a trigger for forcible termination leads to the sequencer being stopped. Figure 29 - 8 shows the flow of internal operations of the SNOOZE mode sequencer.

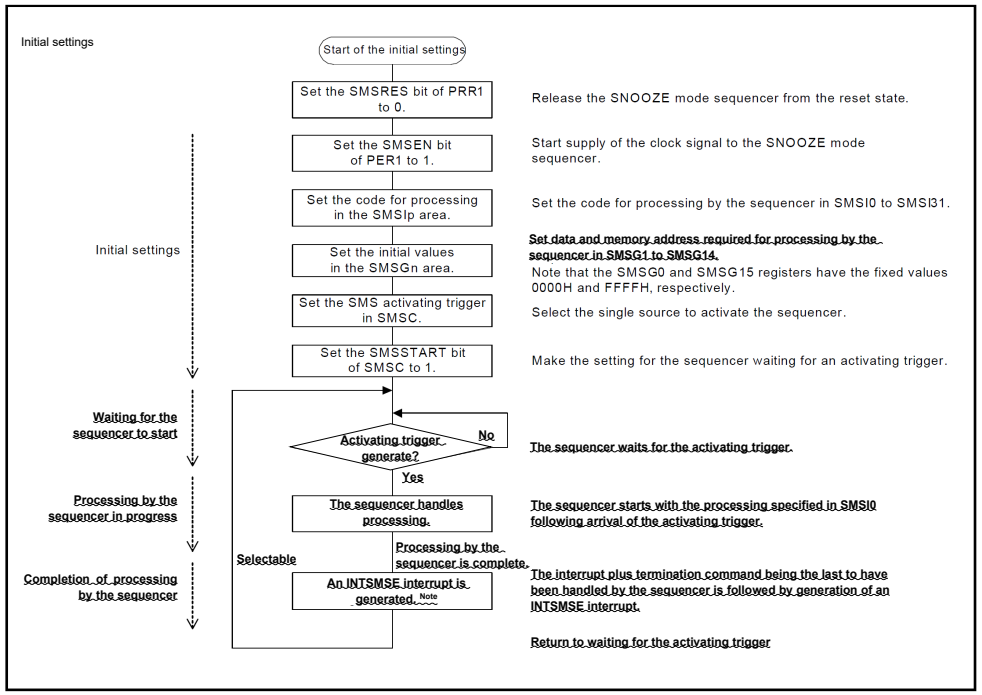
Figure 29 - 8 Flow of Internal Operations of the SNOOZE Mode Sequencer



15. 29.4.4 Procedures for running the SNOOZE mode sequencer (Page 1224)

Incorrect:

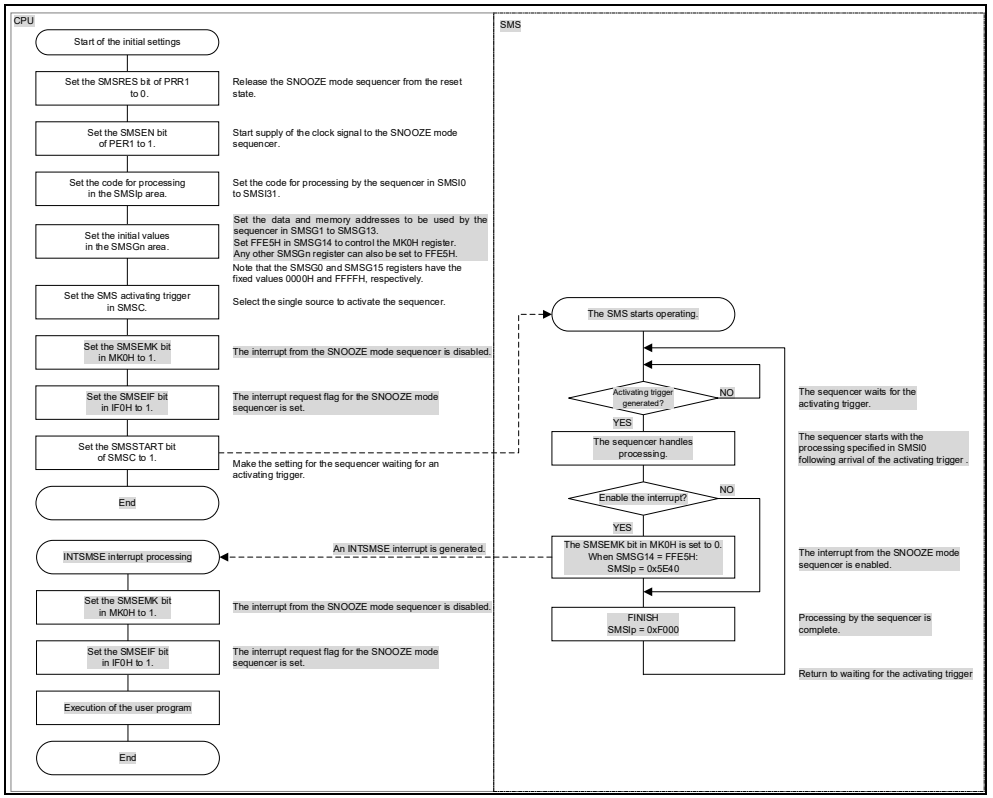
Figure 29 - 11 Flow of Activating and Running the SNOOZE Mode Sequencer



Note If processing by the sequencer ends following the processing for termination command or setting of the trigger bit for forcible termination (the SMSSTOP bit in the SMSC register), an INTSMSE interrupt will not be generated. If processing by the sequencer ends for the latter reason (setting of the trigger bit for forcible termination), the SMSC register itself will be initialized. Therefore, to restart processing by the sequencer, make the initial settings of the SMSC register again (the SMSIp and SMSGn registers are not reset).

Correct:

Figure 29 - 11 Flow of Activating and Running the SNOOZE Mode Sequencer



Caution 1. If processing by the sequencer ends for the latter reason (setting of the trigger bit for forcible termination), the SMSC register itself will be initialized. Therefore, to restart processing by the sequencer, make the initial settings of the SMSC register again (the SMSIp and SMSGn registers are not reset).

Caution 2. Do not use a CPU instruction to set the SMSEMK bit in the MK0H register or SMSEIF bit in the IF0H register to 0 while the setting of the SMSSTART bit in the SMSC register is 1.

16. 29.4.5 States of the SNOOZE mode sequencer (Page 1226)

Incorrect:

Sequencer operating state

The sequencer operating state is that in which the sequencer is operating and is handling processing specified by the SMSIp registers. Executing the termination **or interrupt plus termination** command places the sequencer in the activating trigger waiting state. If operation of the sequencer is forcibly terminated by setting the SMSSTOP bit of the SMSC register to 1, the sequencer enters the sequencer stopped state.

Correct:

Sequencer operating state

The sequencer operating state is that in which the sequencer is operating and is handling processing specified by the SMSIp registers. Executing the termination command places the sequencer in the activating trigger waiting state. If operation of the sequencer is forcibly terminated by setting the SMSSTOP bit of the SMSC register to 1, the sequencer enters the sequencer stopped state.

17. 29.5.20 Interrupt plus termination (Page 1248)

Incorrect:

29.5.20 Interrupt plus termination

The interrupt plus termination command issues an interrupt signal and then stops the SNOOZE mode sequencer. Issuing the interrupt signal enables starting the CPU when it has been placed on standby. Specifically, execution of the command issues the interrupt signal, stops the SNOOZE mode sequencer, clears the SMSSTAT and SMSCV[4:0] bits in the SMSS register to 0, and places the sequencer in the activating trigger waiting state. Set the additional byte to 0001B. Set all bits of the first and second operands to 0.

Sequencer code: 1111B (additional byte: 0001B)
Number of clock cycles for processing: 1 cycle of fCLK
Flags: The states of the SZ and SCY flags are retained.
Equivalent CPU command: WAKEUP
Equivalent CPU operation: SMSS[4:0] ← 0, stopping the sequencer after issuing an interrupt

Symbol	15	14	13	12	11	10	9	8
SMSIp	1	1	1	1	0	0	0	0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1

Example of a statement: 1111 0000 0000 0001 B
The equivalent CPU command in this case is WAKEUP. The interrupt plus termination command stops the sequencer after issuing an INTSMSE interrupt, clears the SMSSTAT and SMSCV[4:0] bits of the SMSS register to 0, and places the sequencer in the activating trigger waiting state.

Correct:

18. 29.6 Operation in Standby Modes (Page 1250)

Incorrect:

29.6 Operation in Standby Modes

State	Operation of the SNOOZE Mode Sequencer
HALT mode	Operation continues.Note 1
STOP mode	The activating trigger for the SNOOZE mode sequencer can be accepted.Note 3
SNOOZE mode	Operation continues.Notes 2, 4, 5, 6

Note 1. When the subsystem clock is selected as f_{CLK}, operation is disabled if the RTCLPC bit of the OSMC register is 1.

Note 2. The SNOOZE mode can only be set when the high-speed on-chip oscillator clock or middle-speed on-chip oscillator clock is selected as f_{CLK}.

Note 3. Detection of an SMS activating trigger in STOP mode places the chip in SNOOZE mode, making the SNOOZE mode sequencer capable of operation. The state of the chip returns to the STOP mode after the operations of the SMS are completed. Note that the sequencer does not have access to certain memory areas in SNOOZE mode. For details, see 29.4.2 Memory space allocated to the sequencer.

Note 4. **When a transfer end interrupt from the CSIp in SNOOZE mode is being used as the activating trigger for the SNOOZE mode sequencer, use the interrupt plus termination command to release the chip from the SNOOZE mode and start processing by the CPU, or make the settings for reception by the CSIp (writing 1 to the STm0 bit, writing 0 to the SWCm bit, setting the SSCm register, and writing 1 to the SSm0 bit) again before the processing for termination.**

Note 5. **When a transfer end interrupt from the UARTq in SNOOZE mode is being used as the activating trigger for the SNOOZE mode sequencer, use the interrupt plus termination command to release the chip from the SNOOZE mode and start processing by the CPU, or make the settings for reception by the UARTq (writing 1 to the STm1 bit, writing 0 to the SWCm bit, setting the SSCm register, and writing 1 to the SSm1 bit) again before the processing for termination.**

Note 6. **When an A/D conversion end interrupt from the A/D converter in SNOOZE mode is being used as the activating trigger for the SNOOZE mode sequencer, use the interrupt plus termination command to release the chip from the SNOOZE mode and start processing by the CPU, or make the settings for the SNOOZE mode function of the A/D converter (writing 1 to the AWC bit after having written 0 to it) again before the processing for termination.**

Correct:

29.6 Operation in Standby Modes

State	Operation of the SNOOZE Mode Sequencer
HALT mode	Operation continues.Note 1
STOP mode	The activating trigger for the SNOOZE mode sequencer can be accepted.Note 3
SNOOZE mode	Operation continues.Notes 2, 4, 5, 6

Note 1. When the subsystem clock is selected as f_{CLK}, operation is disabled if the RTCLPC bit of the OSMC register is 1.

Note 2. The SNOOZE mode can only be set when the high-speed on-chip oscillator clock or middle-speed on-chip oscillator clock is selected as f_{CLK}.

Note 3. Detection of an SMS activating trigger in STOP mode places the chip in SNOOZE mode, making the SNOOZE mode sequencer capable of operation. The state of the chip returns to the STOP mode after the operations of the SMS are completed. Note that the sequencer does not have access to certain memory areas in SNOOZE mode. For details, see 29.4.2 Memory space allocated to the sequencer.

Note 4. When a transfer end interrupt from CSI00 is being used as the activating trigger for the SNOOZE mode sequencer but the transfer end interrupt is disabled (CSIMK = 1), proceed with the following steps before the processing for termination of the SNOOZE mode sequencer. Write 0 to the SMSEMK bit in the MK0H register, and release the chip from the SNOOZE mode to start processing by the CPU, or make the settings for reception by CSI00 (writing 1 to the ST00 bit, writing 0 to the SWC0 bit, setting the SSC0 register, and writing 1 to the SS00 bit) again.

Note 5. When a transfer end interrupt from UART0 is being used as the activating trigger for the SNOOZE mode sequencer, but the transfer end interrupt is disabled (SRMK0 = 1), proceed with the following steps before the processing for termination of the SNOOZE mode sequencer. Write 0 to the SMSEMK bit in the MK0H register, and release the chip from the SNOOZE mode to start processing by the CPU, or make the settings for reception by UART0 (writing 1 to the ST01 bit, writing 0 to the SWC0 bit, setting the SSC0 register, and writing 1 to the SS01 bit) again.

Note 6. When an A/D conversion end interrupt from the A/D converter is being used as the activating trigger for the SNOOZE mode sequencer, but the A/D conversion end interrupt is disabled (ADMK = 1), proceed with the following steps before the processing for termination of the SNOOZE mode sequencer. Write 0 to the SMSEMK bit in the MK0H register, and release the chip from the SNOOZE mode to start processing by the CPU, or make the settings for the SNOOZE mode of the A/D converter (writing 1 to the AWC bit after having written 0 to it) again.

19. 37.4 AC Characteristics (Page 1431)

Incorrect:

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	μs
			LP (low-power main) mode	1.6 V ≤ V_{DD} ≤ 5.5 V	0.5		1	μs
		Subsystem clock (f_{SUB}) operation		1.6 V ≤ V_{DD} ≤ 5.5 V	26.041	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.5		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.5		1	μs
External system clock frequency	f_{EX}	1.8 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		1.6 V ≤ V_{DD} < 1.8 V			1.0		4.0	MHz
	f_{EXS}				32		38.4	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	1.8 V ≤ V_{DD} ≤ 5.5 V			~~15~~			ns
		1.6 V ≤ V_{DD} < 1.8 V			120			ns
	t_{EXHS}, t_{EXLS}				13.7			μs

Correct:

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	μs
			LP (low-power main) mode	1.6 V ≤ V_{DD} ≤ 5.5 V	0.5		1	μs
		Subsystem clock (f_{SUB}) operation		1.6 V ≤ V_{DD} ≤ 5.5 V	26.041	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.5		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.5		1	μs
External system clock frequency	f_{EX}	1.8 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		1.6 V ≤ V_{DD} < 1.8 V			1.0		4.0	MHz
	f_{EXS}				32		38.4	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	1.8 V ≤ V_{DD} ≤ 5.5 V			24			ns
		1.6 V ≤ V_{DD} < 1.8 V			120			ns
	t_{EXHS}, t_{EXLS}				13.7			μs