

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A001B/E	Rev.	2.00
Title	Correction for Incorrect Description Notice RL78/G13 Descriptions in the Hardware User's Manual Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G13 Group R5F100xxx, R5F101xxx	Lot No.	Reference Document	RL78/G13 User's Manual: Hardware Rev. 1.00 R01UH0146EJ0100 (Sep. 2011)		
		All lot				

This document describes misstatements found in the RL78 hardware user's manual Rev. 1.00 (R01UH0146EJ0100).

Corrections

Applicable Page	Applicable Item	Contents
Pages 493, 496, 523, 530	Explanations when using temperature sensor and internal reference voltage (1.45 V) of A/D converter added	Explanations added
Pages 917 to 919	Explanations when using temperature sensor and internal reference voltage (1.45 V) of A/D test function in Safety functions chapter added	Explanations added
Pages 1032 to 1035	Conditions of A/D converter characteristics in Electrical specifications chapter (section 29.7.1) added	Conditions added
Page 1036	Condition of Temperature sensor characteristics in Electrical specifications chapter (section 29.7.2) added	Condition added

Incorrect: Bold with underline; Correct: Gray hatched

Document Improvement

The above corrections will be made for the next revision of the hardware user's manual around February, 2012. Contact a Renesas Electronics sales department details on the publishing schedule.

Corrections in the hardware user's manual

No.	Applicable Item		Rev 1.00	After Rev 2.00 ^{Note}
	Document No.	Japanese	R01UH0146JJ0100	R01UH0146JJ0200
		English	R01UH0146EJ0100	R01UH0146EJ0200
1	Incorrect descriptions of 64-pin plastic TQFP (7 x 7) deleted		-	✓
2	Incorrect descriptions of count registers, in real-time clock deleted		-	✓
3	Explanations of interval timer control register (ITMC) added		-	✓
4	Explanations of timing chart when A/D voltage comparator is used added		-	✓
5	Incorrect descriptions of A/D conversion time selection, there is stabilization wait time (6/8) to (8/8) revised		-	✓
6	Explanations when entering A/D converter standby mode added		-	✓
7	Incorrect descriptions of maskable interrupt request acknowledgment operation		-	✓
8	Incorrect descriptions of voltage detector (LVD) timing chart revised		-	✓
9	Incorrect descriptions of voltage detector (LVD) interrupt and reset mode revised		-	✓
10	Number (4) of Supply current characteristics in Electrical specifications chapter (section 29.4.2) is the same for all RL78/G13 Group products.		-	✓
11	Explanations when using temperature sensor and internal reference voltage (1.45 V) of A/D converter added		-	✓
12	Explanations when using temperature sensor and internal reference voltage (1.45 V) of A/D test function in Safety functions chapter added		-	✓
13	Conditions of A/D converter characteristics in Electrical specifications chapter (section 29.7.1) added		-	✓
14	Condition of Temperature sensor characteristics in Electrical specifications chapter (section 29.7.2) added		-	✓

Note A revised hardware user's manual is scheduled to be released around February, 2012.

Remarks ✓: Corrected

-: Items should be corrected

1. Descriptions of related information according to discontinued development of 64-pin plastic TQFP (7 x 7) package deleted

Order information of 64-pin plastic TQFP (7 x 7) deleted (page 4)

Incorrect:

(2/3)

Pin count	Package	Data flash	Part Number
(Omitted)			
64 pins	64-pin plastic LQFP (12x12)	Mounted	R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAF A, R5F100LHAF A, R5F100LJAF A, R5F100LKAF A, R5F100LLAF A
		Not mounted	R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAF A, R5F101LHAF A, R5F101LJAF A, R5F101LKAF A, R5F101LLAF A
	64-pin plastic LQFP (fine pitch) (10 × 10)	Mounted	R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAF B, R5F100LHAF B, R5F100LJAF B, R5F100LKAF B, R5F100LLAF B
		Not mounted	R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAF B, R5F101LHAF B, R5F101LJAF B, R5F101LKAF B, R5F101LLAF B
	64-pin plastic TQFP (fine pitch) (7 × 7)	Mounted	R5F100LCAFC, R5F100LDAFC, R5F100LEAFC, R5F100LFAFC, R5F100LGAF C, R5F100LHAF C, R5F100LJAF C
		Not mounted	R5F101LCAFC, R5F101LDAFC, R5F101LEAFC, R5F101LFAFC, R5F101LGAF C, R5F101LHAF C, R5F101LJAF C
	64-pin plastic FBGA (4 × 4)	Mounted	R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG, R5F100LJABG
		Not mounted	R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG, R5F101LJABG

Correct:

(2/3)

Pin count	Package	Data flash	Part Number
(Omitted)			
64 pins	64-pin plastic LQFP (12x12)	Mounted	R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAF A, R5F100LKAF A, R5F100LLAFA
		Not mounted	R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAF A, R5F101LKAF A, R5F101LLAFA
	64-pin plastic LQFP (fine pitch) (10 × 10)	Mounted	R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB, R5F100LKAFB, R5F100LLAFB
		Not mounted	R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB, R5F101LJAFB, R5F101LKAFB, R5F101LLAFB
	64-pin plastic FBGA (4 × 4)	Mounted	R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG, R5F100LJABG
		Not mounted	R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG, R5F101LJABG

Pin configuration of 64-pin plastic TQFP (7 x 7) deleted (page 17)

Incorrect:

1.3.11 64-pin products

- 64-pin plastic LQFP (12 × 12)
- 64-pin plastic LQFP (fine pitch) (10 × 10)
- ~~64-pin plastic TQFP (fine pitch) (7 × 7)~~

(Omitted)

Correct:

1.3.11 64-pin products

- 64-pin plastic LQFP (12 × 12)
- 64-pin plastic LQFP (fine pitch) (10 × 10)

(Omitted)

Package drawings of 64-pin plastic TQFP (7 x 7) deleted (page 1055)

Incorrect:

~~R5F100LCAFC, R5F100LDAFC, R5F100LEAFC, R5F100LFAFC, R5F100LGAFC, R5F100LHAFC, R5F100LJAF~~
~~R5F101LCAFC, R5F101LDAFC, R5F101LEAFC, R5F101LFAFC, R5F101LGAFC, R5F101LHAFC, R5F101LJAF~~

64-PIN PLASTIC TQFP (7x7) Under development
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Correct: Applicable page deleted

2. Incorrect descriptions of count registers in real-time clock deleted

Incorrect description of second count register (SEC) in real-time clock deleted (page 439)

Incorrect:

(5) Second count register (SEC)

The SEC register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of seconds. It counts up when the sub-count register overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 59 to this register in BCD code. ~~If a value outside the range is set, the register value returns to the normal value after 1 period.~~

The SEC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Correct:

(5) Second count register (SEC)

The SEC register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of seconds.

It counts up when the sub-count register overflows. When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 59 to this register in BCD code.

The SEC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Incorrect description of minute count register (MIN) in real-time clock deleted (page 439)

Incorrect:

(6) Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes.

It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the second count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 59 to this register in BCD code. ~~If a value outside the range is set, the register value returns to the normal value after 1 period.~~

The MIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Correct:

(6) Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes.

It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the second count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 59 to this register in BCD code.

The MIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Incorrect description of hour count register (HOUR) in real-time clock deleted (page 440)

Incorrect:

(7) Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12 and 21 to 32 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the minute count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time clock control register 0 (RTCC0). If the AMPM bit value is changed, the values of the HOUR register change according to the specified time system. ~~If a value outside the range is set, the register value returns to the normal value after 1 period.~~

The HOUR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

Correct:

(7) Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12 and 21 to 32 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the minute count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time clock control register 0 (RTCC0). If the AMPM bit value is changed, the values of the HOUR register change according to the specified time system.

The HOUR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

Incorrect description of day count register (DAY) in real-time clock deleted (page 442)

Incorrect:

(8) Day count register (DAY)

The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days.

It counts up when the hour counter overflows.

This counter counts as follows.

(Omitted)

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the hour count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 31 to this register in BCD code. ~~If a value outside the range is set, the register value returns to the normal value after 1 period.~~

The DAY register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Correct:

(8) Day count register (DAY)

The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days.

It counts up when the hour counter overflows.

This counter counts as follows.

(Omitted)

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the hour count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 31 to this register in BCD code.

The DAY register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Incorrect description of week count register (WEEK) in real-time clock deleted (page 443)

Incorrect:

(9) Week count register (WEEK)

The WEEK register is an 8-bit register that takes a value of 0 to 6 (decimal) and indicates the count value of weekdays.

It counts up in synchronization with the day counter.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 06 to this register in BCD code. ~~If a value outside the range is set, the register value returns to the normal value after 1 period.~~

The WEEK register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Correct:

(9) Week count register (WEEK)

The WEEK register is an 8-bit register that takes a value of 0 to 6 (decimal) and indicates the count value of weekdays.

It counts up in synchronization with the day counter.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Set a decimal value of 00 to 06 to this register in BCD code.

The WEEK register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Incorrect description of month count register (MONTH) in real-time clock deleted (page 444)

Incorrect:

(10) Month count register (MONTH)

The MONTH register is an 8-bit register that takes a value of 1 to 12 (decimal) and indicates the count value of months. It counts up when the day counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the day count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 12 to this register in BCD code. ~~If a value outside the range is set, the register value returns to the normal value after 1 period.~~

The MONTH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Correct:

(10) Month count register (MONTH)

The MONTH register is an 8-bit register that takes a value of 1 to 12 (decimal) and indicates the count value of months. It counts up when the day counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the day count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 12 to this register in BCD code.

The MONTH register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 01H.

Incorrect description of year count register (YEAR) in real-time clock deleted (page 444)

Incorrect:

(11) Year count register (YEAR)

The YEAR register is an 8-bit register that takes a value of 0 to 99 (decimal) and indicates the count value of years.

It counts up when the month count register (MONTH) overflows.

Values 00, 04, 08, ..., 92, and 96 indicate a leap year.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the MONTH register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 99 to this register in BCD code. ~~If a value outside the range is set, the register value returns to the normal value after 1 period.~~

The YEAR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Correct:

(11) Year count register (YEAR)

The YEAR register is an 8-bit register that takes a value of 0 to 99 (decimal) and indicates the count value of years.

It counts up when the month count register (MONTH) overflows.

Values 00, 04, 08, ..., 92, and 96 indicate a leap year.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (f_{RTC}) later. Even if the MONTH register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 99 to this register in BCD code.

The YEAR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

3. Caution of interval timer control register (ITMC) in 12-bit interval timer added (page 460)

Incorrect:

(3) Interval timer control register (ITMC)

(Omitted)

- Cautions
1. Before changing the RINTE bit from 1 to 0, use the interrupt mask flag register to disable the INTIT interrupt servicing. When the operation starts (from 0 to 1) again, clear the ITIF flag, and then enable the interrupt servicing.
 2. The value read from the RINTE bit is applied one count clock cycle after setting the RINTE bit.
 3. Only change the setting of the ITCMP11 to ITCMP0 bits when RINTE = 0. However, it is possible to change the settings of the ITCMP11 to ITCMP0 bits at the same time as when changing RINTE from 0 to 1 or 1 to 0.

Correct:

(3) Interval timer control register (ITMC)

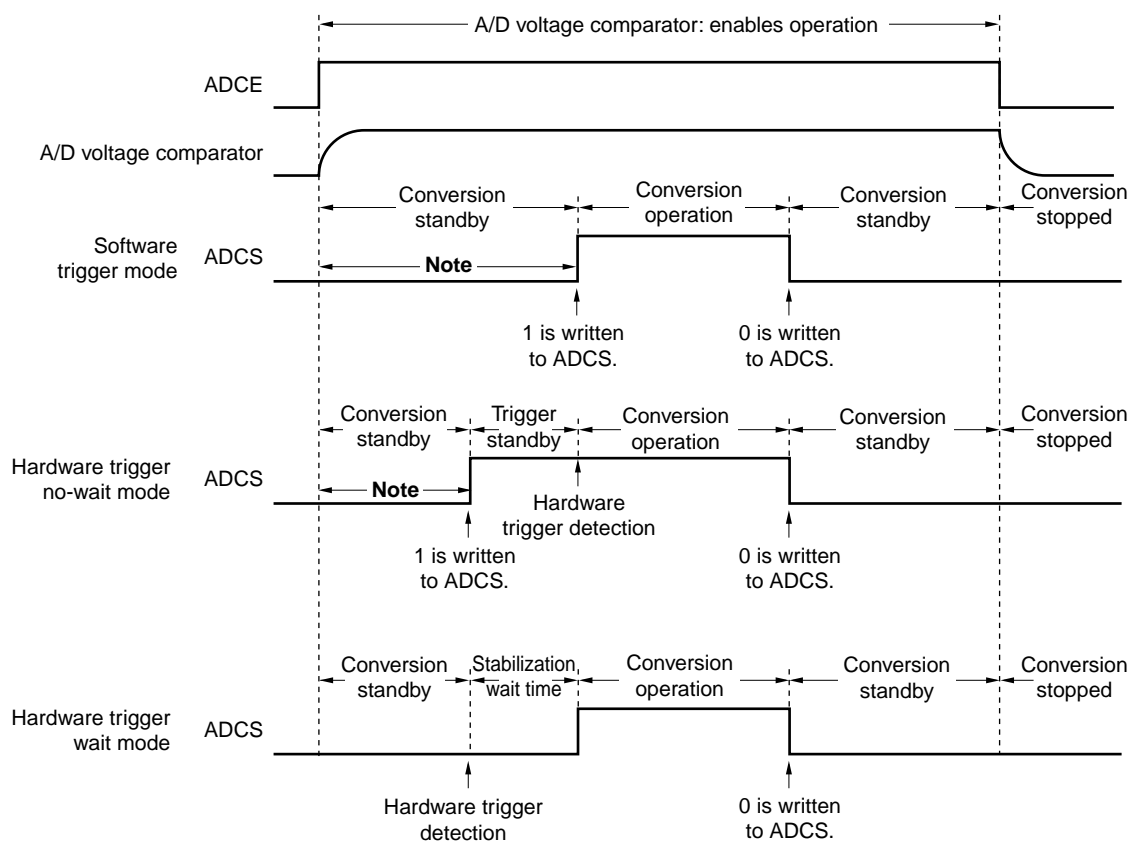
(Omitted)

- Cautions
1. Before changing the RINTE bit from 1 to 0, use the interrupt mask flag register to disable the INTIT interrupt servicing. When the operation starts (from 0 to 1) again, clear the ITIF flag, and then enable the interrupt servicing.
 2. The value read from the RINTE bit is applied one count clock cycle after setting the RINTE bit.
 3. When setting the RINTE bit after returned from standby mode and entering standby mode again, confirm that the written value of the RINTE bit is reflected, or wait that more than one clock of the count clock has elapsed after returned from standby mode. Then enter standby mode.
 4. Only change the setting of the ITCMP11 to ITCMP0 bits when RINTE = 0. However, it is possible to change the settings of the ITCMP11 to ITCMP0 bits at the same time as when changing RINTE from 0 to 1 or 1 to 0.

4. Added Explanations of timing chart when A/D voltage comparator is used (page 483)

Incorrect:

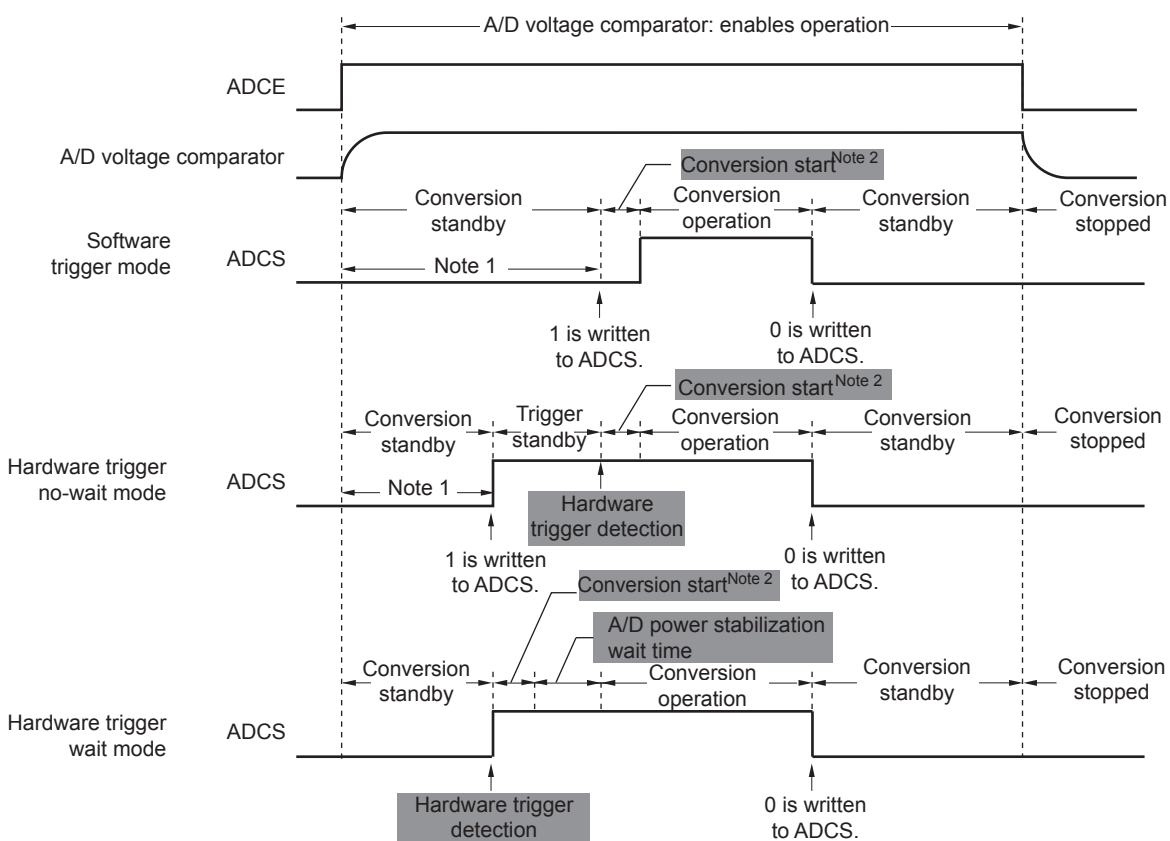
Figure 11-4. Timing Chart When A/D Voltage Comparator Is Used



Note (Omitted)

Correct:

Figure 11-4. Timing Chart When A/D Voltage Comparator Is Used



Note 1. (Omitted)

2. The following time is the maximum amount of time necessary to start conversion.

ADM0			Conversion Clock (f _{AD})	Conversion Start Time (Number of f _{CLK} Clocks)	
FR2	FR1	FR0		Software trigger mode/ Hardware trigger no wait mode	Hardware trigger wait mode
0	0	0	f _{CLK} /64	63	1
0	0	1	f _{CLK} /32	31	
0	1	0	f _{CLK} /16	15	
0	1	1	f _{CLK} /8	7	
1	0	0	f _{CLK} /6	5	
1	0	1	f _{CLK} /5	4	
1	1	0	f _{CLK} /4	3	
1	1	1	f _{CLK} /2	1	

Remark f_{CLK}: CPU/peripheral hardware clock frequency

5. Incorrect descriptions of Table 11-3 A/D Conversion Time Selection (6/8) to (8/8) when there is stabilization wait time (pages 489 to 491)

Incorrect:

Table 11-3. A/D Conversion Time Selection (6/8)

(6) $2.7\text{ V} \leq V_{DD} < 3.6\text{ V}$

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (f _{AD})			
FR2	FR1	FR0	LV1	LV0		f _{CLK} = 1 MHz	f _{CLK} = 2 MHz	f _{CLK} = 4 MHz	f _{CLK} = 8 MHz	f _{CLK} = 16 MHz	f _{CLK} = 32 MHz				
0	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	f _{CLK} /64			
0	0	1									54 μs	27 μs	f _{CLK} /32		
0	1	0									54 μs	27 μs	f _{CLK} /16		
0	1	1									54 μs	27 μs	f _{CLK} /8		
1	0	0									40.5 μs	20.25 μs	f _{CLK} /6		
1	0	1									33.75 μs	16.875 μs	f _{CLK} /5		
1	1	0									54 μs	27 μs	13.5 μs	6.75 μs	Setting prohibited
1	1	1	54 μs	27 μs	13.5 μs	6.75 μs	Setting prohibited	Setting prohibited	f _{CLK} /2						
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	f _{CLK} /64			
0	0	1									50 μs	25 μs	f _{CLK} /32		
0	1	0									50 μs	25 μs	f _{CLK} /16		
0	1	1									50 μs	25 μs	12.5 μs	6.25 μs	f _{CLK} /8
1	0	0									37.5 μs	18.75 μs	9.375 μs	4.6875 μs	f _{CLK} /6
1	0	1									31.25 μs	15.625 μs	7.8125 μs	f _{CLK} /5	
1	1	0									50 μs	25 μs	12.5 μs	6.25 μs	Setting prohibited
1	1	1	50 μs	25 μs	12.5 μs	6.25 μs	Setting prohibited	Setting prohibited	f _{CLK} /2						
0	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	f _{CLK} /64			
0	0	1									54 μs	27 μs	f _{CLK} /32		
0	1	0									54 μs	27 μs	f _{CLK} /16		
0	1	1									54 μs	27 μs	f _{CLK} /8		
1	0	0									40.5 μs	20.25 μs	f _{CLK} /6		
1	0	1									33.75 μs	16.875 μs	f _{CLK} /5		
1	1	0									54 μs	27 μs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	1	54 μs	27 μs	Setting prohibited	Setting prohibited	Setting prohibited	f _{CLK} /2							
0	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	f _{CLK} /64			
0	0	1									50 μs	25 μs	f _{CLK} /32		
0	1	0									50 μs	25 μs	f _{CLK} /16		
0	1	1									50 μs	25 μs	f _{CLK} /8		
1	0	0									37.5 μs	18.75 μs	f _{CLK} /6		
1	0	1									31.25 μs	15.625 μs	f _{CLK} /5		
1	1	0									50 μs	25 μs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	1	50 μs	25 μs	Setting prohibited	Setting prohibited	Setting prohibited	f _{CLK} /2							

Incorrect:

Table 11-3. A/D Conversion Time Selection (7/8)

(7) $1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (fAD)
FR2	FR1	FR0	LV1	LV0		fCLK = 1 MHz	fCLK = 2 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz (Note)	fCLK = 32 MHz	
0	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/64
0	0	1										fCLK/32
0	1	0										fCLK/16
0	1	1										fCLK/8
1	0	0										fCLK/6
1	0	1										fCLK/5
1	1	0										fCLK/4
1	1	1										fCLK/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/64
0	0	1										fCLK/32
0	1	0										fCLK/16
0	1	1										fCLK/8
1	0	0										fCLK/6
1	0	1										fCLK/5
1	1	0										fCLK/4
1	1	1										fCLK/2
0	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs
0	0	1										27 μs
0	1	0										fCLK/16
0	1	1										fCLK/8
1	0	0										fCLK/6
1	0	1										fCLK/5
1	1	0										fCLK/4
1	1	1										fCLK/2
0	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs
0	0	1										25 μs
0	1	0										fCLK/16
0	1	1										fCLK/8
1	0	0										fCLK/6
1	0	1										fCLK/5
1	1	0										fCLK/4
1	1	1										fCLK/2

Note (Omitted)

Incorrect:

Table 11-3. A/D Conversion Time Selection (8/8)

(8) $1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (f _{CLK})
FR2	FR1	FR0	LV1	LV0		f _{CLK} = 1 MHz	f _{CLK} = 2 MHz	f _{CLK} = 4 MHz	f _{CLK} = 8 MHz	f _{CLK} = 16 MHz (Note 2)	f _{CLK} = 32 MHz	
0	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f _{CLK} /64
0	0	1										f _{CLK} /32
0	1	0										f _{CLK} /16
0	1	1										f _{CLK} /8
1	0	0										f _{CLK} /6
1	0	1										f _{CLK} /5
1	1	0										f _{CLK} /4
1	1	1										f _{CLK} /2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f _{CLK} /64
0	0	1										f _{CLK} /32
0	1	0										f _{CLK} /16
0	1	1										f _{CLK} /8
1	0	0										f _{CLK} /6
1	0	1										f _{CLK} /5
1	1	0										f _{CLK} /4
1	1	1										f _{CLK} /2
0	0	0	1	0	Low- Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	108 μs
0	0	1										108 μs
0	1	0										108 μs
0	1	1										81 μs
1	0	0				135 μs						
1	0	1				108 μs						
1	1	0				Setting prohibited						
1	1	1				Setting prohibited						
0	0	0	1	1	Low- Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	100 μs
0	0	1										100 μs
0	1	0										100 μs
0	1	1										100 μs
1	0	0				125 μs						
1	0	1				100 μs						
1	1	0				Setting prohibited						
1	1	1				Setting prohibited						

Note (Omitted)

Correct:

Table 11-3. A/D Conversion Time Selection (6/8)

(6) $2.7\text{ V} \leq V_{DD} < 3.6\text{ V}$

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (f _{AD})			
FR2	FR1	FR0	LV1	LV0		f _{CLK} = 1 MHz	f _{CLK} = 2 MHz	f _{CLK} = 4 MHz	f _{CLK} = 8 MHz	f _{CLK} = 16 MHz	f _{CLK} = 32 MHz				
0	0	0	0	0	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54 μs	f _{CLK} /64			
0	0	1									54 μs	27 μs	f _{CLK} /32		
0	1	0									54 μs	27 μs	f _{CLK} /16		
0	1	1									54 μs	27 μs	f _{CLK} /8		
1	0	0									40.5 μs	20.25 μs	10.125 μs	5.0625 μs	f _{CLK} /6
1	0	1									33.75 μs	16.875 μs	8.4375 μs	Setting prohibited	f _{CLK} /5
1	1	0									54 μs	27 μs	13.5 μs	6.75 μs	Setting prohibited
1	1	1	54 μs	27 μs	13.5 μs	6.75 μs	Setting prohibited	Setting prohibited	f _{CLK} /2						
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	50 μs	f _{CLK} /64			
0	0	1									50 μs	25 μs	f _{CLK} /32		
0	1	0									50 μs	25 μs	f _{CLK} /16		
0	1	1									50 μs	25 μs	12.5 μs	6.25 μs	f _{CLK} /8
1	0	0									37.5 μs	18.75 μs	9.375 μs	4.6875 μs	f _{CLK} /6
1	0	1									31.25 μs	15.625 μs	7.8125 μs	Setting prohibited	f _{CLK} /5
1	1	0									50 μs	25 μs	12.5 μs	6.25 μs	Setting prohibited
1	1	1	50 μs	25 μs	12.5 μs	6.25 μs	Setting prohibited	Setting prohibited	f _{CLK} /2						
0	0	0	1	0	Low-Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	42 μs	f _{CLK} /64			
0	0	1									42 μs	21 μs	f _{CLK} /32		
0	1	0									42 μs	21 μs	f _{CLK} /16		
0	1	1									42 μs	21 μs	f _{CLK} /8		
1	0	0									31.5 μs	15.75 μs	7.875 μs	3.9375 μs	f _{CLK} /6
1	0	1									26.25 μs	13.125 μs	6.5625 μs	3.28125 μs	f _{CLK} /5
1	1	0									42 μs	21 μs	Setting prohibited	Setting prohibited	f _{CLK} /4
1	1	1	42 μs	21 μs	Setting prohibited	Setting prohibited	Setting prohibited	f _{CLK} /2							
0	0	0	1	1	Low-Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	38 μs	f _{CLK} /64			
0	0	1									38 μs	19 μs	f _{CLK} /32		
0	1	0									38 μs	19 μs	f _{CLK} /16		
0	1	1									38 μs	19 μs	f _{CLK} /8		
1	0	0									28.5 μs	14.25 μs	7.125 μs	3.5625 μs	f _{CLK} /6
1	0	1									23.75 μs	11.875 μs	5.9375 μs	2.96875 μs	f _{CLK} /5
1	1	0									38 μs	19 μs	Setting prohibited	Setting prohibited	f _{CLK} /4
1	1	1	38 μs	19 μs	Setting prohibited	Setting prohibited	Setting prohibited	f _{CLK} /2							

Correct:

Table 11-3. A/D Conversion Time Selection (7/8)

(7) $1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						on Clock
FR2	FR1	FR0	LV1	LV0		fCLK = 1 MHz	fCLK = 2 MHz	fCLK = 4 MHz	fCLK = 8 MHz	fCLK = 16 MHz ^{Note}	fCLK = 32 MHz	
x	x	x	0	0	Normal 1	Setting prohibited						–
x	x	x	0	1	Normal 2	Setting prohibited						–
0	0	0	1	0	Low- Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	42 μs	fCLK/64
0	0	1						Setting prohibited	Setting prohibited	42 μs	21 μs	fCLK/32
0	1	0						42 μs	21 μs	Setting prohibited	Setting prohibited	fCLK/16
0	1	1						42 μs	21 μs			fCLK/8
1	0	0						31.5 μs	21 μs			fCLK/6
1	0	1						26.25 μs	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/5
1	1	0						42 μs				21 μs
1	1	1						42 μs	21 μs	Setting prohibited	Setting prohibited	fCLK/2
0	0	0	1	1	Low- Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited		38 μs
0	0	1						Setting prohibited	Setting prohibited	38 μs	19 μs	fCLK/32
0	1	0						38 μs	19 μs	Setting prohibited	Setting prohibited	fCLK/16
0	1	1						38 μs	19 μs			fCLK/8
1	0	0						28.5 μs	19 μs			fCLK/6
1	0	1						28.75 μs	Setting prohibited	Setting prohibited	Setting prohibited	fCLK/5
1	1	0						38 μs				19 μs
1	1	1						38 μs	19 μs	Setting prohibited	Setting prohibited	fCLK/2

Note (Omitted)

Correct:

Table 11-3. A/D Conversion Time Selection (8/8)

(8) $1.6\text{ V} \leq \text{VDD} < 1.8\text{ V}$

When there is stabilization wait time (hardware trigger wait mode)

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Time Selection						Conversion Clock (f _{CLK})	
FR2	FR1	FR0	LV1	LV0		f _{CLK} = 1 MHz	f _{CLK} = 2 MHz	f _{CLK} = 4 MHz	f _{CLK} = 8 MHz	f _{CLK} = 16 MHz <small>Note 2</small>	f _{CLK} = 32 MHz		
x	x	x	0	0	Normal 1	Setting prohibited	–	x	x	x	0	0	
x	x	x	0	1	Normal 2	Setting prohibited	–	x	x	x	0	1	
0	0	0	1	0	Low- Voltage 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f _{CLK} /64	
0	0	1										84 μs	f _{CLK} /32
0	1	0										84 μs	f _{CLK} /16
0	1	1										84 μs	f _{CLK} /8
1	0	0										63 μs	f _{CLK} /6
1	0	1										105 μs	f _{CLK} /5
1	1	0										84 μs	f _{CLK} /4
1	1	1										Setting prohibited	f _{CLK} /2
0	0	0	1	1	Low- Voltage 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	f _{CLK} /64	
0	0	1										76 μs	f _{CLK} /32
0	1	0										76 μs	f _{CLK} /16
0	1	1										76 μs	f _{CLK} /8
1	0	0										95 μs	f _{CLK} /6
1	0	1										76 μs	f _{CLK} /5
1	1	0										76 μs	f _{CLK} /4
1	1	1										Setting prohibited	f _{CLK} /2

Note (Omitted)

6. Note when entering A/D converter standby mode added**Note on A/D converter mode register 2 (ADM2) added (page 493)**

Incorrect:

(4) A/D converter mode register 2 (ADM2)

(Omitted)

Caution Only rewrite the value of the ADM2 register while conversion operation is stopped (which is indicated by the ADCS bit of A/D converter mode register 0 (ADM0) being 0).

Correct:

(4) A/D converter mode register 2 (ADM2)

(Omitted)

Cautions 1. Only rewrite the value of the ADM2 register while conversion operation is stopped (which is indicated by the ADCS bit of A/D converter mode register 0 (ADM0) being 0).

2. When entering STOP mode or HALT mode while the CPU is operating on the subsystem clock, do not set ADREFP1 to 1. When selecting internal reference voltage (ADREFP1, ADREFP0 = 1, 0), the current value of A/D converter reference voltage current (I_{ADREF}) shown in 29.4.2 Supply current characteristics is added.

Note on analog input channel specification register (ADS) added (page 497)

Incorrect:

Figure 11-11. Format of Analog Input Channel Specification Register (ADS) (2/2)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

(Omitted)

Cautions 1. Be sure to clear bits 5 and 6 to 0.

(Omitted)

- 6. If using AVREFP as the + side reference voltage source of the A/D converter, do not select ANI0 as an A/D conversion channel.
- 7. If using AVREFM as the - side reference voltage source of the A/D converter, do not select ANI1 as an A/D conversion channel.
- 8. If ADISS is set to 1, the internal reference voltage (1.45 V) cannot be used for the + side reference voltage source.

Correct:

Figure 11-11. Format of Analog Input Channel Specification Register (ADS) (2/2)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

(Omitted)

Cautions 1. Be sure to clear bits 5 and 6 to 0.

(Omitted)

- 6. If using AVREFP as the + side reference voltage source of the A/D converter, do not select ANI0 as an A/D conversion channel.
- 7. If using AVREFM as the - side reference voltage source of the A/D converter, do not select ANI1 as an A/D conversion channel.
- 8. If ADISS is set to 1, the internal reference voltage (1.45 V) cannot be used for the + side reference voltage source.
- 9. When entering STOP mode or HALT mode while the CPU is operating on the subsystem clock, do not set ADISS to 1. When setting ADISS to 1, the current value of the A/D converter reference voltage current (I_{ADREF}) shown in 29.4.2 Supply current characteristics is added.

7. Incorrect descriptions of maskable interrupt request acknowledgement operation revised

Revised incorrect description of time from generation of maskable interrupt until servicing in Table 16-4. (page 842)

Incorrect:

16.4.1 Maskable interrupt request acknowledgment

(Omitted)

Table 16.4 Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time ^{Note}
Servicing time	9 clocks	14 clocks

~~Note If an interrupt request is generated just before the RET instruction, the wait time becomes longer.~~

Remark 1 clock: 1/f_{CLK} (f_{CLK}: CPU clock)

Correct:

16.4.1 Maskable interrupt request acknowledgment

(Omitted)

Table 16.4 Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time ^{Note}
Servicing time	9 clocks	16 clocks

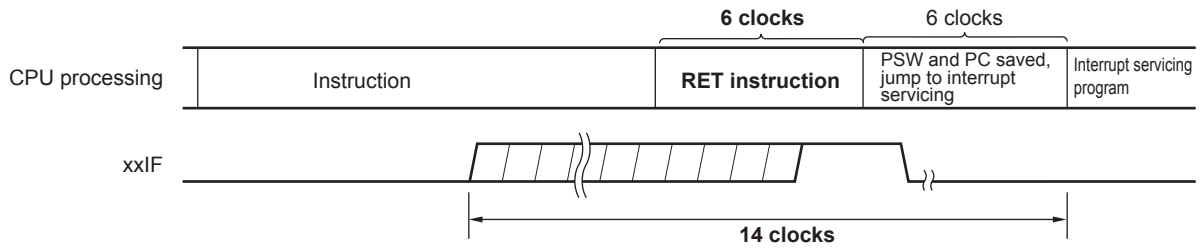
Note Maximum time does not apply when an instruction from the internal RAM area is executed.

Remark 1 clock: 1/f_{CLK} (f_{CLK}: CPU clock)

Figure 16-9. Incorrect description of interrupt request acknowledgment timing (maximum time) revised (page 844)

Incorrect:

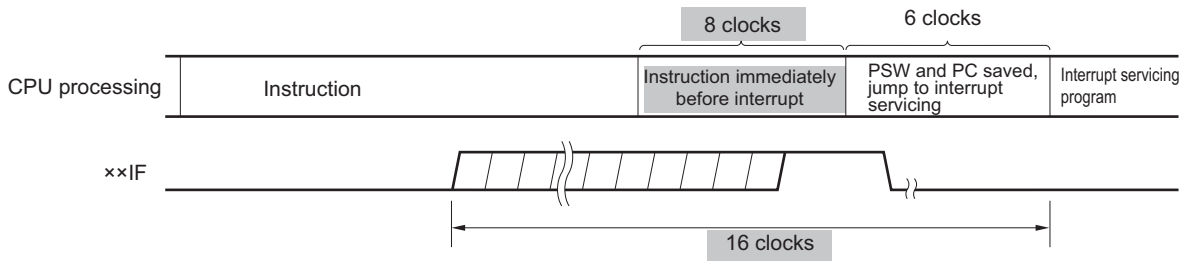
Figure 16-9. Interrupt Request Acknowledgment Timing (Maximum Time)



Remark 1 clock: $1/f_{CLK}$ (f_{CLK} : CPU clock)

Correct:

Figure 16-9. Interrupt Request Acknowledgment Timing (Maximum Time)



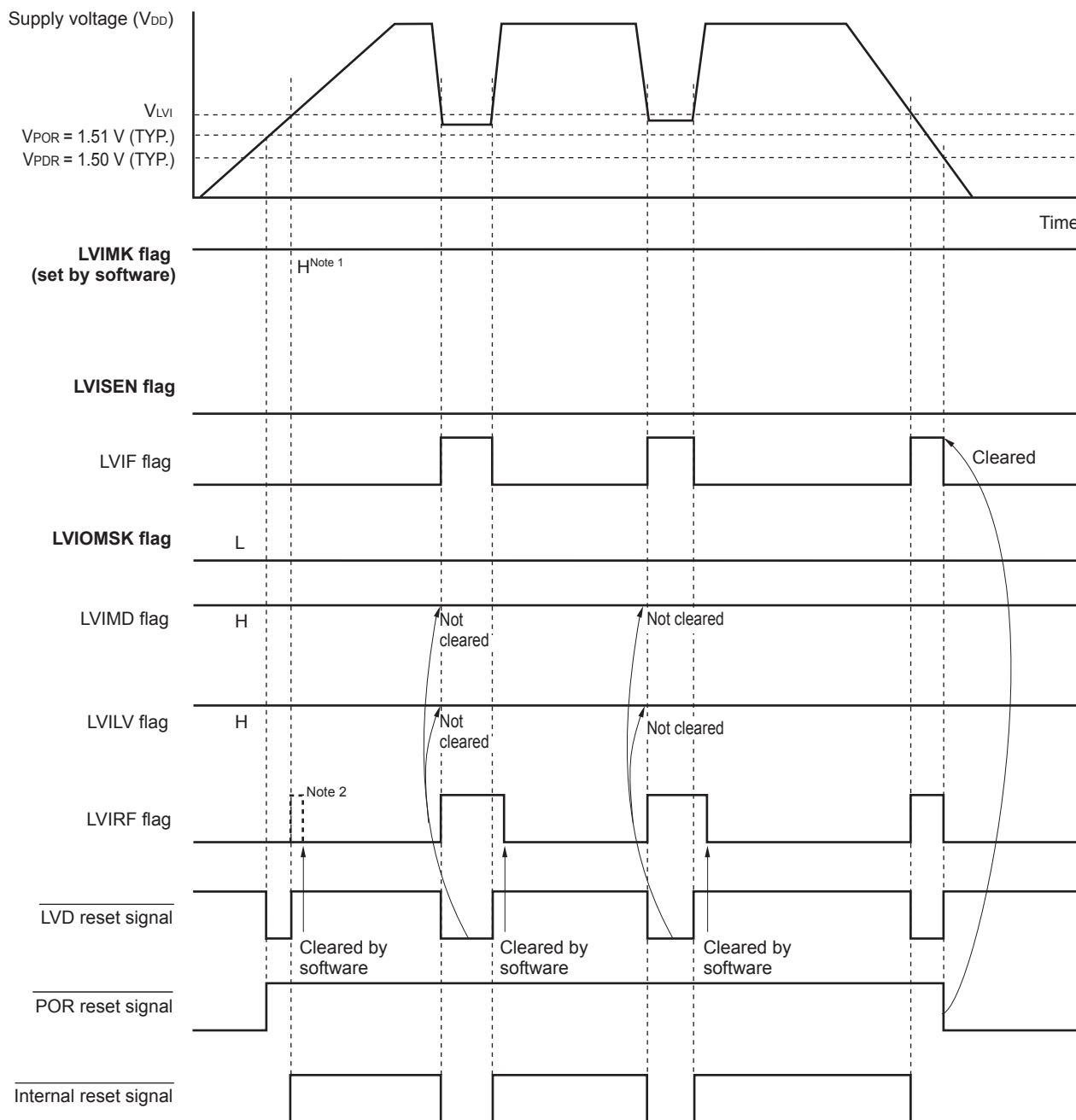
Remark 1 clock: $1/f_{CLK}$ (f_{CLK} : CPU clock)

8. Incorrect descriptions of voltage detector (LVD) timing chart revised

Figure 21-4. Incorrect descriptions of timing of voltage detector internal reset signal generation revised (page 894)

Incorrect:

Figure 21-4. Timing of Voltage Detector Internal Reset Signal Generation (Option Byte LVIMDS1, LVIMDS0 = 1, 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. LVIRF flag is bit 0 of the reset control flag register (RESF).

The LVIRF flag may become 1 from the beginning due to the power-on waveform.

For details of the RESF register, see CHAPTER 19 RESET FUNCTION.

Correct:

Figure 21-4. Timing of Voltage Detector Internal Reset Signal Generation (Option Byte LVIMDS1, LVIMDS0 = 1, 1)

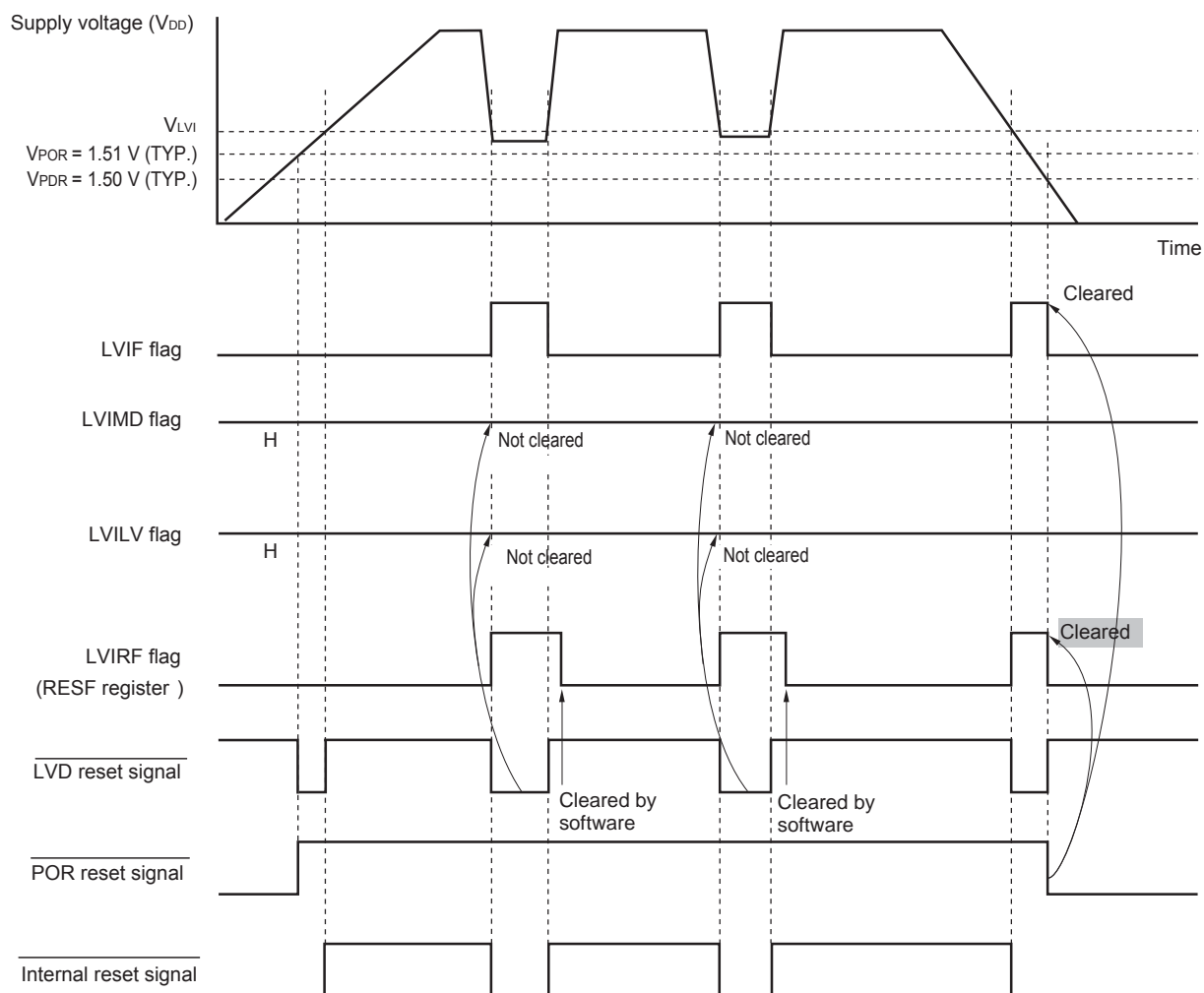
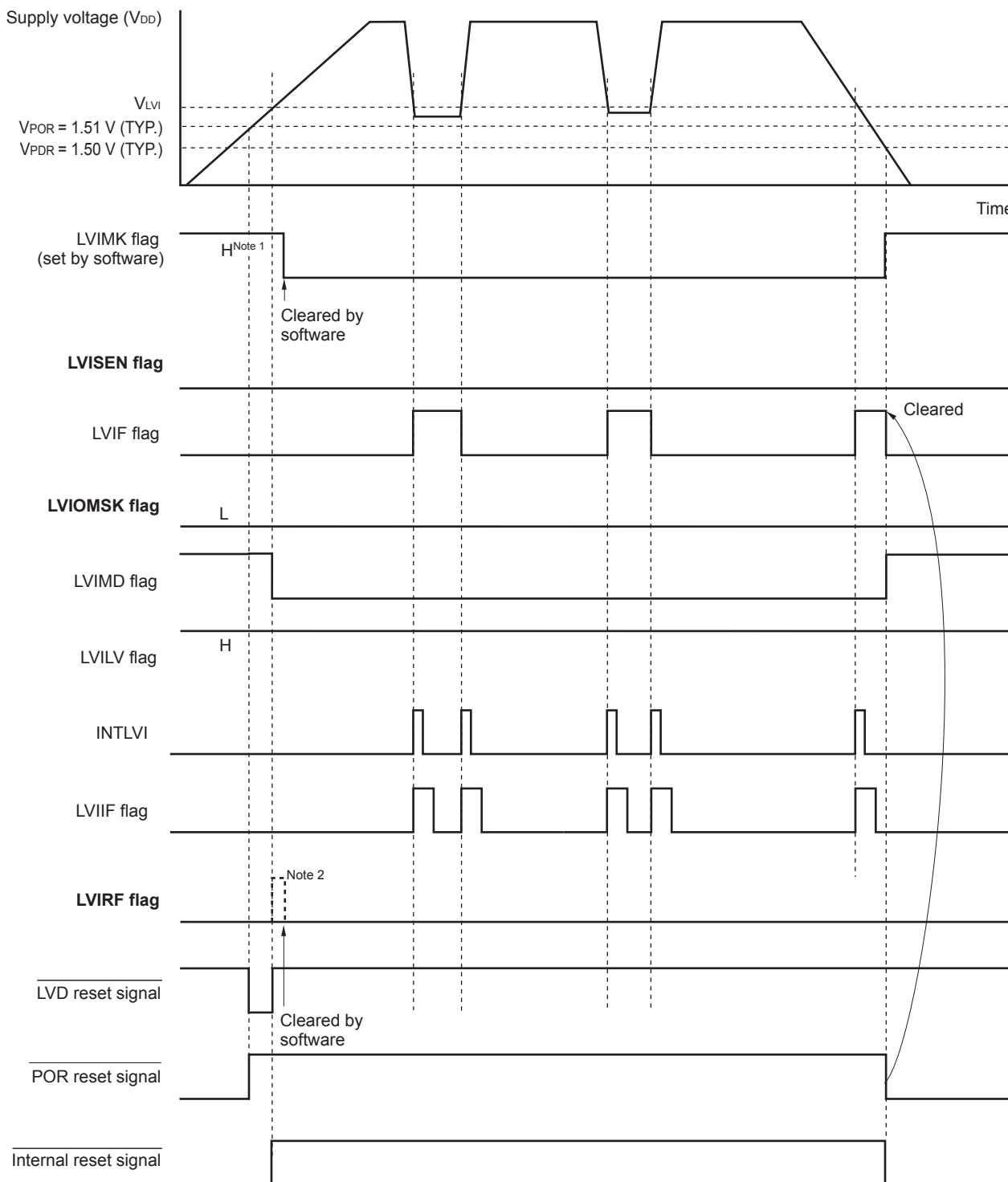


Figure 21-5. Incorrect description of voltage detector internal interrupt signal generation timing revised (page 896)

Incorrect:

Figure 21-5. Timing of Voltage Detector Internal Interrupt Signal Generation
(Option Byte LVIMDS1, LVIMDS0 = 0, 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

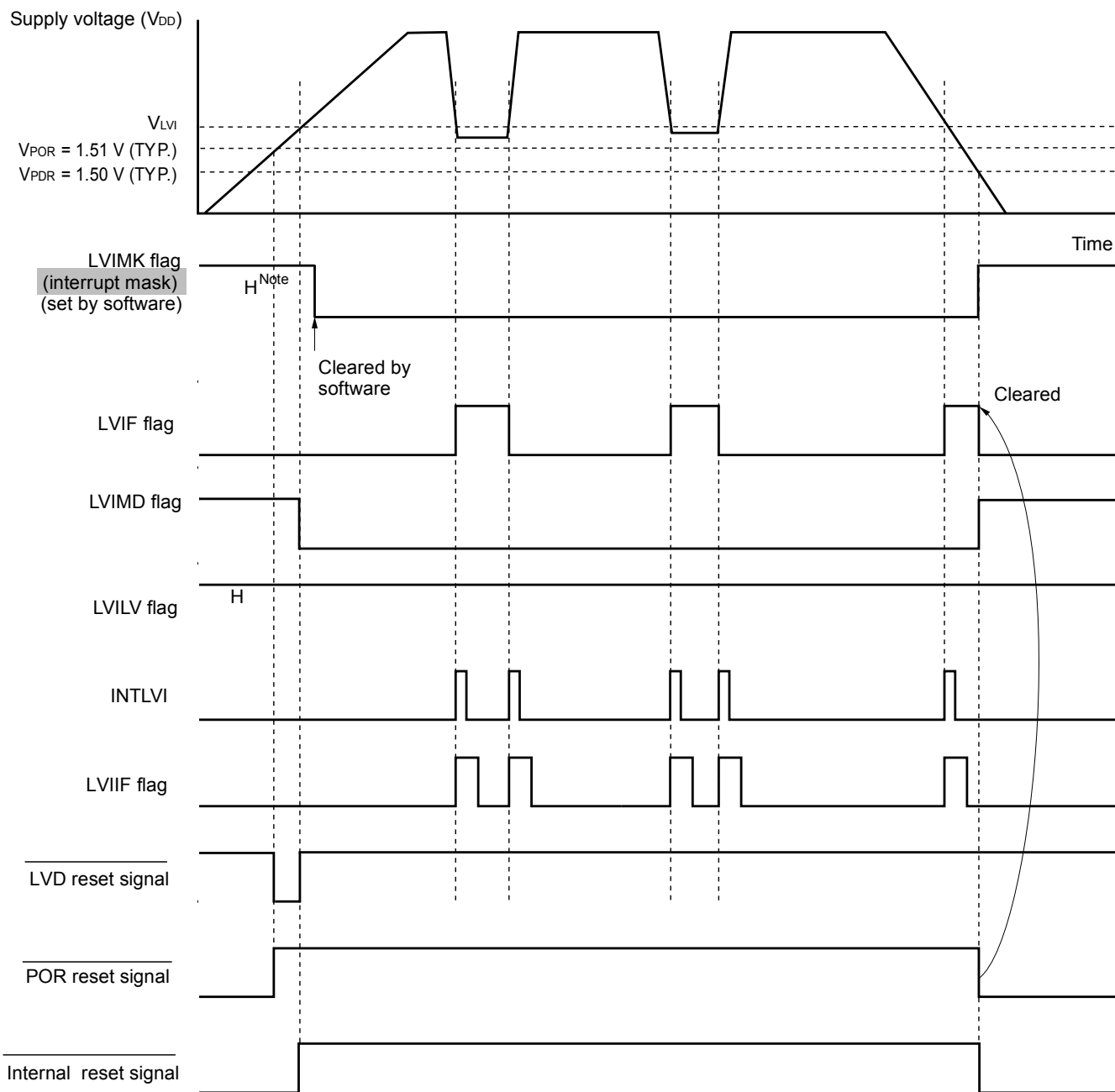
2. LVIRF flag is bit 0 of the reset control flag register (RESF).

The LVIRF flag may become 1 from the beginning due to the power-on waveform.

For details of the RESF register, see CHAPTER 19 RESET FUNCTION.

Correct:

Figure 21-5. Timing of Voltage Detector Internal Interrupt Signal Generation
(Option Byte LVIMDS1, LVIMDS0 = 0, 1)



Note The LVIMK flag is set to "1" by reset signal generation.

9. Incorrect description of voltage detector (LVD) interrupt and reset mode revised

Incorrect description of when used as interrupt and reset mode revised (page 897)

Incorrect:

21.4.3 When used as interrupt and reset mode

- When starting operation

Specify the operation mode (the interrupt and reset (LVIMDS1, LVIMDS0 = 1, 0)) and the detection voltage (V_{LVIH} , V_{LVIL}) by using the option byte 000C1H/010C1H.

(Omitted)

~~Figure 21-6 shows the timing of the internal reset signal and interrupt signal generated by the voltage detector.~~

~~Caution The LVIRF flag may become 1 from the beginning due to the power-on waveform.~~

~~For details of the RESF register, see CHAPTER 19 RESET FUNCTION.~~

Correct:

21.4.3 When used as interrupt and reset mode

- When starting operation

Specify the operation mode (the interrupt and reset (LVIMDS1, LVIMDS0 = 1, 0)) and the detection voltage (V_{LVIH} , V_{LVIL}) by using the option byte 000C1H/010C1H.

(Omitted)

Figure 21-6 shows the timing of voltage detector reset signal and interrupt signal generation.

Perform the processing according to figure 21-7 Processing procedure after an interrupt is generated and figure 21-8

Initial setting of interrupt and reset mode.

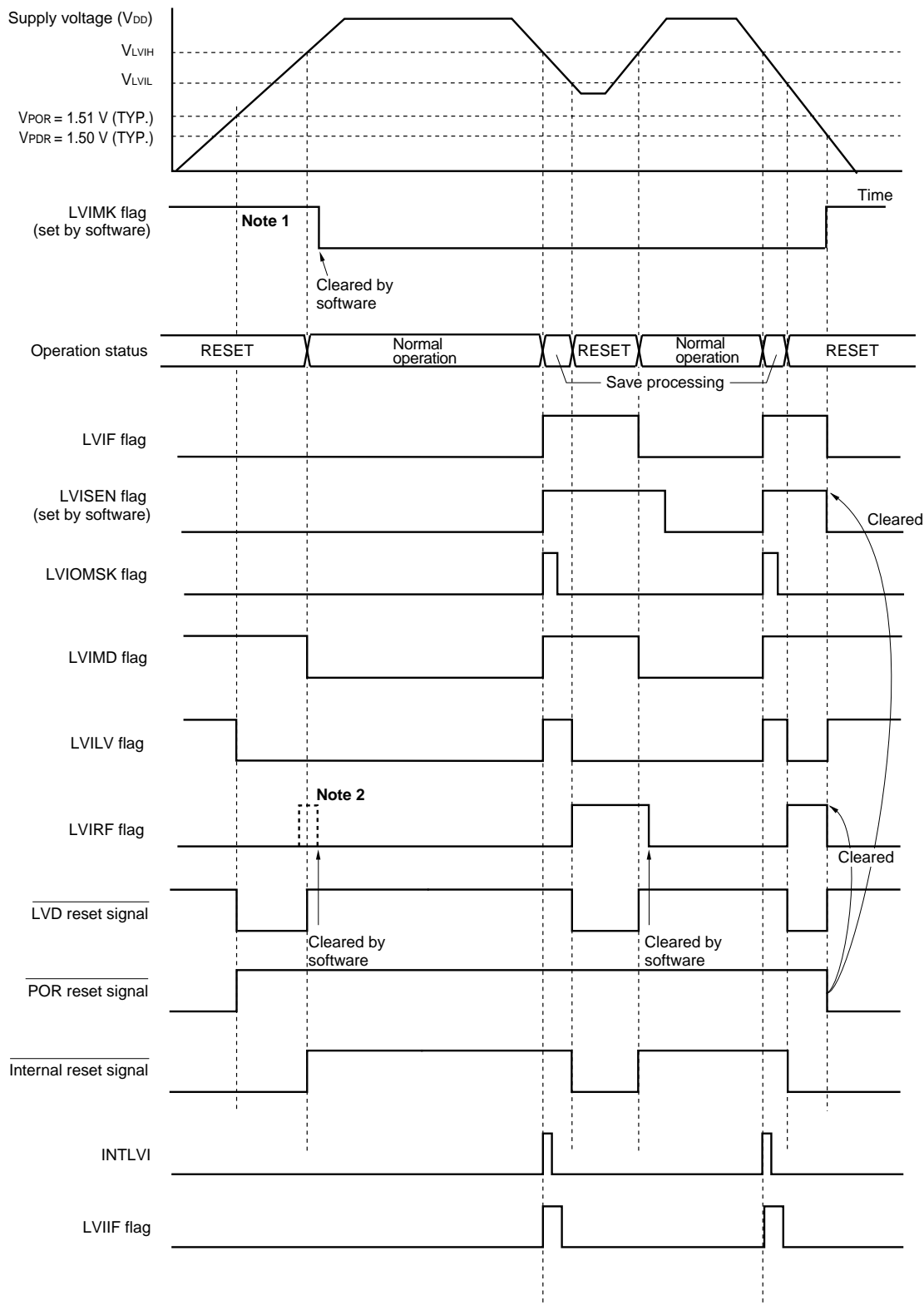
Incorrect description of timing of voltage detector reset signal and interrupt signal generation revised

(page 898)

Incorrect:

Figure 21-6. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation

(Option Byte LVIMDS1, LVIMDS0 = 1, 0)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

~~2. LVIRF flag is bit 0 of the reset control flag register (RESF). The LVIRF flag may become 1 from the beginning due to the power-on waveform. For details of the RESF register, see CHAPTER 19 RESET FUNCTION.~~

Remark V_{POR} : POR power supply rise detection voltage

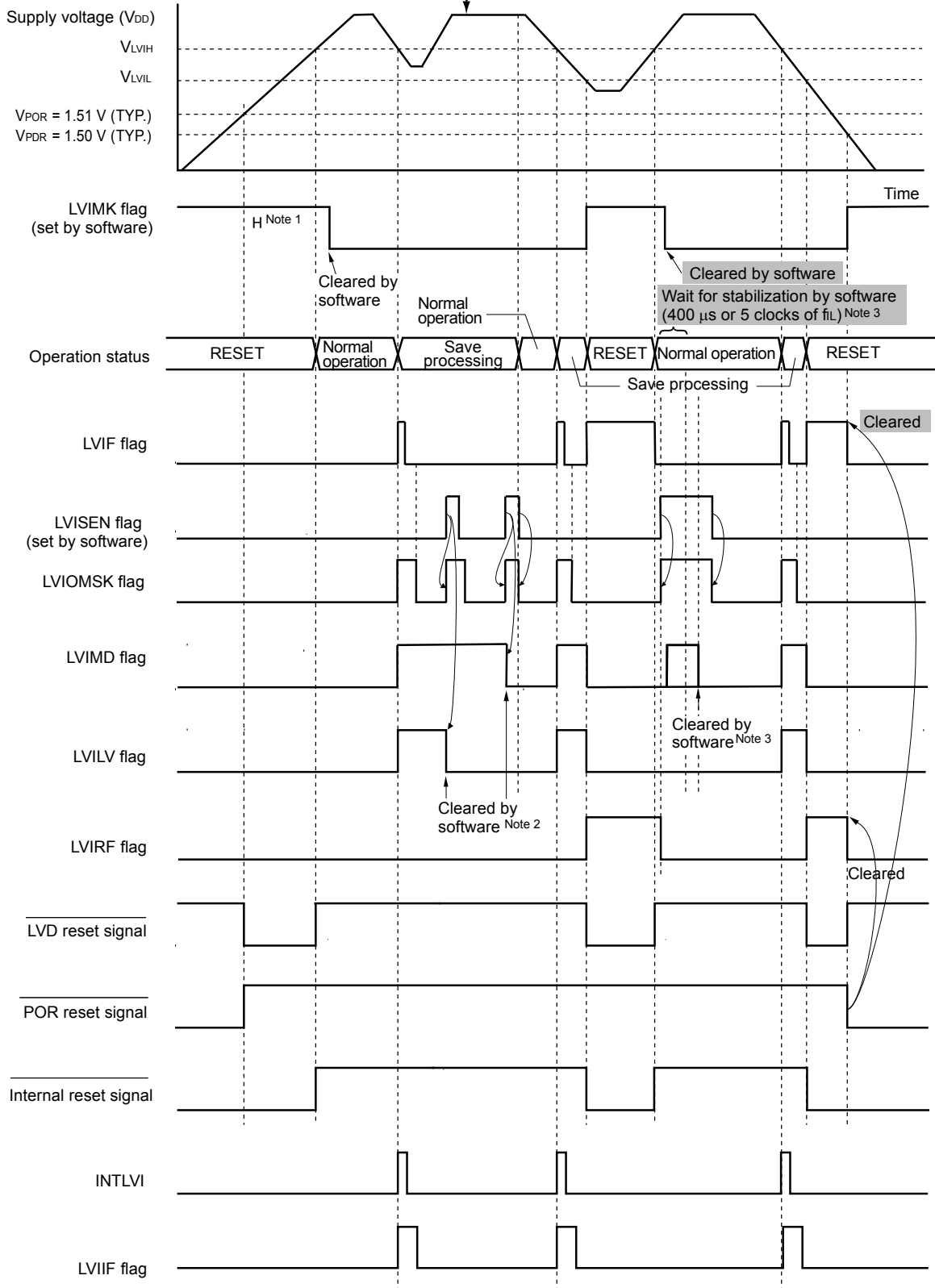
V_{PDR} : POR power supply fall detection voltage

Correct:

Figure 21-6. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation

(Option Byte LVIMDS1, LVIMDS0 = 1, 0) (1/2)

If a reset is not generated after releasing the mask, determine that a condition of V_{DD} becomes $V_{DD} \geq V_{LVIH}$, clear LVIMD, and the MCU returns to normal operation.



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. After an interrupt is generated, perform the processing according to figure 21-7 Processing Procedure After an Interrupt Is Generated in interrupt and reset mode.

3. After a reset is released, perform the processing according to figure 21-8 Initial Setting of Interrupt and Reset Mode in interrupt and reset mode.

Remark V_{POR} : POR power supply rise detection voltage

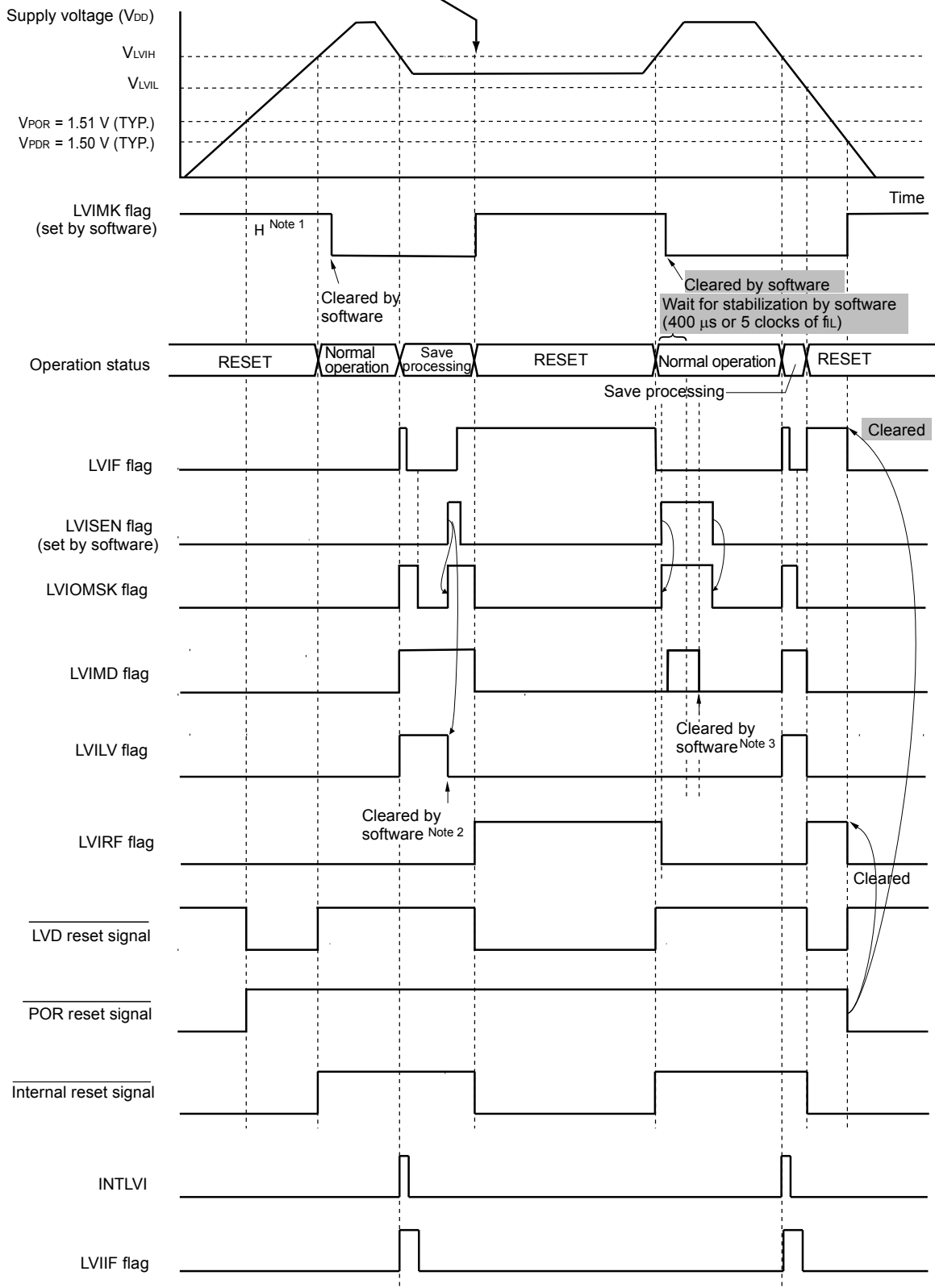
V_{PDR} : POR power supply fall detection voltage

Correct:

Figure 21-6. Timing of Voltage Detector Reset Signal and Interrupt Signal Generation

(Option Byte LVIMDS1, LVIMDS0 = 1, 0) (2/2)

When a condition of V_{DD} is $V_{DD} < V_{LVIH}$ after releasing the mask, a reset is generated because of $LVIMD = 1$ (reset mode).



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. After an interrupt is generated, perform the processing according to figure 21-7 Processing Procedure After an Interrupt Is Generated in interrupt and reset mode.

3. After a reset is released, perform the processing according to figure 21-8 Initial Setting of Interrupt and Reset Mode in interrupt and reset mode.

Remark V_{POR} : POR power supply rise detection voltage

V_{PDR} : POR power supply fall detection voltage

Figure 21-7. Processing Procedure After an Interrupt Is Generated

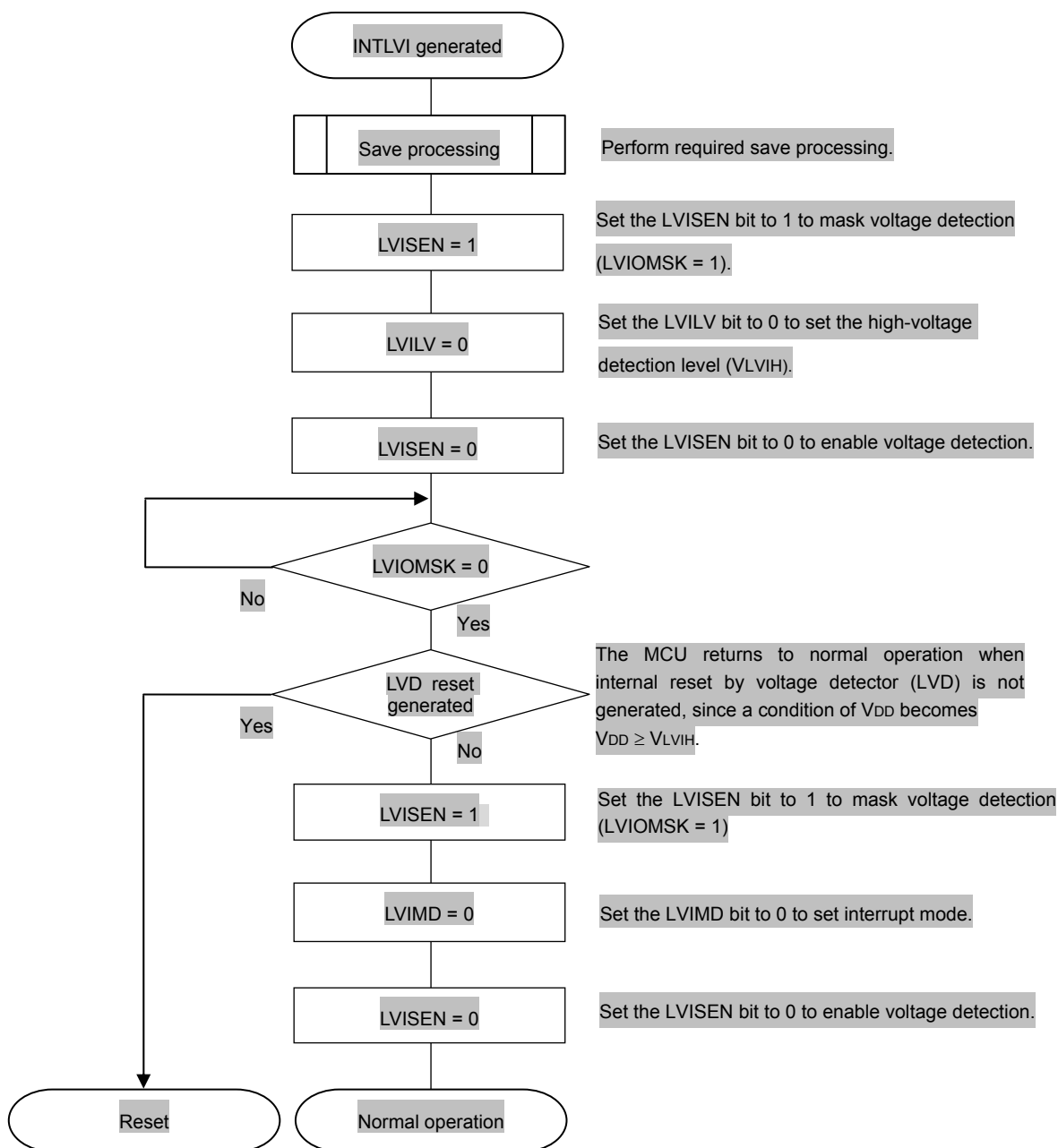
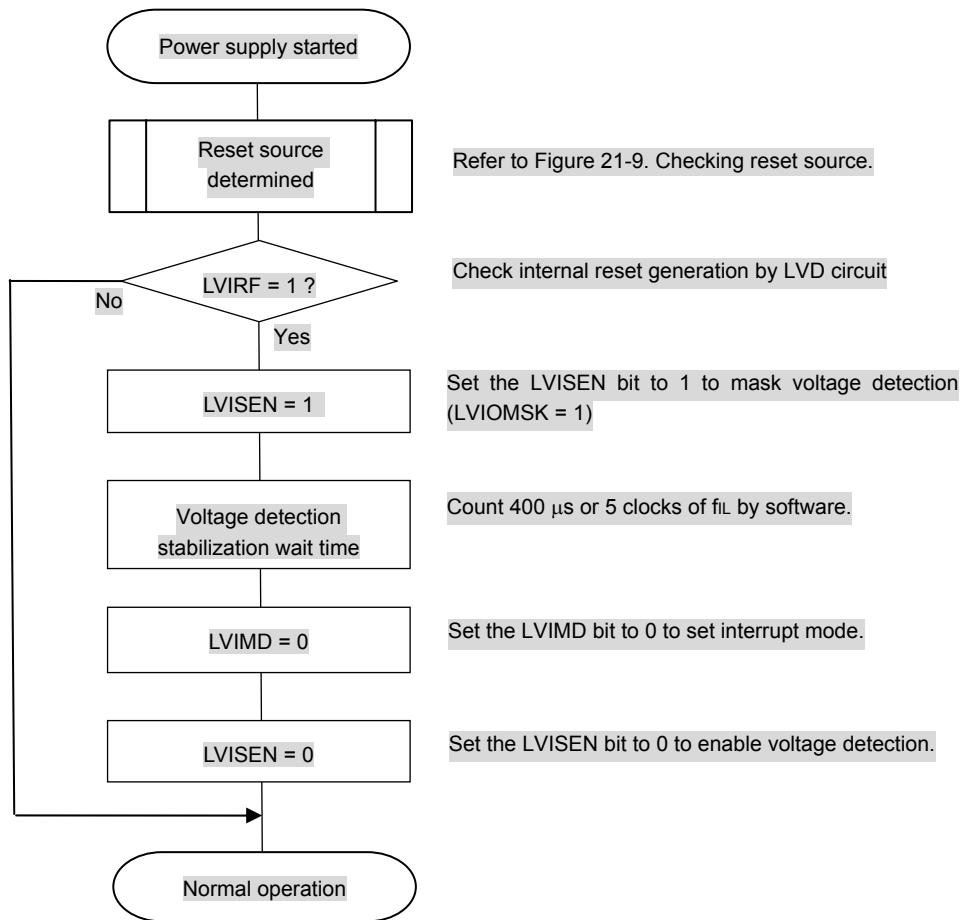


Figure 21-8. Explanations of initial setting of interrupt and reset mode added (page 899)

When setting an interrupt and reset mode (LVIMDS1, LVIMDS0 = 1, 0), voltage detection stabilization wait time for 400 μs or 5 clocks of f_{IL} is necessary after LVD reset is released (LVIRF = 1). After waiting until voltage detection stabilizes, (0) clear the LVIMD bit for initialization. While voltage detection stabilization wait time is being counted and when the LVIMD bit is rewritten, set LVISEN to 1 to mask a reset or interrupt generation by LVD.

Figure 21-8. shows the procedure for initial setting of interrupt and reset mode.

Figure 21-8. Initial Setting of Interrupt and Reset Mode



Remark f_{IL}: Low-speed on-chip oscillator clock frequency

10. Added common item for all RL78/G13 products in 29.4.2 Supply current characteristics of Electrical specifications (page 1005)

Incorrect:

(4) Common to RL78/G13 all products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RTC operating current	IRTC ^{Notes 1, 2}	f _{SUB} = 32.768 kHz	Real-time clock operation		0.02		μA
			Interval timer operation		0.02		
Watchdog timer operating current	IWDT ^{Notes 2,3}	f _{IL} = 15 kHz			0.22		μA
A/D converter operating current	IADC ^{Notes 4}	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.5	0.7	mA
Temperature sensor operating current	ITMPS				75		μA
LVD operating current	ILVI ^{Notes 5}				0.08		μA
BGO operating current	IBGO ^{Notes 6}				2.50	12.20	mA

Note (Omitted)

Correct:

(4) Common to RL78/G13 all products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RTC operating current	IRTC ^{Notes 1, 2}	f _{SUB} = 32.768 kHz	Real-time clock operation		0.02		μA
			Interval timer operation		0.02		
Watchdog timer operating current	IWDT ^{Notes 2,3}	f _{IL} = 15 kHz			0.22		μA
A/D converter operating current	IADC ^{Notes 4}	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	IADREF				75		μA
Temperature sensor operating current	ITMPS				75		μA
LVD operating current	ILVI ^{Notes 5}				0.08		μA
BGO operating current	IBGO ^{Notes 6}				2.50	12.20	mA

Note (Omitted)

11. Explanations when using temperature sensor and internal reference voltage (1.45 V) of A/D converter added

Explanation of Figure 11-7. A/D converter mode register 2 (ADM2) added (page 493)

Incorrect:

Figure 11-7. Format of A/D Converter Mode Register 2 (ADM2) (1/2)

Address: F0010H After reset: 00H R/W

Symbol	7	6	5	4	<3>	<2>	1	<0>
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from V _{DD}
0	1	Supplied from P20/AV _{REFP} /ANI0
1	0	Supplied from the internal reference voltage (1.45 V)
1	1	Setting prohibited
(Omitted)		

(Omitted)

Correct:

Figure 11-7. Format of A/D Converter Mode Register 2 (ADM2) (1/2)

Address: F0010H After reset: 00H R/W

Symbol	7	6	5	4	<3>	<2>	1	<0>
ADM2	ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	0	Supplied from V _{DD}
0	1	Supplied from P20/AV _{REFP} /ANI0
1	0	Supplied from the internal reference voltage (1.45 V) ^{Note}
1	1	Setting prohibited
(Omitted)		

Note This setting value can be selected only in HS (high-speed main) mode.

(Omitted)

Explanation of Figure 11-11. Analog input channel specification register (ADS) added (page 496)

Incorrect:

Figure 11-11. Format of Analog Input Channel Specification Register (ADS) (1/2)

○ Select mode (ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AV _{REFP} pin
0	0	0	0	0	1	ANI1	P21/ANI1/AV _{REFM} pin
(Omitted)							
0	1	1	0	1	1	Setting prohibited	
1	0	0	0	0	0	–	Temperature sensor output
1	0	0	0	0	1	–	Internal reference voltage output (1.45 V)
Other than the above						Setting prohibited	

- Notes 1. 20-, 24-, 25-, 30-, 32-pin products: P01/ANI16 pin
 2. 20-, 24-, 25-, 30-, 32-pin products: P00/ANI17 pin

Correct:

Figure 11-11. Format of Analog Input Channel Specification Register (ADS) (1/2)

○ Select mode (ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AV _{REFP} pin
0	0	0	0	0	1	ANI1	P21/ANI1/AV _{REFM} pin
(Omitted)							
0	1	1	0	1	1	Setting prohibited	
1	0	0	0	0	0	–	Temperature sensor output ^{Note 3}
1	0	0	0	0	1	–	Internal reference voltage output (1.45 V) ^{Note 3}
Other than the above						Setting prohibited	

- Notes 1. 20-, 24-, 25-, 30-, 32-pin products: P01/ANI16 pin
 2. 20-, 24-, 25-, 30-, 32-pin products: P00/ANI17 pin
 3. This setting value can be selected only in HS (high-speed main) mode.

Explanation of 11.7.4 Setup when using temperature sensor added (page 523)

Incorrect:

11.7.4 Setup when using temperature sensor (example for software trigger mode and one-shot conversion mode)

Figure 11-35. Setup When Using Temperature Sensor

(Omitted)

Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

Correct:

11.7.4 Setup when using temperature sensor (example for software trigger mode and one-shot conversion mode)

Figure 11-35. Setup When Using Temperature Sensor

(Omitted)

Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

Caution This setting can be used only in HS (high-speed main) mode.

Explanation of (2) Input range of ANI0 to ANI14 and ANI16 to ANI26 pins in 11.10 Cautions for A/D Converter added (page 530)

Incorrect:

11.10 Cautions for A/D Converter

(2) Input range of ANI0 to ANI14 and ANI16 to ANI26 pins

Observe the rated range of the ANI0 to ANI14 and ANI16 to ANI26 pins input voltage. If a voltage of V_{DD} and AV_{REFP} or higher and V_{SS} and AV_{REFM} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

When internal reference voltage (1.45 V) is selected reference voltage source for the + side of the A/D converter, do not input internal reference voltage or higher voltage to a pin selected by the ADS register. However, it is no problem that a pin not selected by the ADS register is inputted voltage greater than the internal reference voltage.

Correct:

11.10 Cautions for A/D Converter

(2) Input range of ANI0 to ANI14 and ANI16 to ANI26 pins

Observe the rated range of the ANI0 to ANI14 and ANI16 to ANI26 pins input voltage. If a voltage of V_{DD} and AV_{REFP} or higher and V_{SS} and AV_{REFM} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

When internal reference voltage (1.45 V) is selected reference voltage source for the + side of the A/D converter, do not input internal reference voltage or higher voltage to a pin selected by the ADS register. However, it is no problem that a pin not selected by the ADS register is inputted voltage greater than the internal reference voltage.

Caution **The internal reference voltage (1.45 V) can be selected only in HS (high-speed main) mode.**

12. Explanations of A/D test function in Safety functions chapter (section 22.3.8) added

Explanation of Figure 22-15. A/D test register (ADTES) added (page 917)

Incorrect:

(1) A/D test register (ADTES)

Figure 22-15. Format of A/D Test Register (ADTES)

Address: F0013H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADTES	0	0	0	0	0	0	ADTES1	ADTES0

ADTES1	ADTES0	A/D conversion target
0	0	AN _{lxx} (This is specified using the analog input channel specification register (ADS).)
1	0	AV _{REFM}
1	1	AV _{REFP}
Other than the above		Setting prohibited

Correct:

(1) A/D test register (ADTES)

Figure 22-15. Format of A/D Test Register (ADTES)

Address: F0013H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADTES	0	0	0	0	0	0	ADTES1	ADTES0

ADTES1	ADTES0	A/D conversion target
0	0	AN _{lxx} (This is specified using the analog input channel specification register (ADS).) ^{Note}
1	0	AV _{REFM}
1	1	AV _{REFP}
Other than the above		Setting prohibited

Note The temperature sensor output and internal reference voltage output (1.45 V) can be selected only in HS (high-speed main) mode.

Explanation of Figure 22-16. Analog input channel specification register (ADS) added (pages 918 to 919)

Incorrect:

Figure 22-16. Format of Analog Input Channel Specification Register (ADS) (1/2)

○ Select mode (ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AV _{REFP} pin
0	0	0	0	0	1	ANI1	P21/ANI1/AV _{REFM} pin
(Omitted)							
0	1	1	0	1	1	Setting prohibited	
1	0	0	0	0	0	–	Temperature sensor output
1	0	0	0	0	1	–	Internal reference voltage output (1.45 V)
Other than the above						Setting prohibited	

(Notes and cautions are listed on the next page.)

- Notes 1. 20-, 24-, 25-, 30-, 32-pin products: P01/ANI16 pin
- 2. 20-, 24-, 25-, 30-, 32-pin products: P00/ANI17 pin

(Omitted)

Correct:

Figure 22-16. Format of Analog Input Channel Specification Register (ADS) (1/2)

○ Select mode (ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AV _{REFP} pin
0	0	0	0	0	1	ANI1	P21/ANI1/AV _{REFM} pin
(Omitted)							
0	1	1	0	1	1	Setting prohibited	
1	0	0	0	0	0	–	Temperature sensor output ^{Note 3}
1	0	0	0	0	1	–	Internal reference voltage output (1.45 V) ^{Note 3}
Other than the above						Setting prohibited	

(Notes and cautions are listed on the next page.)

- Notes 1. 20-, 24-, 25-, 30-, 32-pin products: P01/ANI16 pin
- 2. 20-, 24-, 25-, 30-, 32-pin products: P00/ANI17 pin
- 3. This setting value can be selected only in HS (high-speed main) mode.

(Omitted)

13. Conditions of A/D converter characteristics in Electrical specifications chapter (section 29.7.1)

added

Condition of (1) When AVREF (+) = AVREFP/ANI0, AVREF (-) = AVREFM/ANI1, target ANI pin : ANI2 to ANI14 added (page 1032)

Incorrect:

(1) When AVREF (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AVREF (-) = AVREFM/ANI1 (ADREFM = 1), target ANI pin : ANI2 to ANI14

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Notes 1, 2}	AINL	10-bit resolution AVREFP = VDD	1.8 V ≤ VDD ≤ 5.5 V	1.2	±3.5	LSB
			1.6 V ≤ VDD ≤ 5.5 V	1.2	±7.0	LSB
Conversion time	tCONV	(Omitted)				
Zero-scale error ^{Notes 1, 2}	EZS					
Full-scale error ^{Notes 1, 2}	EFS					
Integral linearity error ^{Note 1}	ILE					
Differential linearity error ^{Note 1}	DLE					
Reference voltage (+)	AVREFP		1.6		VDD	V
Analog input voltage	VAIN		0		AVREFP	V
	VBGR	2.4 V ≤ VDD ≤ 5.5 V	1.38	1.45	1.5	V

(Omitted)

Correct:

(1) When $AV_{REF(+)} = AV_{REFP}/ANI0$ ($ADREFP1 = 0, ADREFP0 = 1$), $AV_{REF(-)} = AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin : ANI2 to ANI14

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error ^{Notes 1, 2}	A_{INL}	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 3.5	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
Conversion time	t_{CONV}	(Omitted)					
Zero-scale error ^{Notes 1, 2}	E_{ZS}						
Full-scale error ^{Notes 1, 2}	E_{FS}						
Integral linearity error ^{Note 1}	I_{LE}						
Differential linearity error ^{Note 1}	D_{LE}						
Reference voltage (+)	AV_{REFP}			1.6		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP}	V
	V_{BGR}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	HS mode	1.38	1.45	1.5	V

(Omitted)

Condition of (2) When AVREF (+) = AVREFP/ANI0, AVREF (-) = AVREFM/ANI1, target ANI pin : ANI16 to ANI26 added (page 1033)

Incorrect:

(2) When AVREF (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AVREF (-) = AVREFM/ANI1 (ADREFM = 1), target ANI pin : ANI16 to ANI26

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Notes 1, 2}	AINL	10-bit resolution		1.2	±5.0	LSB
		AVREFP = VDD	1.8 V ≤ VDD ≤ 5.5 V			
			1.6 V ≤ VDD ≤ 5.5 V	1.2	±8.5	LSB
Conversion time	tCONV	(Omitted)				
Zero-scale error ^{Notes 1, 2}	EZS					
Full-scale error ^{Notes 1, 2}	EFS					
Integral linearity error ^{Note 1}	ILE					
Differential linearity error ^{Note 1}	DLE					
Reference voltage (+)	AVREFP		1.6		VDD	V
Analog input voltage	VAIN		0		AVREFP and EVDD0	V
	VBGR	2.4 V ≤ VDD ≤ 5.5 V	1.38	1.45	1.5	V

(Omitted)

Correct:

(2) When $AV_{REF} (+) = AV_{REFP}/ANI0$ ($ADREFP1 = 0, ADREFP0 = 1$), $AV_{REF} (-) = AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin : ANI16 to ANI26

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = AV_{REFM})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error ^{Notes 1, 2}	A_{INL}	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 5.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 8.5	LSB
Conversion time	t_{CONV}	(Omitted)					
Zero-scale error ^{Notes 1, 2}	E_{ZS}						
Full-scale error ^{Notes 1, 2}	E_{FS}						
Integral linearity error ^{Note 1}	I_{LE}						
Differential linearity error ^{Note 1}	D_{LE}						
Reference voltage (+)	AV_{REFP}			1.6		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP} and EV_{DD0}	V
	V_{BGR}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	HS mode	1.38	1.45	1.5	V

(Omitted)

Condition of (3) When AVREF (+) = VDD, AVREF (-) = VSS, target ANI pin : ANI0 to ANI14, ANI16 to ANI26 added (page 1034)

Incorrect:

(3) When AVREF (+) = VDD (ADREFP1 = 0, ADREFP0 = 0), AVREF (-) = VSS (ADREFM = 0), target ANI pin : ANI0 to ANI14, ANI16 to ANI26

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V, Reference voltage (+) = VDD, Reference voltage (-) = VSS)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Resolution	RES		8		10	bit	
Overall error ^{Notes 1, 2}	AINL	10-bit resolution	1.8 V ≤ VDD ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ VDD ≤ 5.5 V		1.2	±10.5	LSB
Conversion time	tCONV	(Omitted)					
Zero-scale error ^{Notes 1, 2}	EZS						
Full-scale error ^{Notes 1, 2}	EFS						
Integral linearity error ^{Note 1}	ILE						
Differential linearity error ^{Note 1}	DLE						
Analog input voltage	VAIN	ANI0 to ANI14	0		VDD	V	
		ANI16 to ANI26	0		EVDD0	V	
	VBGR	2.4 V ≤ VDD ≤ 5.5 V	1.38	1.45	1.5	V	

(Omitted)

Correct:

(3) When $AV_{REF (+)} = V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), $AV_{REF (-)} = V_{SS}$ (ADREFM = 0), target ANI pin : ANI0 to ANI14, ANI16 to ANI26

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		8		10	bit
Overall error ^{Notes 1, 2}	AINL	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.2	± 7.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.2	± 10.5	LSB
Conversion time	t_{CONV}	(Omitted)				
Zero-scale error ^{Notes 1, 2}	EZS					
Full-scale error ^{Notes 1, 2}	EFS					
Integral linearity error ^{Note 1}	ILE					
Differential linearity error ^{Note 1}	DLE					
Analog input voltage	V_{AIN}	ANI0 to ANI14	0		V_{DD}	V
		ANI16 to ANI26	0		EV_{DD0}	V
	V_{BGR}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ HS mode	1.38	1.45	1.5	V

(Omitted)

Condition of (4) When AVREF (+) = Internal reference voltage, AVREF (-) = AVREFM/ANI1, target ANI pin : ANI0 to ANI14, ANI16 to ANI26 added (page 1035)

Incorrect:

(4) When AVREF (+) = Internal reference voltage (ADREFFP1 = 1, ADREFFP0 = 0), AVREF (-) = AVREFM/ANI1 (ADREFM = 1), target ANI pin : ANI0 to ANI14, ANI16 to ANI26

(TA = -40 to +85°C, ~~1.6 V < EVDD0 = EVDD1 < VDD < 5.5 V~~, VSS = EVSS0 = EVSS1 = 0 V, Reference voltage (+) = VBGR, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	tCONV	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±1.0	LSB
Reference voltage (+)	VBGR			1.38	1.45	1.5	V
Reference voltage (-)	AVREFM			VSS			V
Analog input voltage	VAIN			0		VBGR	V

(Omitted)

Correct:

(4) When AVREF (+) = Internal reference voltage (ADREFFP1 = 1, ADREFFP0 = 0), AVREF (-) = AVREFM/ANI1 (ADREFM = 1), target ANI pin : ANI0 to ANI14, ANI16 to ANI26

(TA = -40 to +85°C, ~~2.4 V < VDD < 5.5 V~~, VSS = EVSS0 = EVSS1 = 0 V, Reference voltage (+) = VBGR, Reference voltage (-) = AVREFM = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	tCONV	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±1.0	LSB
Reference voltage (+)	VBGR			1.38	1.45	1.5	V
Reference voltage (-)	AVREFM			VSS			V
Analog input voltage	VAIN			0		VBGR	V

(Omitted)

14. Condition of Temperature sensor characteristics in Electrical Specifications chapter (section 29.7.2) added (page 1036)

Incorrect:

29.7.2 Temperature sensor characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} < \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} < \text{V}_{\text{DD}} < 5.5\text{ V}$, $V_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Reference output voltage	V_{CONST}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		-3.6		mV/C
Operation stabilization wait time	t_{AMP}				5	μs

Correct:

29.7.2 Temperature sensor characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$, $V_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Reference output voltage	V_{CONST}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		-3.6		mV/C
Operation stabilization wait time	t_{AMP}				5	μs

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TN-RL*-A001A/E	Dec. 5, 2011	First edition issued Incorrect descriptions of No.1 to No.10 revised
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