To our customers,

# Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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# RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

| Product Category | MPU&MCU | | Document No. | TN-H8*-A338A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Correction of the H8SX/1600 Series Hardware Manual | | Information Category | Technical Notification | | |
| Applicable Product | See below. | Lot No.<br>All lots | Reference Document | See below. | | |

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of some modifications in the description on the standby control register and in the interrupt input timing figure of electrical characteristics.

**[Target Products and Reference Documents]**

**Target Products**

| Series | Group | Reference Document |
|---|---|---|
| H8SX/1600 | H8SX/1650 | H8SX/1650 Group Hardware Manual (Rev. 2.00 REJ09B0029-0200Z) |
| | H8SX/1657 | H8SX/1657 Group Hardware Manual (Rev. 1.00 REJ09B0106-0100Z) |

## 1. Changes to the Description on the Standby Control Register

### 1.1 Standby Mode

Though the standby control register (SBYCR) is described as an 8-bit register, it is modified to a 16-bit register. The lower 8 bits of SBYCR are reserved.

**[Before change]**

Standby Control Register (SBYCR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | SSBY | OPE | — | STS4 | STS3 | STS2 | STS1 | STS0 |
| Initial Value | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | SSBY | 0 | R/W | Omitted (No changes) |
| 6 | OPE | 1 | R/W | |
| 5 | — | 0 | R/W | |
| 4 | STS4 | 0 | R/W | |
| 3 | STS3 | 1 | | |
| 2 | STS2 | 1 | | |
| 1 | STS1 | 1 | | |
| 0 | STS0 | 1 | | |

**[After change]**

Standby Control Register (SBYCR)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | SSBY | OPE | — | STS4 | STS3 | STS2 | STS1 | STS0 |
| Initial Value | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | — | — | — | — | — | — | — | — |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 15 | SSBY | 0 | R/W | Omitted (No changes) |
| 14 | OPE | 1 | R/W | |
| 13 | — | 0 | R/W | |
| 12 | STS4 | 0 | R/W | |
| 11 | STS3 | 1 | | |
| 10 | STS2 | 1 | | |
| 9 | STS1 | 1 | | |
| 8 | STS0 | 1 | | |
| 7 to 0 | — | All 0 | R/W | Reserved<br>These bits are always read as 0. The write values should always be 0 |

## 1.2 List of Registers

Though SBYCR is described as an 8-bit register in the section on the List of Registers, it is modified to a 16-bit register. The lower 8 bits of SBYCR are reserved.

**[Before change]**

| Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 | Module |
|---|---|---|---|---|---|---|---|---|---|
| Other registers except SBYCR omitted | | | | | | | | | |
| SBYCR | SSBY | OPE | — | STS4 | STS3 | STS2 | STS1 | STS0 | |

**[After change]**

| Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 | Module |
|---|---|---|---|---|---|---|---|---|---|
| Other registers except SBYCR omitted | | | | | | | | | |
| SBYCR | SSBY | OPE | — | STS4 | STS3 | STS2 | STS1 | STS0 | |
| | — | — | — | — | — | — | — | — | |

## 1.3 Affect on Software

The address before and after the modification is shown below. There are not changes concerning the addresses of SSBY, OPE, and STS[4:0]. This modification does not cause any software changes.

**[Address before change]**

SBYCR (8-bit register)

| | Bit: 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **H'FFDC6** | SSBY | OPE | — | STS4 | STS3 | STS2 | STS1 | STS0 |

**[Address after change]**

SBYCR (16-bit register)

| | Bit: 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **H'FFDC6** | SSBY | OPE | — | STS4 | STS3 | STS2 | STS1 | STS0 | — | — | — | — | — | — | — | — |

• Address in byte access

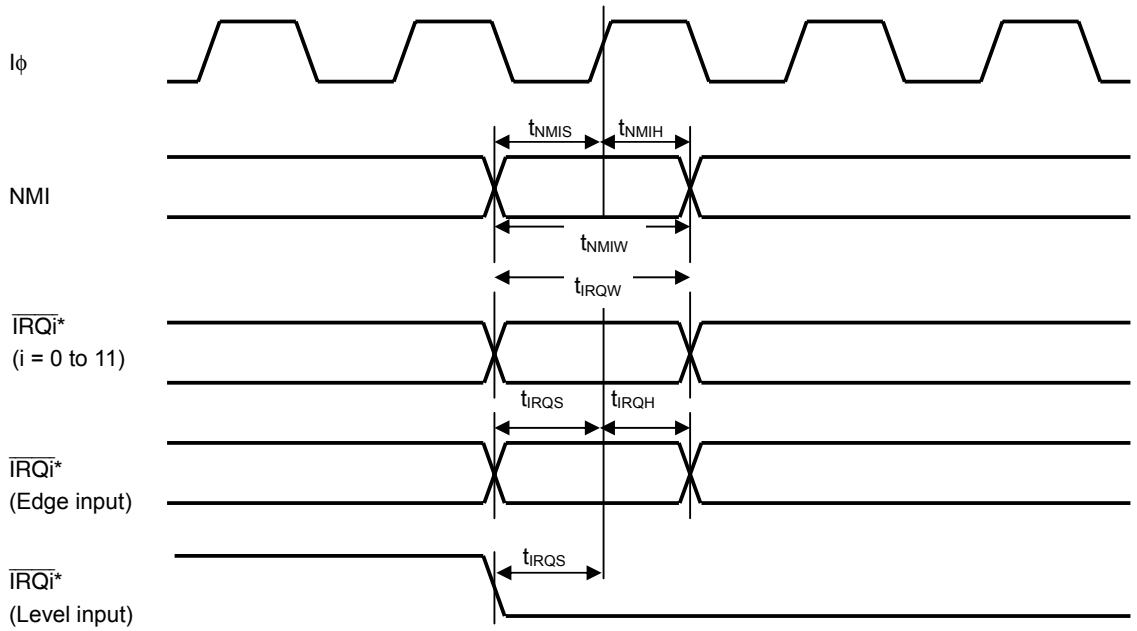
| | Bit: 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **H'FFDC6** | SSBY | OPE | — | STS4 | STS3 | STS2 | STS1 | STS0 |

| | Bit: 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| H'FFDC7 | — | — | — | — | — | — | — | — |

## 2. Interrupt Input Timing

The reference clock in the interrupt input timing figure of electrical characteristics is corrected as follows:

**[Before change]** Reference clock at Iϕ rising




**[After change]** Reference clock at Iϕ falling