To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Renesas Technology Corp.

Product Category	MPU/MCU		Document No.	TN-SH7-A754A/E	Rev.	1.00
Title	Correction of errors in the SH7216 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	SH7216 Group SH7214 Group	Lot No. After 0924	Reference Document	SH7216 Group Hardware Manual Rev1.01 REJ09B0543-0101		

This update is to inform you of corrections to errors in the hardware manual for the applicable products indicated above.

The required changes are given in detail below.

<Addition and corrections>

Section 1 Overview

- Product names have been added to the items or specification for table 1.1, SH7216 Features as follows.

[Before change]

Items	Specification
FPU	On-chip floating-point coprocessor
Clock pulse generator (CPG)	CPU clock: Maximum 200 MHz
Ethernet controller (EtherC)	Media Access Control function (MAC)
On-chip ROM	1 Mbyte
On-chip RAM	Eight pages 128 Kbytes
Packages	LQFP2424-176 (0.5 pitch): R5F72167 LQFP2020-176 (0.4 pitch): R5F72167

[After change]

Items	Specification
FPU (SH7216A, SH7216B, SH7216G, and SH7216H only)	On-chip floating-point coprocessor
Clock pulse generator (CPG)	CPU clock: Maximum 200 MHz (SH7216A, SH7216B, SH7214A, SH7214B) Maximum 100 MHz (SH7216G, SH7216H, SH7214G, SH7214H)
Ethernet controller (EtherC) (SH7216A, SH7214A, SH7216G, and SH7214G only)	Media Access Control function (MAC)
On-chip ROM	1 Mbyte, 768 Kbytes, 512 Kbytes
On-chip RAM	Eight pages, six pages, four pages 128 Kbytes, 96 Kbytes, 64 Kbytes
Packages	LQFP2424-176 (0.5 pitch) LQFP2020-176 (0.4 pitch) BGA1313-176 (0.8 pitch)

- Pin assignment for BGA package has been added to figure 1.2, Pin Assignment.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	PE1	VSS	PE14	PE11	PE8	VSS	PA2	VSS	AVREFVSS	PF5	AVREF	PF3	PF0	AVREFVSS	RES	A
B	PE3	PE0	VCCQ	PE13	PE9	PE7	PA3	PA0	AVSS	PF6	AVREF	PF1	ASEMD0	VCL	VSS	B
C	PE6	PE4	PE2	PE12	PE10	PA5	PA1	VCL	MD0	AVCC	AVCC	TRST	FWE	VCCQ	TDO	C
D	PA21	PE5	VCL	PE15	VCCQ	PA4	WDTOVF	MD1	PF7	PF4	PF2	AVSS	TCK	TMS	TDI	D
E	PA18	PA19	PA20	VSS								PLLVCC	PLLVSS	EXTAL	XTAL	E
F	PA16	PA15	PA17	VSS								PB14	NMI	PB15	VSS	F
G	PA13	VSS	VCCQ	PA14								DrVSS	VBUS	USD-	USD+	G
H	PC2	PC3	PC1	PC0								PB12	PB13	DrVCC	VSS	H
J	PC6	PC7	PC5	PC4								VCL	VCCQ	USBEXTAL	USBXTAL	J
K	PC9	PC10	PC8	VSS								PA8	PA7	PA6	VSS	K
L	PC12	PC13	PC11	PC14								VSS	PA11	PA10	PA9	L
M	PC15	VSS	VCCQ	PB0	PB8	VSS	PD4	PD5	VSS	PD14	PD19	PD21	PD30	VCCQ	PA12	M
N	VCL	PB1	PB5	PB7	PB10	PD1	VCCQ	PD10	PD11	VCL	PD16	VCCQ	PD27	PD29	PD31	N
P	PB2	PB3	VCL	VCCQ	PB11	PD3	PD7	PD9	PD13	VSS	PD18	PD22	PD24	PD25	PD28	P
R	PB4	PB6	VSS	PB9	PD0	PD2	PD6	PD8	PD12	PD15	PD17	PD20	PD23	VSS	PD26	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

BP-176V
(Top view)

- The following amendments have been made to the pin functions for figure 1.2, Pin Assignment on page 11, in Section 1, Overview.

[Before change]

No.48 PB7/A23/IRQ7/SCK4/TCLKC/TEND0

[After change]

No.48 PB7/A23/IRQ7/SCK4/TCLKC/TEND0/RDWR

Section 2 CPU

- The following explanation has been added on page 21 in section 2, CPU.

[Before change]

Figure 2.1 shows the data format supported by the SH-2A/SH2A-FPU.

[After change]

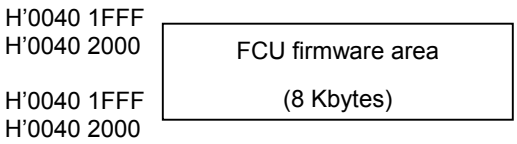
Figure 2.1 shows the data formats supported by the SH-2A and SH2A-FPU.

The CPU of the SH7216A, SH7216B, SH7216G, and SH7216H is the SH2A-FPU; the CPU of the SH7214A, SH7214B, SH7214G, and SH7214H is the SH-2A.

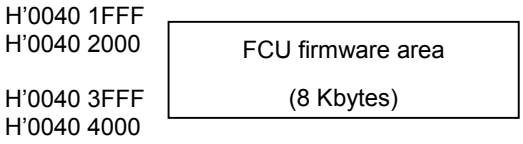
Section 3 MCU Operating Modes

- The following amendments have been made to figures 3.1 to 3.3 on pages 73 to 75.

[Before change]



[After change]



Section 4 Clock Pulse Generator (CPG)

- The following note has been added to figure 4.1, Block Diagram of Clock Pulse Generator on page 78 in section 4, Clock Pulse Generator (CPG).

[After change]

Note: Maximum operating frequencies:

Iϕ (max.) = 200MHz for the SH7216A, SH7216B, SH7214A, and SH7214B

Iϕ (max.) = 100 MHz for the SH7216G, SH7216H, SH7214G, and SH7214H

- The following note has been added to 4.3, Clock Operating Modes on page 82 in section 4, Clock Pulse Generator (CPG).

  [Before change]

  Maximum operating frequencies:

  Iϕ = 200 MHz, Bϕ= 50 MHz, Pϕ = 50 MHz, Mϕ= 100 MHz, Aϕ = 50 MHz

  [After change]

  Maximum operating frequencies*: Iϕ = 200 MHz/100 MHz, Bϕ= 50 MHz, Pϕ = 50 MHz, Mϕ= 100 MHz, Aϕ = 50 MHz

  * Iϕ (max.) = 200MHz for the SH7216A, SH7216B, SH7214A, and SH7214B

    Iϕ (max.) = 100 MHz for the SH7216G, SH7216H, SH7214G, and SH7214H

Section 7 User Break Controller (UBC)

- The following has been added to section 7, User Break Controller (UBC) on page 235,

  [After change]

  7.5.1 Interrupt Source

  The UBC has the user break interrupt as an interrupt source.

  Table 7.4 gives details of this interrupt source.

  A user break interrupt is generated when any of the compare–match flag bits (SCMFD3 to 0 and SCMFC3 to 0) in the break control register (BRCR) is set to 1.

  Clearing the interrupt flag bit to 0 cancels the interrupt request.

  Table 7.4 Interrupt Source

Name	Interrupt Source	Interrupt Enable Bit	Interrupt Flag	Interrupt Level
User break	User break Interrupt	—	SCMFD3, SCMFD2, SCMFD1, SCMFD0, SCMFC3, SCMFC2, SCMFC1, SCMFC0	Fixed at 15

Section 8 Data Transfer Controller (DTC)

- The following amendment has been made to the explanation under 8.5.9, DTC Bus Release Timing on page 238 in section 8, Data Transfer Controller (DTC).

  [Before change]

  The DTC requests the bus mastership to the bus arbiter when an activation request occurs. The DTC releases the bus after a vector read, NOP execution after vector read, transfer information read, a single data transfer,

[After change]

The DTC requests the bus mastership to the bus arbiter when an activation request occurs. The DTC releases the bus after a vector read, transfer information read, a single data transfer,

- The following amendments have been made to the notes for table 8.11 under 8.5.9, DTC Bus Release Timing on page 238 in section 8, Data Transfer Controller (DTC)

  [Before change]

  The following restrictions apply to setting 2.

  The clock setting through the frequency control register (FROCR) must be Iφ: Bφ : Pφ = 8 : 4 : 4, 4 : 2 : 2, or 2 : 1 : 1.

  [After change]

  The following limitation applies to setting 2.

  Set the frequency control register (FRQCR) so that IΦ : BΦ : PΦ : MΦ : AΦ is 16 : 4 : 4 : 4 : 4, 16 : 4 : 4 : 8 : 4, 8 : 4 : 4 : 4 : 4, or 8 : 4 : 4 : 8 : 4.

  The following limitation applies to setting 3.

  Set the DTPR bit in BSCEHR to 0. Setting this bit to 1 is prohibited.

- The following has been added to the notes for 8.5.10, DTC Activation Priority Order on page 240, in section 8, Data Transfer Controller (DTC).

  [After change]

  Although transfer starts for the first source from which a request was received when a DTC request is generated before the next activation trigger, when an activation trigger with higher priority has arrived before generation of the DTC request, transfer starts for the source with higher priority. Generation of the DTC request varies depending on the operation state of the internal bus.

- The following amendment has been made to the explanation under 8.9.1, Module Standby Mode Setting on page 244 in section 8, Data Transfer Controller.

  [Before change]

  Operation of the DTC can be disabled or enabled using the standby control register. The initial setting is for operation of the DTC to be disabled.

  [After change]

  Operation of the DTC can be disabled or enabled using the standby control register. The initial setting is for operation of the DTC to be enabled.

Section 9 Bus State Controller (BSC)

- The following amendments have been made to the explanation under 9.4.8, Bus Function Extending Register (BSCEHR) on pages 302 and 303 in section 9, Bus State Controller (BSC).

[Before change]

Description of the DTBST bit

1. Clock setting through the frequency control register (FRQCR) must be Iϕ : Bϕ : Pϕ: Mϕ: Aϕ = 4 : 2 : 2 : 2 : 2 or 2 : 1 : 1 :1 : 1.

Description of the DTPR bit

Note that DTC transfer is always started according to the DTC activation priority when multiple DTC activation requests are generated while the DTC is active.

Notes: When this bit is set to 1, the following restrictions apply.

1. The vector information must be stored in the on-chip ROM or on-chip RAM.
2. The transfer information must be stored in the on-chip RAM.
3. The function for skipping the transfer information read step is always disabled.

[After change]

Description of the DTBST bit

1. Clock setting through the frequency control register (FRQCR) must be Iϕ : Bϕ : Pϕ: Mϕ: Afϕ = 16 : 4 : 4 : 4 : 4, 16 : 4 : 4 : 8 : 4, 8 : 4 : 4 : 4 : 4, or 8 : 4 : 4 : 8 : 4.

Description of the DTPR bit

For details, refer to section 8.5.10, DTC Activation Priority Order.

Notes: When this bit is set to 1, the following restrictions apply.

1. The vector information must be stored in the on-chip ROM or on-chip RAM.
2. The transfer information must be stored in the on-chip RAM.
3. The function for skipping the transfer information read step is always disabled.
4. Set DTLOCK = 0. The setting DTLOCK = 1 is prohibited.

- The following has been added to the notes for table 9.17 under 9.5.7, Burst ROM (Clock Asynchronous) Interface on page 358 in section 9, Bus State Controller (BSC).

[After change]

Only the DMAC is capable of transfer with 16 bytes as the unit of access. The largest unit of access for the DTC, E-DMAC, and CPU is 32 bits.

- The following amendment has been made to the explanation under 9.5.9, Burst ROM (Clock Synchronous) Interface on page 363 in section 9, Bus State Controller (BSC).

  [Before change]

  These invalid data read cycles increase the memory access time and degrade the program execution speed and DMA transfer speed. To prevent this problem, using 16-byte read by cache fill in the cache-enabled space or 16-byte read by the DMA is recommended.

  [After change]

  These invalid data read cycles increase the memory access time and degrade the program execution speed and DMA transfer speed. To prevent this problem, 16-byte read by the DMA is recommended.

- The following explanation has been added on page 378 in section 9, Bus State Controller (BSC).

  [After change]

  9.6 Interrupt Sources

  9.6.1 Interrupt Sources

  The BSC has the compare–match interrupt (CMI) as an interrupt source.

  Table 9.23 gives details of this interrupt source. The compare–match interrupt enable (CMIE) bit in the refresh timer control/status register (RTCSR) enables or disables this interrupt source.

  Setting of the compare–match flag in the RTCSR to 1 while the setting of the compare–match interrupt enable (CMIE) bit is 1 leads to the generation of a compare–match interrupt.

  Clearing the interrupt flag bit to 0 cancels the interrupt request.

  Table 9.23 Interrupt Sources

Name	Interrupt Source	Interrupt enable bit	Interrupt Flag
CMI	compare–match interrupt	CMIE	CMF

- The following amendment has been made to the explanation under 9.6.1, Note on Connection of External LSI Circuits such as SDRAMs and ASICs on page 378 in section 9, Bus State Controller (BSC).

  [Before change]

  Each of the following pairs of pin functions among the pins for the output of SDRAM control signals is multiplexed on respective single pins: RD/WR and A16, RASL and A18, and CASL and A19. When an external chip (SDRAM, ASIC, etc.) is to be connected to the bus of a SH7216 Group product, follow the procedure described below.

  - Use the 16 bits from A0 to A15 as the address for the external chip such as ASICs.

[After change]

Each of the following pairs of pin functions among the pins for the output of SDRAM control signals is multiplexed on respective single pins: RD/WR and PB0/ A16, RD/WR and PB7/A23, RASL and PB2/A18, and CASL and PB3/A19. When an external chip (SDRAM, ASIC, etc.) is to be connected to the bus of a SH7216 Group product, the connection should be as described below.

.

- Use the multiplexed RD/WR signal on PB7/A23.
- Use the 23 bits from A0 to A22 as the address for an external chip such as an ASICs.

Section 10 Direct Memory Access Controller (DMAC)

- The following explanation has been added on page 429 in section 10, Direct Memory Access Controller (DMAC).

[After change]

10.5 Interrupt Sources

10.5.1 Interrupt Sources and Order of Priority

The interrupt sources of the DMAC are the data transfer end interrupt (DEI) and data transfer half-end interrupt (HEI) for each channel.

The interrupt sources and their order of priority are listed in table 10.11.

The IE bit and HIE bits in the DMA channel control registers (CHCRs) enable or disable the respective interrupt sources. Furthermore, the interrupt requests are independently conveyed to the interrupt controller.

A data-transfer end interrupt (DEI) is generated when, in the DMA channel control register (CHCR), the transfer end flag is set to 1 while the setting of the transfer end interrupt enable (IE) bit is 1.

A data-transfer 1/2 end interrupt (HEI) is generated when, in the DMA channel control register (CHCR), the half-end flag is set to 1 while the setting of the half-end interrupt enable (HIE) bit is 1.

Clearing the interrupt flag bits to 0 cancels the interrupt requests.

Priority among the channels is adjustable by the interrupt controller. The order of priority for interrupts of a given channel is fixed. For details, refer to section 6, Interrupt Controller.

Table 10.11 Interrupt Sources

Channel	Interrupt Source	Interrupt Enable	Interrupt Flag	Priority
0	Data transfer end interrupt (TEI_0)	IE	TE	High
	Data transfer half end interrupt (HEI_0)	HIE	HE	
1	Data transfer end interrupt (TEI_1)	IE	TE	
	Data transfer half end interrupt (HEI_1)	HIE	HE	
2	Data transfer end interrupt (TEI_2)	IE	TE	
	Data transfer half end interrupt (HEI_2)	HIE	HE	
3	Data transfer end interrupt (TEI_3)	IE	TE	
	Data transfer half end interrupt (HEI_3)	HIE	HE	
4	Data transfer end interrupt (TEI_4)	IE	TE	
	Data transfer half end interrupt (HEI_4)	HIE	HE	
5	Data transfer end interrupt (TEI_5)	IE	TE	
	Data transfer half end interrupt (HEI_5)	HIE	HE	
6	Data transfer end interrupt (TEI_6)	IE	TE	
	Data transfer half end interrupt (HEI_6)	HIE	HE	
7	Data transfer end interrupt (TEI_7)	IE	TE	
	Data transfer half end interrupt (HEI_7)	HIE	HE	Low

Section 14 Compare Match Timer (CMT)

- The following amendment has been made to the explanation under 14.2.1, Compare Match Timer Start Register (CMSTR) on page 721 in section 14, Compare Match Timer.

  [Before change]

  CMSTR is initialized to H'0000 by a power-on reset or in software standby mode, but retains its previous value in module standby mode.

  [After change]

  CMSTR is initialized to H'0000 by a power-on reset or in module standby mode, but retains its previous value in software standby mode.

- The following amendment has been made to the explanation under 14.2.2, Compare Match Timer Control/Status Register (CMCSR) on page 722 in section 14, Compare Match Timer.

  [Before change]

  CMCSR is initialized to H'0000 by a power-on reset or in software standby mode, but retains its previous value in module standby mode.

[After change]

CMCSR is initialized to H'0000 by a power-on reset or in module standby mode, but retains its previous value in software standby mode.

- The following amendment has been made to the explanation under 14.2.3, Compare Match Counter (CMCNT) on page 724 in section 14, Compare Match Timer.

[Before change]

CMCNT is initialized to H'0000 by a power-on reset or in software standby mode, but retains its previous value in module standby mode.

[After change]

CMCNT is initialized to H'0000 by a power-on reset or in module standby mode, but retains its previous value in software standby mode.

- The following amendment has been made to the explanation under 14.2.4 Compare Match Constant Register (CMCOR) on page 724 in section 14, Compare Match Timer.

[Before change]

CMCOR is initialized to H'FFFF by a power-on reset or in software standby mode, but retains its previous value in module standby mode.

[After change]

CMCOR is initialized to H'0000 by a power-on reset or in software standby mode, but retains its previous value in software standby mode.

- The following has been added to the explanation under 14.4.1, Interrupt Sources and DTC/DMA Transfer Requests on page 726 in section 14, Compare Match Timer (CMT).

[After change]

Table 14.2 Interrupt Sources

Channel	Interrupt Source	Interrupt Enable Bit	Interrupt Flag Bit	DMAC/DTC Activation	Priority
0	CMI0	CMIE	CMF	Possible	High
1	CMI1	CMIE	CMF	Possible	Low

Section 15 Watchdog Timer (WDT)

- The following has been added to section 15, Watchdog Timer (WDT), on page 743.

[After change]

15.5.1 Interrupt Sources

The watchdog timer has the interval timer interrupt as an interrupt source.

Table 15.3 gives details of this interrupt source.

This source generates an interval timer interrupt when the interval timer overflow flag (IOVF) bit in the watchdog timer control/status register (WTCSR) is set to 1.

Clearing the interrupt flag bit to 0 cancels the interrupt request.

Table 15.3 Interrupt Sources

Name	Interrupt Source	Interrupt Enable Bit	Interrupt Flag Bit
ITI	Interval timer	—	Interval timer overflow flag (IOVF)

Section 16 Serial Communication Interface (SCI)

- The following amendment has been made to the explanation under 16.3.7, Serial Status Register (SCSSR) on page 757 to 762 in section 16, Serial Communication Interface (SCI).

[Before change]

By a power-on reset or in standby mode

[After change]

By a power-on reset or in module standby mode

- The following amendment has been made to the figure 16.12, Sample Flowchart for Receiving Serial Data (1) on page 795 in section 16, Serial Communication Interface (SCI).

[Before change]

Set the CKE1 and CKE0 bits in SCSCR (TE and RE bits are 0).

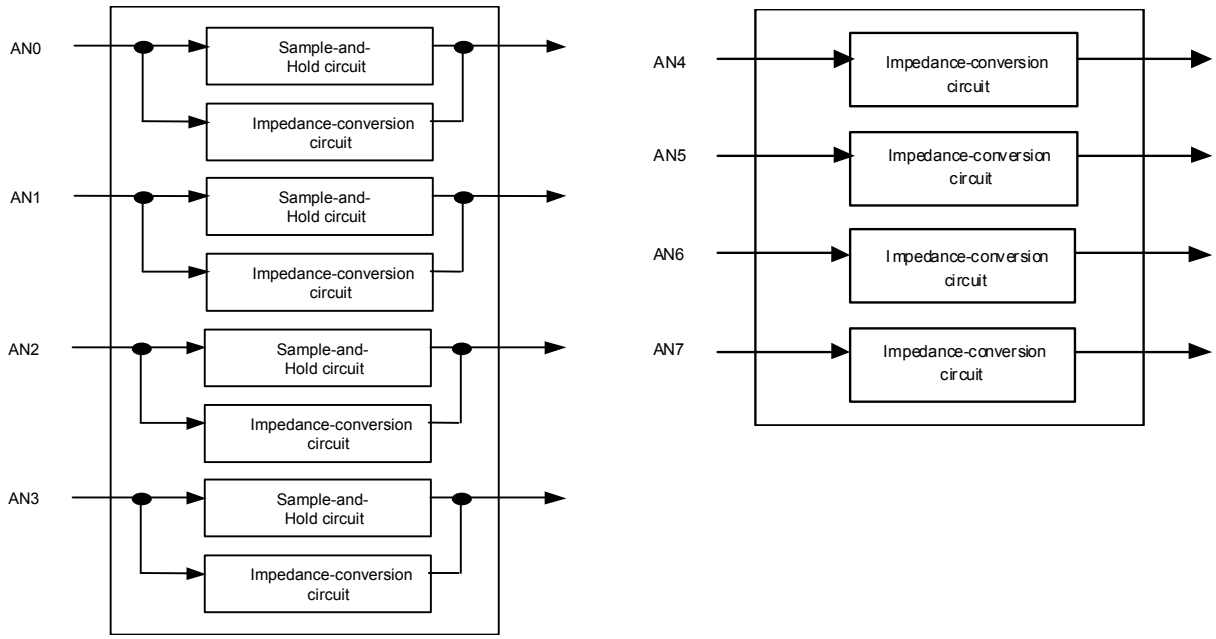
[After change]

Read the receive data register (SCRDR) and clear the RDRF flag in SCSSR to 0.

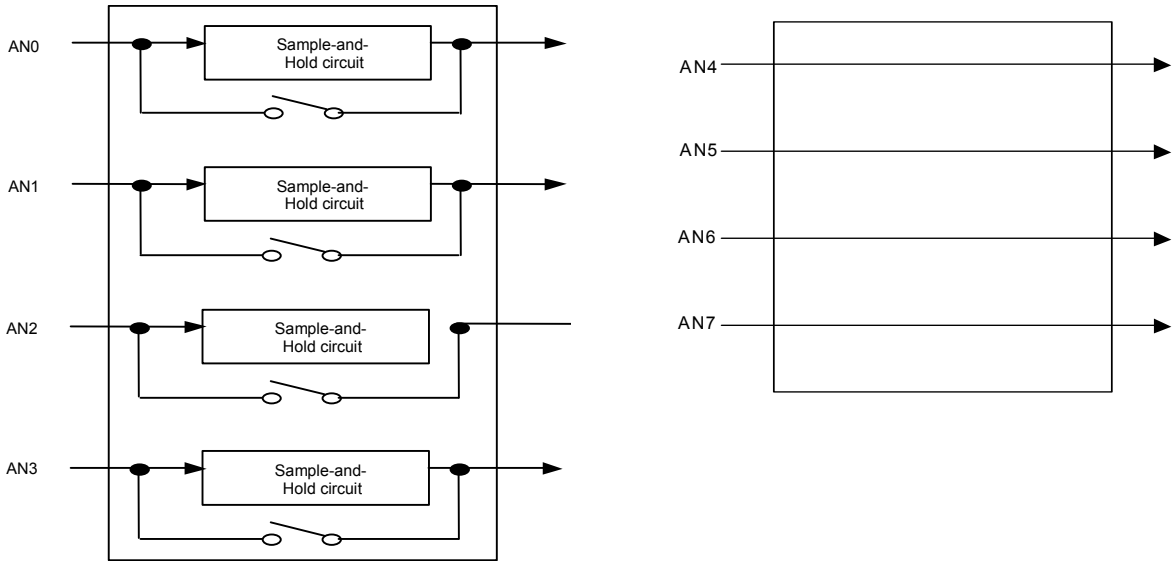
Section 20 A/D Converter Serial Communication Interface (SCI)

- The following amendments have been made to the figure 20.1, Block Diagram of A/D Converter on page 1006 in section 20, A/D Converter (ADC).

[Before change]



[After change]



- The following amendment has been made to the figure 20.4, Example 1 of A/D_0 Converter Operation (Continuous Scan Mode and Sample-and-Hold Circuit Enabled) on page 1022 in section 20, A/D Converter (ADC).

  [Before change]

  [ADBYPSCR_0 setting]

  SH bit = 0

  [After change]

  [ADBYPSCR_0 setting]

  SH bit = 1

- The following amendments have been made to the explanation under 20.7.5, Notes on Noise Countermeasures on page 1033 in section 20, A/D Converter (ADC).

  [Before change]

  The bypass capacitors connected to AVREF and the filter capacitor connected to ANn should be connected to the AVss.

  [After change]

  The bypass capacitors connected to AVREF and the filter capacitor connected to ANn should be connected to the

  AVREFVSS.

  0.1μF capacitor shown in figure 20.10 should be placed as close to the pins as possible.

Section 21 Controller Area Network (RCAN-ET)

- The following amendments have been made to the explanation under 21.3.3. (3), BCR0 on page 1060 in section 21, Controller Area Network (RCAN-ET).

  [Before change]

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	BPR[7:0]	00000000	R/W	Baud Rate Pre-scale These bits are used to define the peripheral bus clock periods contained in a Time Quantum. 00000000 : 2 x peripheral bus clock 00000001 : 4 x peripheral bus clock 00000010 : 6 x peripheral bus clock : : 2 x (register value + 1) x peripheral bus clock 11111111 : 512 x peripheral bus clock

  [After change]

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	BPR[7:0]	00000000	R/W	Baud Rate Pre-scale These bits are used to define the peripheral bus clock periods contained in a Time Quantum. 00000000 : 2 x peripheral bus clock 00000001 : 4 x peripheral bus clock 00000010 : 6 x peripheral bus clock : : 2 x (register value + 1) x peripheral bus clock 01111111 : 512 x peripheral bus clock

- The following have been added to section 21, Controller Area Network (RCAN-ET), on page 1097.

[After change]
21.9 Usage Notes

21.9.1 Module Standby Mode

Settings to run or stop the clock for the RCAN-ET module can be made in standby control register 6 (STBCR6). The initial value stops the clock for the module. Change the setting after release from module-stop mode.

21.9.2 Reset

The RCAN-ET module has a hardware reset and a software reset.

- Hardware reset

The RCAN-ET module is initialized in the hardware reset and module standby states.

- Software reset

The CAN communications function and contents of registers other than the MCR0 bit are initialized by the MCR0 bit in the master control register (MCR).

Since the IRR0 bit in the interrupt request register (IRR) becomes set through initialization at the time of a reset, clear it as indicated in the “configuration mode” section of the reset sequence.
Since regions other than message control field 1 (CONTROL1) in mailboxes are configured as RAM, they are not initialized by a reset. Accordingly, initialize all mailboxes as indicated in the “configuration mode” section of the reset sequence.

21.9.3 CAN Sleep Mode

In CAN sleep mode, supply of the clock signal within the module is largely stopped. Accordingly, do not attempt access to registers other than the MCR, GSR, IRR, and IMR during periods in CAN sleep mode.

21.9.4 Register Access

During the period where the CAN communications function within the RCAN-ET module is storing a frame received over the CAN bus in a mailbox, a wait of zero to five cycles of the peripheral bus clock is generated for access to regions of the mailboxes.

21.9.5 Interrupts

Mailbox 0 reception interrupt is capable of activating the DTC or DMAC as indicated in table 21.2. When the Mailbox 0 reception interrupt source is in use as an activation source for DTC or DMAC operation, read from message control field 0 (CONTROL0) to message control field 1 (CONTROL1) by using the block transfer mode etc. of the DTC or the transfer counter mode etc. of the DMAC.

Section 22 Pin Function Controller (PFC)

- The following amendments have been made to table 22.2, Multiplexed Pins (SH7216 Port B) on page 1102 in section 22, Pin Function Controller (PFC).

[Before change]

Table 22.2 Multiplexed Pins (SH7216 Port B)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)	Function 6 (Related Module)	Function 7 (Related Module)	Function 8 (Related Module)
B	PB7 I/O (Port)	A23 output (BSC)	TEND0 output (DMAC)	IRQ7 input (INTC)	TCLKC input (MTU2)	—	SCK4 I/O (SCI)	—

[After change]

Table 22.2 Multiplexed Pins (SH7216 Port B)

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)	Function 6 (Related Module)	Function 7 (Related Module)	Function 8 (Related Module)
B	PB7 I/O (Port)	A23 output (BSC)	TEND0 output (DMAC)	IRQ7 input (INTC)	TCLKC input (MTU2)	—	SCK4 I/O (SCI)	RDWR output (BSC)

- The following amendments have been made to the explanation under 22.1.5, Port B Control Registers L1 to L4 (PBCRL1 to PBCRL4) on page 1125 in section 22, Pin Function Controller (PFC)

[Before change]

- Port B Control Register L2 (PBCRL2)

Bit	Bit Name	Initial Value	R/W	Description
14 to 12	PB7MD[2:0]	000	R/W	PB7 Mode Select the function of the PB7/A23/TEND0/IRQ7/TCLKC/SCK4 pin. 000: PB7 I/O (port) 001: A23 output (BSC) 010: TEND0 output (DMAC) 011: IRQ7 input (INTC) 100: TCLKC input (MTU2) 101: Setting prohibited 110: SCK4 I/O (SCI) 111: Setting prohibited

[After change]

- Port B Control Register L2 (PBCRL2)

Bit	Bit Name	Initial Value	R/W	Description
14 to 12	PB7MD[2:0]	000	R/W	PB7 Mode Select the function of the PB7/A23/TEND0/IRQ7/TCLKC/SCK4/RDWR pin. 000: PB7 I/O (port) 001: A23 output (BSC) 010: TEND0 output (DMAC) 011: IRQ7 input (INTC) 100: TCLKC input (MTU2) 101: Setting prohibited 110: SCK4 I/O (SCI) 111: RDWR output (BSC)

Section 23 I/O Ports

- The following amendment has been made to the explanation under 23.1.3, Port A Port Registers H and L (PAPRH and PAPRL) on page 1192 in section 23, I/O Ports.

  [Before change]
  PAPRH and PAPRL are 16-bit read-only registers, which always return the states of the pins regardless of the PFC setting.

  [After change]
  PAPRH and PAPRL are 16-bit read-only registers, which always return the states of the pins. However, when the RSPI function is selected for PA12 and when the Ethernet functions are selected for pins PA6 to PA11, the states of the corresponding pins cannot be read out.

- The following amendment has been made to figure 23.2, Port B on page 1194 in section 23, I/O Ports.

  [Before change]
  PB7 (I/O) / A23 (output) / TEND0 (output) / IRQ7 (input) / TCLKC (input) / SCK4 (I/O)

  [After change]
  PB7 (I/O) / A23 (output) / TEND0 (output) / IRQ7 (input) / TCLKC (input) / SCK4 (I/O) / RDWR (output)

- The following amendment has been made to the explanation under 23.2.3, Port B Port Register L (PBPRL) on page 1196 in section 23, I/O Ports.

  [Before change]
  PBPRL is a 16-bit read-only register, which always returns the states of the pins regardless of the PFC setting.

  [After change]
  PBPRL is a 16-bit read-only register, which always returns the states of the pins. However, when the SCIF function is selected for PB3 and when the TE bit in SCSCR and the SPB2I0 bit in SCSPTR are 0, the states of the corresponding pins cannot be read out.

- The following amendments have been made to the explanation under 23.4.3, Port D Port Registers H and L (PDPRH and PDPRL on page 1205 in section 23, I/O Ports.

  [Before change]
  PDPRH and PDPRL are 16-bit read-only registers, which always return the states of the pins regardless of the PFC setting.

  [After change]

PDPRH and PDPRL are 16-bit read-only registers, which always return the states of the pins. However, when the RSPI function is selected for PD31 and PD30, and when the Ethernet functions are selected for pins PD22 to PD20, the states of the corresponding pins cannot be read out.

- The following amendments have been made to the explanation under 23.5.3, Port E Port Register L (PEPRL) on page 1209 in section 23, I/O Ports.

  [Before change]
  PEPRL is a 16-bit read-only register, which always returns the states of the pins regardless of the PFC setting.

  [After change]
  PEPRL is a 16-bit read-only register, which always returns the states of the pins regardless of the PFC setting. However, when the RSPI function is selected for PE10 and PE8 to PE7, when the Ethernet functions are selected for pins PE15 to PE11, PE9 and PE8, PE2 and PE1, or when the SCIF function is selected for PE5 and the TE bit in SCSCR and the SPB2I0 bit in SCSPTR are 0, the states of the corresponding pins cannot be read out.

Section 27 Flash Memory (ROM)

- The following amendments have been made to the explanation under 27.1, Features on page 1437 in section 27, Flash Memory.

  [Before change]

  27.1 Features

  User Mat: 1 MB

  [After change]

  27.1 Features

  User Mat: 1 Mbyte (SH72167, SH72147)

  : 768 Kbytes (SH72166, SH72146)

  : 512 Kbytes (SH72165, SH72145)

- The following amendment has been made to the explanation under 27.6.3 FCU Command Usage on page 1512 in section 27, Flash Memory (ROM).

  [Before change]

  Figure 27.16 shows the procedure for firmware transfer to the FCU RAM. Before writing data to the FCU RAM, clear FENTRYR to H'0000 to stop the FCU. For details on the DMAC settings, refer to section 10, Direct Memory Access Controller (DMAC).

  [After change]

  Figure 27.16 shows the procedure for firmware transfer to the FCU RAM. Before writing data to the FCU RAM, clear FENTRYR to H'0000 to stop the FCU. Use the CPU or DMAC to transfer firmware to the FCU RAM. For details on setting of the DMAC, refer to section 10, Direct Memory Access Controller (DMAC).

- The following amendment has been made to the explanation under figure 27.16 Procedure for Firmware Transfer to FCU RAM on page 1513 in section 27, Flash Memory ROM.

  [Before change]

  Set DMAC

  [After change]

  Copy to the FCU RAM

Section 28 Data Flash (FLD)

- The following explanation has been added to 28.1 Features on page 1546 in section 28, Data Flash (FLD).

  [Before change]
  Reading through the peripheral bus (P bus)
  The data MAT can be read through the P bus.

  [After change]
  Reading through the peripheral bus (P bus)
  The data MAT can be read through the P bus.
  Reading program can be executed on the on-chip RAM or on-chip ROM.

- The following explanation has been added to 28.8, Usage Notes, on page 1585 in section 28, Data Flash (FLD).

  [After change]
  If a program for reading out the data flash is to be executed, execute it from the on-chip RAM or on-chip ROM.

Section 29 On-Chip RAM

- The following explanation has been added to 29.1, Features on page 1587 in section 29, On-Chip RAM.

  [Before change]
  This LSI incorporates 128-Kbyte RAM,

  [After change]
  SH7214 and SH7216 products incorporate up to 128 Kbytes of RAM.,

  29.1 Features
  - Pages

    SH72167, SH72147: 128 Kbytes Eight pages (pages 0 to 7)
    SH72166, SH72146: 96Kbytes Six pages (pages 0 to 5)
    SH72165, SH72145: 64Kbytes Four pages (pages 0 to 3)

Section 30 Power-Down Modes

- The following amendment has been made to the explanation under 30.3.3 Standby Control Register 3 (STBCR3) on page 1601 in section 30, Power-Down Modes.

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
4	MSTP34	1	R/W	Module Stop 34 When the MSTP34 bit is set to 1, the supply of the clock to the POE2 is halted. 0: POE2 runs. 1: Clock supply to POE2 halted.

[After change]

Bit	Bit Name	Initial Value	R/W	Description
4	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.

- The following has been deleted from the explanation under 30.4.4 Module Standby Function, (1) Transition to Module Standby Function on page 1611 in section 30, Power-Down Modes.

[Before change]

However, the states of the CMT and DAC registers are exceptional. In the CMT, all registers are initialized in software standby mode, but retain their previous values in module standby mode. In the DAC, all registers retain their previous values in software standby mode, but are initialized in module standby mode.

[After change]

Deleted.

Section 31 User Debugging Interface (H-UDI)

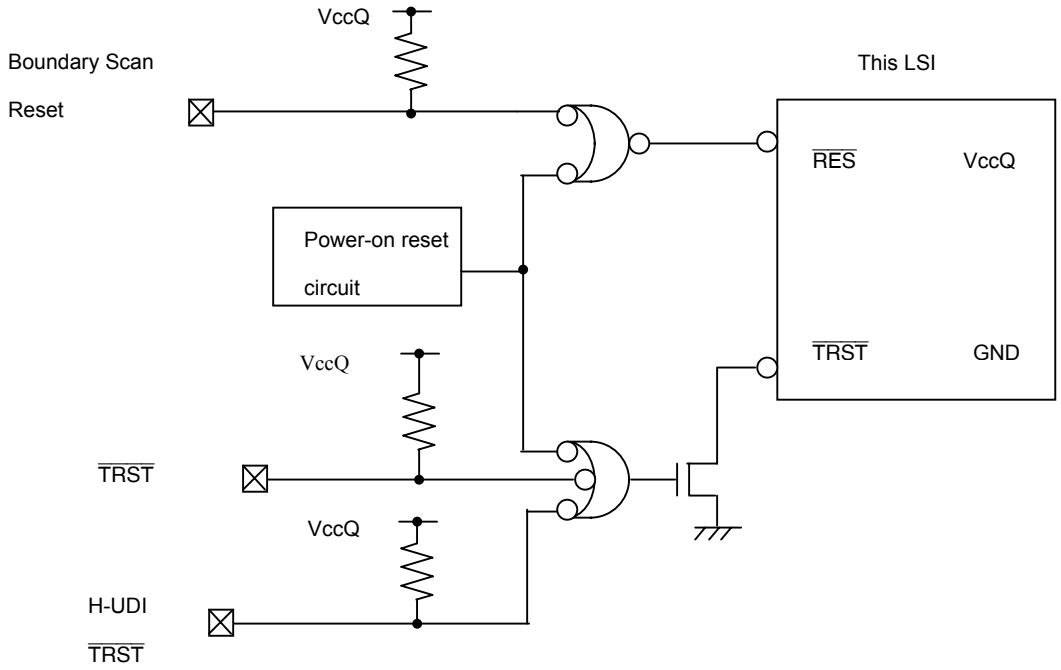
- The following has been added to the notes under 31.7 Usage Notes on 1638 in section 31, User Debugging Interface (H-UDI).

[After change]

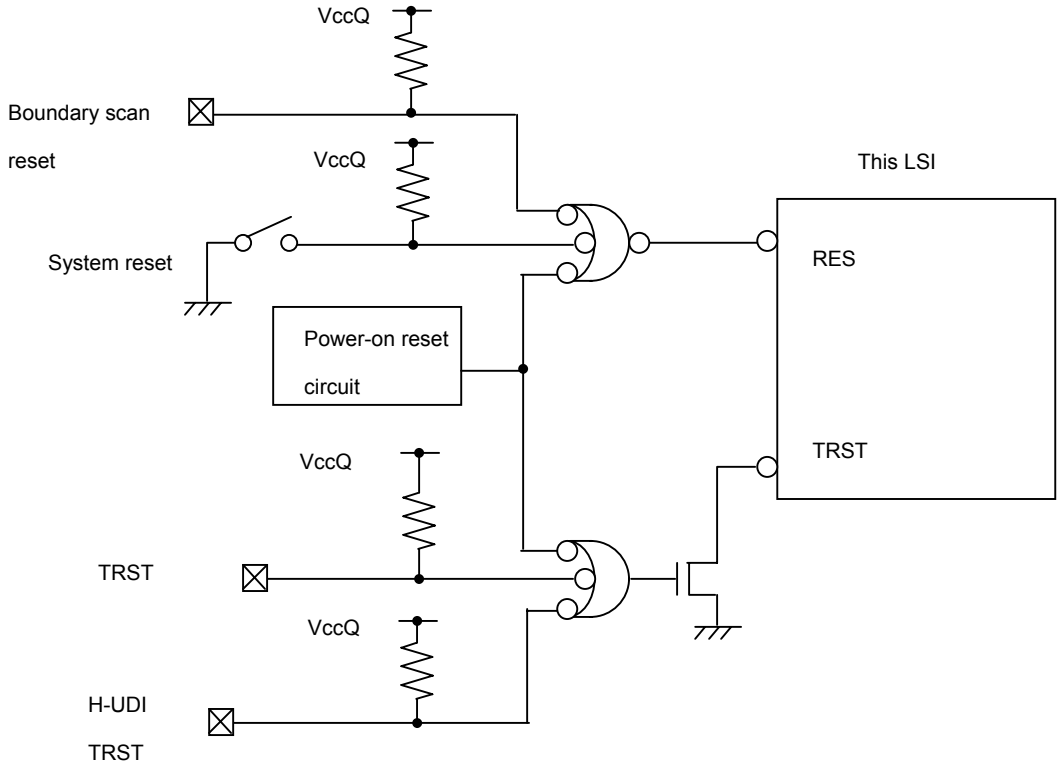
Fix the signal on the TMS pin to the high level over the period until 200 ns have elapsed after negation of the TRST signal.

- The following has been amended to figure 31.5, Peripheral Circuit Example of RST and TRST in section 31, User Debugging Interface (H-UDI).

[Before change]



[After change]



Section 32 List of Registers

- The following amendment has been made to the PFC on page 1699 and 1700 in section 32, List of Registers.

[Before change]

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
PFC	PDACKCR	—	—	—	—	—	—	—	—
		—	—	—	—	DACK3TMG	DACK2TMG	DACK1TMG	DACK0TMG
	PEPCRL	PE15PCR	PE14PCR	PE13PCR	PE12PCR	PE11PCR	PE10PCR	PE9PCR	PE8PCR
		PE7PCR	PE6PCR	PE5PCR	PE4PCR	PE3PCR	PE2PCR	PE1PCR	PE0PCR

[After change]

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
PFC	PEPCRL	PE15PCR	PE14PCR	PE13PCR	PE12PCR	PE11PCR	PE10PCR	PE9PCR	PE8PCR
		PE7PCR	PE6PCR	PE5PCR	PE4PCR	PE3PCR	PE2PCR	PE1PCR	PE0PCR
	PDACKCR	—	—	—	—	—	—	—	—
		—	—	—	—	DACK3TMG	DACK2TMG	DACK1TMG	DACK0TMG

- The following amendment has been made to the POE2 and CMT on page 1720in section 32, List of Registers.

[Before change]

Module Name	Register	Power-on Reset	Manual Reset	Software Standby	Module Standby	Sleep
POE2	ICSR1	Initialized	Retained	Retained	Retained	Retained
	OCSR1	Initialized	Retained	Retained	Retained	Retained
	ICSR2	Initialized	Retained	Retained	Retained	Retained
	OCSR2	Initialized	Retained	Retained	Retained	Retained
	ICSR3	Initialized	Retained	Retained	Retained	Retained
	SPOER	Initialized	Retained	Retained	Retained	Retained
	POECR1	Initialized	Retained	Retained	Retained	Retained
	POECR2	Initialized	Retained	Retained	Retained	Retained
CMT	CMSTR	Initialized	Retained	Initialized	Retained	Retained
	CMCSR_0	Initialized	Retained	Initialized	Retained	Retained
	CMCNT_0	Initialized	Retained	Initialized	Retained	Retained
	CMCOR_0	Initialized	Retained	Initialized	Retained	Retained
	CMCSR_1	Initialized	Retained	Initialized	Retained	Retained
	CMCNT_1	Initialized	Retained	Initialized	Retained	Retained
	CMCOR_1	Initialized	Retained	Initialized	Retained	Retained

[After change]

Module Name	Register	Power-on Reset	Manual Reset	Software Standby	Module Standby	Sleep
POE2	ICSR1	Initialized	Retained	Retained	—	Retained
	OCSR1	Initialized	Retained	Retained	—	Retained
	ICSR2	Initialized	Retained	Retained	—	Retained
	OCSR2	Initialized	Retained	Retained	—	Retained
	ICSR3	Initialized	Retained	Retained	—	Retained
	SPOER	Initialized	Retained	Retained	—	Retained
	POECR1	Initialized	Retained	Retained	—	Retained
	POECR2	Initialized	Retained	Retained	—	Retained
CMT	CMSTR	Initialized	Retained	Retained	Initialized	Retained
	CMCSR_0	Initialized	Retained	Retained	Initialized	Retained
	CMCNT_0	Initialized	Retained	Retained	Initialized	Retained
	CMCOR_0	Initialized	Retained	Retained	Initialized	Retained
	CMCSR_1	Initialized	Retained	Retained	Initialized	Retained
	CMCNT_1	Initialized	Retained	Retained	Initialized	Retained
	CMCOR_1	Initialized	Retained	Retained	Initialized	Retained

- The following amendment has been made to the RSPI on page 1722 in section 32, List of Registers.

[Before change]

Module Name	Register	Power-on Reset	Manual Reset	Software Standby	Module Standby	Sleep
RSPI	SPCR	Initialized	Retained	Retained	Retained	Retained
	SSLP	Initialized	Retained	Retained	Retained	Retained
	SPPCR	Initialized	Retained	Retained	Retained	Retained
	SPSR	Initialized	Retained	Retained	Retained	Retained
	SPDR	Initialized	Retained	Retained	Retained	Retained
	SPSCR	Initialized	Retained	Retained	Retained	Retained
	SPSSR	Initialized	Retained	Retained	Retained	Retained
	SPBR	Initialized	Retained	Retained	Retained	Retained
	SPDCR	Initialized	Retained	Retained	Retained	Retained
	SPCKD	Initialized	Retained	Retained	Retained	Retained
	SSLND	Initialized	Retained	Retained	Retained	Retained
	SPND	Initialized	Retained	Retained	Retained	Retained
	SPCMD0	Initialized	Retained	Retained	Retained	Retained
	SPCMD1	Initialized	Retained	Retained	Retained	Retained
	SPCMD2	Initialized	Retained	Retained	Retained	Retained
	SPCMD3	Initialized	Retained	Retained	Retained	Retained

[After change]

Module Name	Register	Power-on Reset	Manual Reset	Software Standby	Module Standby	Sleep
RSPI	SPCR	Initialized	Retained	Retained	Initialized	Retained
	SSLP	Initialized	Retained	Retained	Initialized	Retained
	SPPCR	Initialized	Retained	Retained	Initialized	Retained
	SPSR	Initialized	Retained	Retained	Initialized	Retained
	SPDR	Initialized	Retained	Retained	Initialized	Retained
	SPSCR	Initialized	Retained	Retained	Initialized	Retained
	SPSSR	Initialized	Retained	Retained	Initialized	Retained
	SPBR	Initialized	Retained	Retained	Initialized	Retained
	SPDCR	Initialized	Retained	Retained	Initialized	Retained
	SPCKD	Initialized	Retained	Retained	Initialized	Retained
	SSLND	Initialized	Retained	Retained	Initialized	Retained
	SPND	Initialized	Retained	Retained	Initialized	Retained
	SPCMD0	Initialized	Retained	Retained	Initialized	Retained
	SPCMD1	Initialized	Retained	Retained	Initialized	Retained
	SPCMD2	Initialized	Retained	Retained	Initialized	Retained
	SPCMD3	Initialized	Retained	Retained	Initialized	Retained

- The following amendment has been made to the RCAN-ET on page 1723 and 1724 in section 32, List of Registers.

[Before change]

Module Name	Register	Power-on Reset	Manual Reset	Software Standby	Module Standby	Sleep
RCAN-ET	MCR	Initialized	Retained	Initialized	Initialized	Retained
	GSR	Initialized	Retained	Initialized	Initialized	Retained
	BCR1	Initialized	Retained	Initialized	Initialized	Retained
	BCR0	Initialized	Retained	Initialized	Initialized	Retained
	IRR	Initialized	Retained	Initialized	Initialized	Retained
	IMR	Initialized	Retained	Initialized	Initialized	Retained
	TEC/REC	Initialized	Retained	Initialized	Initialized	Retained
	TXPR1, 0	Initialized	Retained	Initialized	Initialized	Retained
	TXCR0	Initialized	Retained	Initialized	Initialized	Retained
	TXACK0	Initialized	Retained	Initialized	Initialized	Retained
	ABACK0	Initialized	Retained	Initialized	Initialized	Retained
	RXPR0	Initialized	Retained	Initialized	Initialized	Retained
	RFPR0	Initialized	Retained	Initialized	Initialized	Retained
	MBIMR0	Initialized	Retained	Initialized	Initialized	Retained
	UMSR0	Initialized	Retained	Initialized	Initialized	Retained
	MB[0]. CONTROL0H	Initialized	Retained	Initialized	Initialized	Retained
	MB[0]. CONTROL0L	Initialized	Retained	Initialized	Initialized	Retained

[After change]

Module Name	Register	Power-on Reset	Manual Reset	Software Standby	Module Standby	Sleep
RCAN-ET	MCR	Initialized	Retained	Retained	Initialized	Retained
	GSR	Initialized	Retained	Retained	Initialized	Retained
	BCR1	Initialized	Retained	Retained	Initialized	Retained
	BCR0	Initialized	Retained	Retained	Initialized	Retained
	IRR	Initialized	Retained	Retained	Initialized	Retained
	IMR	Initialized	Retained	Retained	Initialized	Retained
	TEC/REC	Initialized	Retained	Retained	Initialized	Retained
	TXPR1, 0	Initialized	Retained	Retained	Initialized	Retained
	TXCR0	Initialized	Retained	Retained	Initialized	Retained
	TXACK0	Initialized	Retained	Retained	Initialized	Retained
	ABACK0	Initialized	Retained	Retained	Initialized	Retained
	RFPR0	Initialized	Retained	Retained	Initialized	Retained
	RFPR0	Initialized	Retained	Retained	Initialized	Retained
	MBIMR0	Initialized	Retained	Retained	Initialized	Retained
	UMSR0	Initialized	Retained	Retained	Initialized	Retained
	MB[0]. CONTROL1H	Initialized	Retained	Retained	Initialized	Retained
	MB[0]. CONTROL1L	Initialized	Retained	Retained	Initialized	Retained

Appendix

- The following amendment has been made to Appendix A. Pin States on page 1814.

[Before change]

Pin Function			Pin State						
Type	Pin Name		Reset State		Power-Down State				
			Power-On	Manual	Software Standby	Sleep	Bus Mastership Release	Oscillation Stop Detected	POE Function Used
RSPI	SSL 0		Z	I/O	K*[1]	I/O	I/O	I/O	I/O
	SSL	To SSL3	Z	O	O*[1]	O	O	O	O

[After change]

Pin Function			Pin State						
Type	Pin Name		Reset State		Power-Down State				
			Power-On	Manual	Software Standby	Sleep	Bus Mastership Release	Oscillation Stop Detected	POE Function Used
RSPI	SSL 0		Z	I/O	K*[1]	I/O	I/O	I/O	I/O
	SSL	To SSL3	Z	O	K*[1]	O	O	O	O

- The following amendments have been made to notes of Appendix A. Pin States on page 1818.

[Before change]

5. Becomes high-impedance when the MZIZDH bit in the high-current port control register (HCPCR) is set to 1.
6. Becomes high-impedance when the MZIZDL bit in the high-current port control register (HCPCR) is set to 1.
7. Becomes high-impedance when the MZIZEH bit in the high-current port control register (HCPCR) is set to 1.
8. Becomes high-impedance when the MZIZEL bit in the high-current port control register (HCPCR) is set to 1.

[After change]

5. Becomes high-impedance when the MZIZDH bit in the high-current port control register (HCPCR) is set to 0.
6. Becomes high-impedance when the MZIZDL bit in the high-current port control register (HCPCR) is set to 0.
7. Becomes high-impedance when the MZIZEH bit in the high-current port control register (HCPCR) is set to 0.
8. Becomes high-impedance when the MZIZEL bit in the high-current port control register (HCPCR) is set to 0.