The correction of errors in the I2C Bus Interface (RIIC) Hardware Manual

1. The corrections of errors in section 3.4 Master Receiver Operation

**[before]**

5. After one byte of data has been received, the RDRF flag in ICSR2 is set to 1 on the rising edge of the eighth or ninth cycle of SCL clock (the clock signal) as selected by the RDRFS bit in ICMR3. Reading out ICDRR at this time will produce the received data, and the RDRF flag is automatically cleared to 0 at the same time. Furthermore, the value of the acknowledgement field received during the ninth cycle of SCL clock is returned as the value set in the ACKBT bit of ICMR3.

6. When the next value to be received will be the final byte, set the WAIT bit in ICMR3 to 1 (so that waiting is applied) before reading ICDRR. This causes the SCLn line to be held low from the falling edge of the ninth clock cycle after reception of the next data (i.e. the final byte), enabling issuance of a stop condition. However, when the ICMR3.RDRFS bit is 0 and the slave device must be notified that it is to end transfer for data reception after transfer of the next (final) byte, set the ACKBT bit in ICMR3 to 1 (NACK).

**[after]**

5. After one byte of data has been received, the RDRF flag in ICSR2 is set to 1 on the rising edge of the eighth or ninth cycle of SCL clock (the clock signal) as selected by the RDRFS bit in ICMR3. Reading out ICDRR at this time will produce the received data, and the RDRF flag is automatically cleared to 0 at the same time. Furthermore, the value of the acknowledgement field received during the ninth cycle of SCL clock is returned as the value set in the ACKBT bit of ICMR3. Furthermore, if the next byte to be received is the next to last byte, set the ICMR3.WAIT bit to 1 (for wait insertion) before reading the ICDRR (containing the second byte from last). As well as enabling NACK output even in the case of delays in processing to set the ICMR3.ACKBT bit to 1 (NACK) in step (6), due to other interrupts etc., this fixes the SCLn line to the low level on the rising edge of the ninth clock cycle in reception of the last byte, so the state is such that issuing a stop condition is possible.

6. When the ICMR3.RDRFS bit is 0 and the slave device must be notified that it is to end transfer for data reception after transfer of the next (final) byte, set the ACKBT bit in ICMR3 to 1 (NACK).
2. The corrections of errors 「xx.3.4 Example of Master Reception Flowchart」

【before】

![Flowchart diagram]

- Master reception
- Initial settings
  - No
    - ICCR2.BSY = 0?
      - Yes
      - ICCR2.ST = 1
    - Yes
      - Write data to ICDRT
  - Yes
    - ICSR2.TDRF = 1?
      - Yes
      - ICSR2.NACKF = 0?
        - No
        - Perform dummy read of ICDRR
      - Yes
        - Perform dummy read of ICDRR
  - No
    - ICSR2.RDRF = 1?
      - Yes
      - Next data = final byte = 0?
        - Yes
        - Read ICDRR
        - ICMR3.WAIT = 1
          - Set ICMR3.ACKBT
          - Read ICDRR
        - No
          - Read ICDRR
  - Yes
    - Read final data and issue a stop condition.
    - ICSR2.STOP = 0
      - ICCR2.SP = 1
        - Read ICDRR
        - Perform dummy read of ICDRR
    - ICSR2.WAIT = 0
      - [1] Initial settings
      - [2] Check I²C bus occupation and issue a start condition.
      - [3] Transmit slave address and R and check ACK.
      - [5] Read receive data
      - [6] Prepare for receiving final data and read data of (final byte) 1 byte.
      - [7] Read final data and issue a stop condition.
      - [8] Check stop condition issuance
      - [9] Processing for the next transfer operation

Figure xx.10   Example of Master Reception Flowchart (7-Bit Address Format)
【after】

1. 初期設定
2. I2C 总线占用检查并发出开始条件。
3. 传输从机地址和 R 并检查 ACK。
4. 假读取。
5. 读取接收数据并准备接收最终数据。
6. 设置确认标志并读取数据（最终字节 - 1 字节）。
7. 读取最终数据并发出停止条件。
8. 检查停止条件的发出。
9. 对于下一个传输操作的处理。

图例 xx.10  7 位地址格式的主接收流程图
3. The corrections of errors  

**Master Receive Operation Timing (3)**

**[before]**

![Diagram of Master Receive Operation Timing (3) before](image)

**Figure xx.13** Master Receive Operation Timing (3) (when RDRFS=0)

**[after]**

![Diagram of Master Receive Operation Timing (3) after](image)

**Figure xx.13** Master Receive Operation Timing (3) (when RDRFS=0)