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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A771A/E	Rev.	1.00
Title	Correction of Errors in the Hardware Manual		Information Category	Technical Notification		
Applicable Product	SH7216 Group SH7214 Group	Lot No. All lots	Reference Document	SH7216 Group Hardware Manual (REJ09B0543-0101)		

We would like to inform you that errors have been found in the hardware manual of applicable products indicated above.

Details are given below.

1. The description on the TEND bit in section 16.3.7, Serial Status Register (SCSSR) in section 16, Serial Communication Interface (SCI) of the SH7216 Hardware Manual, was amended as follows.

[Before amendment]

Bit	Bit Name	Initial Value	R/W	Description
2	TEND	1	R	Transmit End [Clearing condition] When 0 is written to TDRE after reading TDRE = 1

[After amendment]

Bit	Bit Name	Initial Value	R/W	Description
2	TEND	1	R	Transmit End [Clearing condition] When 0 is written to TEND after reading TEND = 1

2. The following change was made to section 22, Pin Function Controller (PFC), of the SH7216 Hardware Manual: an asterisk was deleted from the entry for the PA12MD[2:0] bits in port A control register L4 (PACRL4) (section 22.1.2, Port A Control Registers H1 and H2, and L1 to L4 (PACRH1 and PACRH2, and PACRL1 to PACRL4)). Note the effect on the description of the initial value of the PA12MD[2:0] bits. Before the deletion, the initial value of bits 2 to 0 in PACRL4 was stated to be 3'b001 in the on-chip ROM disabled external expansion mode. That is, the PA12/CS0/IRQ0/TIC5U/SSL1/TX_CLK pin functioned as the CS0 output pin in that mode. After the deletion, however, the description states that the initial value of bits 2 to 0 in PACRL4 is 3'b000 regardless of the operating mode. That is, the pin functions as the PA12 I/O pin regardless of the operating mode.