To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A387A/E	Rev.	1.00
Title	Correction of Errors in H8SX/1663 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	H8SX/1663 Group	Lot No. All lots	Reference Document	H8SX/1663 Group Hardware Manual (REJ09B0294-0100)		

We would like to inform you of the correction of errors in the H8SX/1663 Group Hardware Manual as shown below.

<Corrections>

1. Overview

(1) Page 3, the function of pin no. 131 in figure 1.2, Pin Assignments

[Before Change]

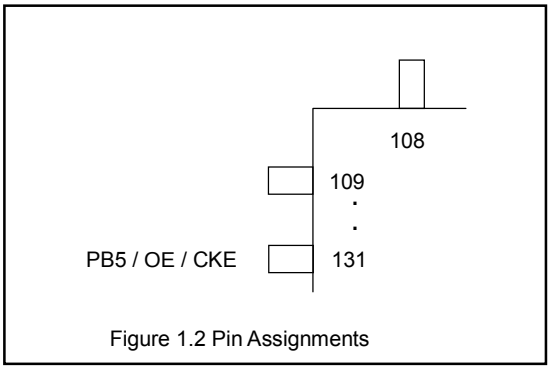

Figure 1.2 Pin Assignments

[After Change]

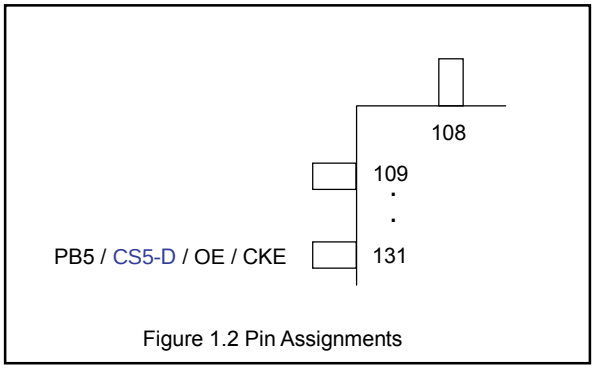

Figure 1.2 Pin Assignments

(2) Page 4, pin no. 131 in table 1.1, Pin Configuration in Each Operating Mode

[Before Change]

Pin No.	Pin Name	
	Modes 2, 6, and 7	**Modes 4 and 5**
131	PB5/OE/CKE	PB5/OE/CKE

[After Change]

Pin No.	Pin Name	
	Modes 2, 6, and 7	**Modes 4 and 5**
131	PB5/CS5-D/OE/CKE	PB5/CS5-D/OE/CKE

(3) Page 12, table 1.2, Pin Functions

[Before Change]

Classification	Abbreviation	Pin No. (FP-144LV)	I/O	Description
Bus control	CS0	144	Output	Select signals for areas 7 to 0
	CS1	1		
	CS2-A/CS2-B	2/1		
	CS3-A	3		
	CS4-A/CS4-B	144/130		
	CS5-A/CS5-B	1/144		
	CS6-A/CS6-B/CS6-D	2/1/132		
	CS7-A/CS7-B	3/1		

[After Change]

Classification	Abbreviation	Pin No. (FP-144LV)	I/O	Description
Bus control	CS0	144	Output	Select signals for areas 7 to 0
	CS1	1		
	CS2-A/CS2-B	2/1		
	CS3-A	3		
	CS4-A/CS4-B	144/130		
	CS5-A/CS5-B/CS5-D	1/144/131		
	CS6-A/CS6-B/CS6-D	2/1/132		
	CS7-A/CS7-B	3/1		

2. I/O Ports

(1) Page 436, Number of pins of port B in table 9.2, Register Configuration in Each Port

[Before Change]

Table 9.2 Register Configuration in Each Port

Port	Number of Pins	Registers					
		DDR	DR	PORT	ICR	PCR	ODR
Port B	4	O	O	O	O	—	—

[After Change]

Table 9.2 Register Configuration in Each Port

Port	Number of Pins	Registers					
		DDR	DR	PORT	ICR	PCR	ODR
Port B	8	O	O	O	O	—	—

(2) Page 480, PB3 and PB0 in table 9.5, Available Output Signals and Settings in Each Port

[Before Change]

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PB	3	CS3A_OE	CS3	PFCR2.CS3S=0	SYSCR.EXPE=1, PFCR0.CS3E=1
	0	CS4_OE	CS4		SYSCR.EXPE=1, PFCR0.CS4E=1

[After Change]

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PB	3	CS3A_OE	CS3	[Deleted]	SYSCR.EXPE=1, PFCR0.CS3E=1
	0	CS4A_OE	CS4	PFCR1.CS4S[A,B]=00	SYSCR.EXPE=1, PFCR0.CS4E=1

(3) Page 481, PE7 to PE0 in table 9.5, Available Output Signals and Settings in Each Port

[Before Change]

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PE	7	A15_OE	A15		SYSCR.EXPE=1, PDDDR.PE7DDR=1
	6	A14_OE	A14		SYSCR.EXPE=1, PDDDR.PE6DDR=1
	5	A13_OE	A13		SYSCR.EXPE=1, PDDDR.PE5DDR=1
	4	A12_OE	A12		SYSCR.EXPE=1, PDDDR.PE4DDR=1
	3	A11_OE	A11		SYSCR.EXPE=1, PDDDR.PE3DDR=1
	2	A10_OE	A10		SYSCR.EXPE=1, PDDDR.PE2DDR=1
	1	A9_OE	A9		SYSCR.EXPE=1, PDDDR.PE1DDR=1
	0	A8_OE	A8		SYSCR.EXPE=1, PDDDR.PE0DDR=1

[After Change]

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PE	7	A15_OE	A15		SYSCR.EXPE=1, PEDDR.PE7DDR=1
	6	A14_OE	A14		SYSCR.EXPE=1, PEDDR.PE6DDR=1
	5	A13_OE	A13		SYSCR.EXPE=1, PEDDR.PE5DDR=1
	4	A12_OE	A12		SYSCR.EXPE=1, PEDDR.PE4DDR=1
	3	A11_OE	A11		SYSCR.EXPE=1, PEDDR.PE3DDR=1
	2	A10_OE	A10		SYSCR.EXPE=1, PEDDR.PE2DDR=1
	1	A9_OE	A9		SYSCR.EXPE=1, PEDDR.PE1DDR=1
	0	A8_OE	A8		SYSCR.EXPE=1, PEDDR.PE0DDR=1

(4) Page 485, description of bits 1 and 0 in PFCR1

[Before Change]

Bit	Bit Name	Initial Value	R/W	Description
7	CS7SA*	0	R/W	[No change]
6	CS7SB*	0	R/W	
5	CS6SA*	0	R/W	
4	CS6SB*	0	R/W	
3	CS5SA*	0	R/W	
2	CS5SB*	0	R/W	
1	CS4SA*	0	R/W	CS4 Output Pin Select
0	CS4SB*	0	R/W	Selects the output pin for CS4 when CS4 output is enabled (CS4E = 1) 00: Specifies pin PB1 as CS4-A output 01: Specifies pin PB0 as CS4-B output 10: Setting prohibited 11: Setting prohibited

[After Change]

Bit	Bit Name	Initial Value	R/W	Description
7	CS7SA*	0	R/W	[No change]
6	CS7SB*	0	R/W	
5	CS6SA*	0	R/W	
4	CS6SB*	0	R/W	
3	CS5SA*	0	R/W	
2	CS5SB*	0	R/W	
1	CS4SA*	0	R/W	CS4 Output Pin Select
0	CS4SB*	0	R/W	Selects the output pin for CS4 when CS4 output is enabled (CS4E = 1) 00: Specifies pin PB0 as CS4-A output 01: Specifies pin PB4 as CS4-B output 10: Setting prohibited 11: Setting prohibited

3. Watchdog Timer

(1) Page 645, the clearing condition of the WOVF bit in RSTCSR

[Before Change]

Bit	Bit Name	Initial Value	R/W	Description
7	WOVF	0	R/W	Watchdog Timer Overflow Flag This bit is set when TCNT overflows in watchdog timer mode. This bit cannot be set in interval timer mode, and only 0 can be written. [Setting condition] When TCNT overflows (changed from H'FF to H'00) in watchdog timer mode [Clearing condition] Reading RSTCSR when WOVF = 1, and then writing 0 to WOVF (When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.)
6	RSTE	0	R/W	[No change]
5	—	0	R/W	
4 to 0	—	1	R	

[After Change]

Bit	Bit Name	Initial Value	R/W	Description
7	WOVF	0	R/W	Watchdog Timer Overflow Flag This bit is set when TCNT overflows in watchdog timer mode. This bit cannot be set in interval timer mode, and only 0 can be written. [Setting condition] When TCNT overflows (changed from H'FF to H'00) in watchdog timer mode [Clearing condition] Reading RSTCSR when WOVF = 1, and then writing 0 to WOVF [Deleted]
6	RSTE	0	R/W	[No change]
5	—	0	R/W	
4 to 0	—	1	R	

4. Serial Communication Interface

(1) Page 671, the name of bit 4 in the serial status register (SSR)

[Before Change]

• When SMIF in SCMR = 0

Bit	7	6	5	4	3	2	1	0
Bit name	TDRE	RDRF	ORER	FRE	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
R/W	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

[After Change]

• When SMIF in SCMR = 0

Bit	7	6	5	4	3	2	1	0
Bit name	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
R/W	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

(2) Page 681, table 15.3, Relationships between N Setting in BRR and Bit Rate B

[Before Change]

Mode	ABCS Bit	Bit Rate	Error
Asynchronous mode	0	$B = \frac{P\phi \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	[No change]
	1	$B = \frac{P\phi \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	

[After Change]

Mode	ABCS Bit	Bit Rate	Error
Asynchronous mode	0	$N = \frac{P\phi \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	[No change]
	1	$N = \frac{P\phi \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	

5. Clock Pulse Generator

(1) Page 961, the name of bit 0 in SUBCKCR

[Before Change]

Subclock control register (SUBCKCR)

Bit	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	-	EXSTP	WAKE32K	CS32K
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[After Change]

Subclock control register (SUBCKCR)

Bit	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	-	EXSTP	WAKE32K	CK32K
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6. Power-Down Modes

(1) Page 972, note 4 for table 23.1, Operating States

[Before Change]

4. "Functioning" or "Halted" is selectable through the setting of bits MSTPA9 and MSTPA8 in MSTPCRA. However, pin output is disabled even when "Functioning" is selected.

[After Change]

4. "Functioning" or "Halted" is selectable through the setting of bits MSTPA9 and MSTPA8 in MSTPCRA. [Deleted]