To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A407A/E	Rev.	1.00
Title	Correction of errors in the H8SX/1658R and H8SX/1658M Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	H8SX/1658R and H8SX/1658M Group	Lot No. All lots	Reference Document	H8SX/1658R Group, H8SX/1658M Group Hardware Manual (REJ09B0413-0200)		

We would like to inform you of the correction of errors in the above listed hardware manuals. Please refer to the following for details.

<Corrections>

Section7 Interrupt Controller

Deletion of DTCERG, and DTCERH

(1) Page 156, 7.6.5 DTC and DMAC Activation by Interrupt

[Before Change]

(1) Selection of Interrupt Sources

The activation source for each DMAC channel is selected by DMRSR. The selected activation source is input to the DMAC through the select circuit. When transfer by an on-chip module interrupt is enabled (DTF1 = 1, DTF0 = 0, and DTE = 1 in DMDR) and the DTA bit in DMDR is set to 1, the interrupt source selected for the DMAC activation source is controlled by the DMAC and cannot be used as a DTC activation source or CPU interrupt source.

Interrupt sources that are not controlled by the DMAC are set for DTC activation sources or CPU interrupt sources by the DTCE bit in DTCERA to DTCERH of the DTC.

- Description omitted (no changes) –

[After Change]

(1) Selection of Interrupt Sources

The activation source for each DMAC channel is selected by DMRSR. The selected activation source is input to the DMAC through the select circuit. When transfer by an on-chip module interrupt is enabled (DTF1 = 1, DTF0 = 0, and DTE = 1 in DMDR) and the DTA bit in DMDR is set to 1, the interrupt source selected for the DMAC activation source is controlled by the DMAC and cannot be used as a DTC activation source or CPU interrupt source.

Interrupt sources that are not controlled by the DMAC are set for DTC activation sources or CPU interrupt sources by the DTCE bit in DTCERA to **DTCERF** of the DTC.

- Description omitted (no changes) –

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(2) Page 157, 7.6.5 DTC and DMAC Activation by Interrupt

[Before Change]

(3) Operation Order

- Description omitted (no changes) –

Table 7.6 lists the selection of interrupt sources and interrupt source clear control by setting the DTA bit in DMDR of the DMAC, the DTCE bit in DTCERA to DTCERH of the DTC, and the DISEL bit in MRB of the DTC.

[After Change]

(3) Operation Order

- Description omitted (no changes) –

Table 7.6 lists the selection of interrupt sources and interrupt source clear control by setting the DTA bit in DMDR of the DMAC, the DTCE bit in DTCERA to **DTCERF** of the DTC, and the DISEL bit in MRB of the DTC.

Section 13 I/O Ports

(1) Page 510, table 13.2

[Before Change]

Port	Number of Pins	Registers					
		DDR	DR	PORT	ICR	PCR	ODR
Ports 1 to 5		– Description omitted (no changes) –					
Port 6	6	O	O	O	O	—	—
Port A	8	O	O	O	O	—	—
Port B	4	O	O	O	O	—	—
Ports D*1 to E*1		– Description omitted (no changes) –					
Port F	5	O	O	O	O	O	O
Ports H to K*2		– Description omitted (no changes) –					
Port M	5	O	O	O	O	—	—

[Legend]

O: Register exists

– : No register exists

Notes: 1. Do not access port D or E registers when PCJKE = 1.

2. Do not access port J or K registers when PCJKE = 0.

[After Change]

Port	Number of Pins	Registers					
		DDR	DR	PORT	ICR	PCR	ODR
Ports 1 to 5		– Description omitted (no changes) –					
Port 6*3	6	O	O	O	O	—	—
Port A	8	O	O	O	O	—	—
Port B*4	4	O	O	O	O	—	—
Ports D*1 to E*1		– Description omitted (no changes) –					
Port F*5	5	O	O	O	O	O	O
Ports H to K*2		– Description omitted (no changes) –					
Port M*6	5	O	O	O	O	—	—

[Legend]

O: Register exists

– : No register exists

Notes: 1. Do not access port D or E registers when PCJKE = 1.

2. Do not access port J or K registers when PCJKE = 0.

3. For port 6, only the six lower-order bits are valid (the two higher-order bits are reserved). The write value should always be the initial value.

4. For port B, only the four lower-order bits are valid (the four higher-order bits are reserved). The write value should always be the initial value.

5. For port F, only the five lower-order bits are valid (the three higher-order bits are reserved). The write value should always be the initial value.

6. For port M, only the five lower-order bits are valid (the three higher-order bits are reserved). The write value should always be the initial value.

Section 21 A/D Converter

(1) Page984, table21.3 A/D Conversion Characteristics (EXCKS1 = 0), Table 21.4 A/D Conversion Characteristics (EXCKS1 = 1: Unit 1)

[Before Change]

Table 21.3 A/D Conversion Characteristics (EXCKS1 = 0)

		CKS1=0						CKS1=1					
		CKS=0			CKS=1			CKS=0			CKS=1		
Item	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
A/D conversion start delay time	t_D	4	—	14	4	—	10	4	—	8	3	—	7
Input sampling time	t_{SPL}	—	312	—	—	156	—	—	78	—	—	39	—
A/D conversion time	t_{CONV}	518	—	528	262	—	268	134	—	138	69	—	73

Table 21.4 A/D Conversion Characteristics (EXCKS1 = 1: Unit 1)

		CKS1=0						CKS1=1					
		CKS=0			CKS=1			CKS=0			CKS=1		
Item	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
A/D conversion start delay time	t_D	4	—	14	4	—	10	4	—	8	3	—	7
Input sampling time	t_{SPL}	—	120	—	—	60	—	—	30	—	—	15	—
A/D conversion time	t_{CONV}	326	—	336	166	—	172	86	—	90	45	—	49

[After Change]

Table 21.3 A/D Conversion Characteristics (**Unit 0**)

		CKS1=0						CKS1=1					
		CKS0=0			**CKS0=1**			**CKS0=0**			**CKS0=1**		
Item	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
A/D conversion start delay time	t_D	**3**	—	14	**3**	—	10	**3**	—	8	3	—	7
Input sampling time	t_{SPL}	—	312	—	—	156	—	—	78	—	—	39	—
A/D conversion time	t_{CONV}	**517**	—	528	**261**	—	268	**133**	—	138	69	—	73

Table 21.4.1 A/D Conversion Characteristics (Unit 1: EXCKS = 0)

		CKS1=0						**CKS1=1**					
		CKS0=0			**CKS0=1**			**CKS0=0**			**CKS0=1**		
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A/D conversion start delay time	**t_D**	**4**	**—**	**14**	**4**	**—**	**10**	**4**	**—**	**8**	**4**	**—**	**7**
Input sampling time	**t_{SPL}**	**—**	**312**	**—**	**—**	**156**	**—**	**—**	**78**	**—**	**—**	**39**	**—**
A/D conversion time	**t_{CONV}**	**518**	**—**	**528**	**262**	**—**	**268**	**134**	**—**	**138**	**70**	**—**	**73**

Table 21.4.**2** A/D Conversion Characteristics (**Unit 1: EXCKS = 1**)

		CKS1=0						CKS1=1					
		CKS0=0			**CKS0=1**			**CKS0=0**			**CKS0=1**		
Item	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
A/D conversion start delay time	t_D	4	—	14	4	—	10	4	—	8	**4**	—	7
Input sampling time	t_{SPL}	—	120	—	—	60	—	—	30	—	—	15	—
A/D conversion time	t_{CONV}	326	—	336	166	—	172	86	—	90	**46**	—	49

Section 29 Electrical Characteristics

(1) Page1251, table29.2 DC Characteristics (2)

[Before Change]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Tree-state leakage current (off state)	Ports 1,2,**3,**6 A to F,H to K,M			– Description omitted (no changes) –			

[After Change]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Tree-state leakage current (off state)	Ports 1,2,6,**A,B, D** to F,H to K,M			– Description omitted (no changes) –			

(2) Page1255, table29.4 DC Characteristics (2)

[Before Change]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Tree-state leakage current (off state)	Ports 1,2,6,A,B, C to F,H ,I,J,K,M			– Description omitted (no changes) –			

[After Change]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Tree-state leakage current (off state)	Ports 1,2,6,**A,B, D** to F,H to K,M			– Description omitted (no changes) –			

(3) Page1263, table29.8 Bus Timing (1)

[Before Change]

Item	Symbol	Min.	Max.	Unit	Test Conditions
Read data access time (from address)4	t_{AA4}		2.5 x t_{cyc} - 20	ns	– Description omitted (no changes) –

[After Change]

Item	Symbol	Min.	Max.	Unit	Test Conditions
Read data access time (from address)4	t_{AA4}	—	2.5 x t_{cyc} - 20	ns	– Description omitted (no changes) –