To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Mar.10.2009

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-H8*-A406A/E	Rev.	1.00
Title	Correction of errors in the H8SX/1657 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	H8SX/1657 Group	Lot No. All lots	Reference Document	H8SX/1657 Group Hardware Manual (REJ09B0341-0200)		

We would like to inform you of the correction of errors in the above hardware manuals. Please refer to the following for details.

<Corrections>

Section 1 Overview

(1) Page 2, table 1.1, Overview of Functions

[Before Change]

Classification	Module/ Function	Description
CPU	CPU	- Description omitted (no changes) - • Supports multiply-and-accumulate instructions (16 × 16 + 32 → 32 bits)

[After Change]

Classification	Module/ Function	Description
CPU	CPU	- Description omitted (no changes) - • Supports multiply-and-accumulate instructions (**16 × 16 + 42 → 42 bits**)

Section 5 Interrupt Controller

Deletion of DTCERF, DTCERG, and DTCERH
(1) Page 120 to 121, 5.6.5 DTC and DMAC Activation by Interrupt

[Before Change]

(1) Selection of Interrupt Sources

The activation source for each DMAC channel is selected by DMRSR. The selected activation source is input to the DMAC through the select circuit. When transfer by an on-chip module interrupt is enabled (DTF1 = 1, DTF0 = 0, and DTE = 1 in DMDR) and the DTA bit in DMDR is set to 1, the interrupt source selected for the DMAC activation source is controlled by the DMAC and cannot be used as a DTC activation source or CPU interrupt source.

Interrupt sources that are not controlled by the DMAC are set for DTC activation sources or CPU interrupt sources by the DTCE bit in DTCERA to DTCERH of the DTC.

- Description omitted (no changes) –

(2) Priority Determination

- Description omitted (no changes) –

(3) Operation Order

- Description omitted (no changes) –

Table 5.6 lists the selection of interrupt sources and interrupt source clear control by setting the DTA bit in DMDR of the DMAC, the DTCE bit in DTCERA to DTCERH of the DTC, and the DISEL bit in MRB of the DTC.

[After Change]

(1) Selection of Interrupt Sources

The activation source for each DMAC channel is selected by DMRSR. The selected activation source is input to the DMAC through the select circuit. When transfer by an on-chip module interrupt is enabled (DTF1 = 1, DTF0 = 0, and DTE = 1 in DMDR) and the DTA bit in DMDR is set to 1, the interrupt source selected for the DMAC activation source is controlled by the DMAC and cannot be used as a DTC activation source or CPU interrupt source.

Interrupt sources that are not controlled by the DMAC are set for DTC activation sources or CPU interrupt sources by the DTCE bit in DTCERA to **DTCERE** of the DTC.

- Description omitted (no changes) –

(2) Priority Determination

- Description omitted (no changes) –

(3) Operation Order

- Description omitted (no changes) –

Table 5.6 lists the selection of interrupt sources and interrupt source clear control by setting the DTA bit in DMDR of the DMAC, the DTCE bit in DTCERA to **DTCERE** of the DTC, and the DISEL bit in MRB of the DTC.

Section 7 DMA Controller (DMAC)

(1) Page 242, description of bits 31 to 0's initial values in DBSR

[Before Change]

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	BKSZH31 to BKSZH16	Undefined	R/W	Description omitted (no changes)
15 to 0	BKSZ15 to BKSZ0	Undefined	R/W	Description omitted (no changes)

[After Change]

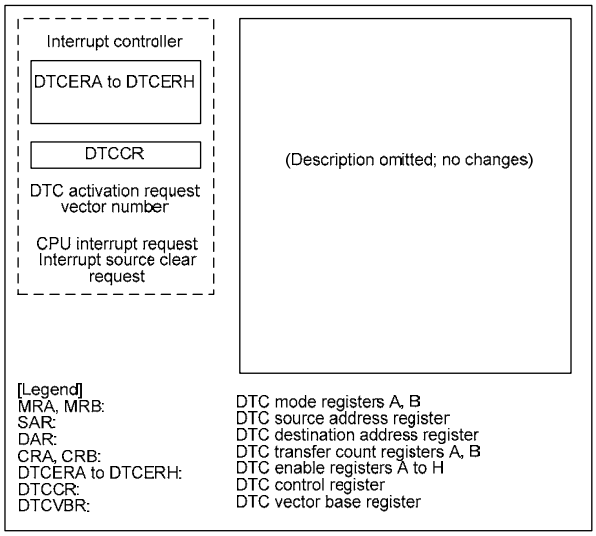
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	BKSZH31 to BKSZH16	**0**	R/W	Description omitted (no changes)
15 to 0	BKSZ15 to BKSZ0	**0**	R/W	Description omitted (no changes)

Section 8 Data Transfer Controller

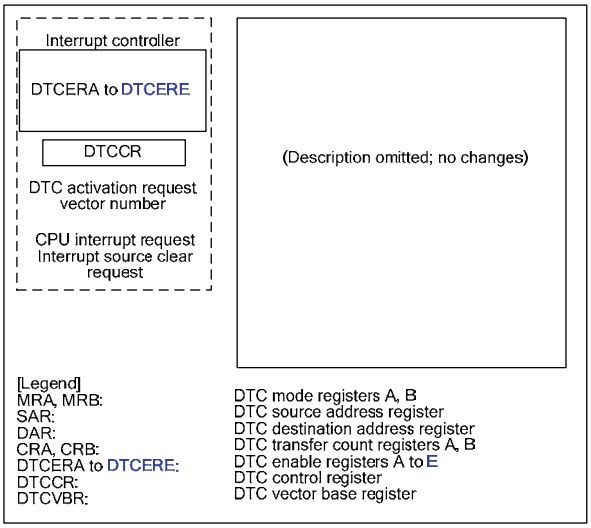
Deletion of DTCERF, DTCERG, and DTCERH

(1) Page 308, the DTCER description in figure 8.1 Block Diagram of DTC

[Before Change]



[After Change]



(2) Page 309, section 8.2 Register Descriptions

Deletion of DTCERF, DTCERG, and DTCERH in DTCER

[Before Change]

- DTC enable registers A to H (DTCERA to DTCERH)

[After Change]

- DTC enable registers A to **E** (DTCERA to **DTCERE**)

(3) Page 315, section 8.2.7, DTC Enable Registers A to H (DTCERA to DTCERE)

[Before Change]

8.2.7, DTC enable registers A to H (DTCERA to DTCERE)

DTCER which is comprised of eight registers, DTCERA to DTCERE, is a register that specifies DTC activation interrupt sources. (further description omitted)

[After Change]

8.2.7, DTC Enable Registers A to **E** (DTCERA to DTCERE)

DTCER which is comprised of **five** registers, DTCERA to DTCERE, is a register that specifies DTC activation interrupt sources.(further description omitted)

Section 9 I/O Ports

(1) Page 389, table 9.5, Available Output Signals and Settings in Each Port

[Before Change]

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PA	1	$\overline{\text{BACK}}$_OE	$\overline{\text{BACK}}$		SYSCRE.EXPE = 1, BCR1.BRLE = 1
		(RD/$\overline{\text{WR}}$)_OE	RD/$\overline{\text{WR}}$		SYSCR.EXPE = 1, PFCR2.REWRE = 1 or SRAMCR.BCSELn = 1

[After Change]

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PA	1	$\overline{\text{BACK}}$_OE	$\overline{\text{BACK}}$		SYSCRE.EXPE = 1, BCR1.BRLE = 1
		(RD/$\overline{\text{WR}}$)_OE	RD/$\overline{\text{WR}}$		SYSCR.EXPE = 1, PFCR2.**RDWRE** = 1 or SRAMCR.BCSELn = 1

(2) Pages 397 and 398, description of bits 7 to 4 in PFCR7

[Before Change]

Bit	Bit Name	Initial Value	R/W	Description
7	DMAS3A	0	R/W	DMAC control pin select
6	DMAS3B	0	R/W	Selects the I/O port to control DMAC_3. 00: Setting prohibited 01: Specifies pins P63 to P65 as DMAC control pins 10: Setting prohibited 11: Setting prohibited
5	DMAS2A	0	R/W	DMAC control pin select
4	DMAS2B	0	R/W	Selects the I/O port to control DMAC_2. 00: Setting prohibited 01: Specifies pins P60 to P62 as DMAC control pins 10: Setting prohibited 11: Setting prohibited

[After Change]

Bit	Bit Name	Initial Value	R/W	Description
7	DMAS3A	0	R/W	DMAC control pin select
6	DMAS3B	0	R/W	Selects the I/O port to control DMAC_3. 00: **Setting ignored (Pins P63 to P65 cannot be used as DMAC control pins.)** 01: Specifies pins P63 to P65 as DMAC control pins 10: Setting prohibited 11: Setting prohibited
5	DMAS2A	0	R/W	DMAC control pin select
4	DMAS2B	0	R/W	Selects the I/O port to control DMAC_2. 00: **Setting ignored (Pins P60 to P62 cannot be used as DMAC control pins.)** 01: Specifies pins P60 to P62 as DMAC control pins 10: Setting prohibited 11: Setting prohibited

Section 12 8-Bit Timers (TMR)

(1) Page 532, description in Section 12.7.2, A/D Converter Activation, is corrected as follows.

[Before Change]

The A/D converter can be activated only by TMR_0 compare match A.

If the ADTE bit in TCSR_0 is set to 1 when the CMFA flag in TCSR_0 is set to 1 by the occurrence of TMR_0 compare match A, a request to start A/D conversion is sent to the A/D converter. If the 8-bit timer conversion start trigger has been selected on the A/D converter side at this time, A/D conversion is started.

[After Change]

The A/D converter can be activated only **by TMR_0 or TMR_2 compare match A.**

If the ADTE bit in TCSR_0 is set to 1 when the CMFA flag in TCSR_0 is set to 1 **by the occurrence of compare match A**, a request to start A/D conversion is sent to the A/D converter. If the 8-bit timer conversion start trigger has been selected on the A/D converter side at this time, A/D conversion is started.

Section 14 Serial Communication Interface (SCI)

(1) Page 564, the name of bit 4 in Serial Status Register (SSR)

[Before Change]

Serial Status Register (SSR)

- When SMIF in SCMR = 0

Bit	7	6	5	4	3	2	1	0
Bit Name	TDRE	RDRF	ORER	FRE	PER	TEND	MPB	MPBT
Initial Value	1	0	0	0	0	1	0	0
R/W	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Only 0 can be written, to clear the flag.

[After Change]

- When SMIF in SCMR = 0

Bit	7	6	5	4	3	2	1	0
Bit Name	TDRE	RDRF	ORER	**FER**	PER	TEND	MPB	MPBT
Initial Value	1	0	0	0	0	1	0	0
R/W	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Only 0 can be written, to clear the flag.

Section 20 Power-Down Modes

(1) Page 762, description of bit 13 in MSTPCRA is corrected as follows.

[Before Change]

Bit	Bit Name	Initial Value	R/W	Module
14	MSTPA14	0	R/W	Reserved
13	MSTPA13	0	R/W	These bits are always read as 0. The write value should always be 0

[After Change]

Bit	Bit Name	Initial Value	R/W	Module
14	MSTPA14	0	R/W	Reserved This bit is always read as 0. The write value should always be 0
13	**MSTPA13**	**0**	**R/W**	**DMA controller (DMAC)**