To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A401A/E	Rev.	1.00
Title	Correction of errors in the H8SX/1648, H8SX/1648A, H8SX/1648L, H8SX/1648G, and H8SX/1648H Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	H8SX/1648, H8SX/1648A, H8SX/1648L, H8SX/1648G, and H8SX/1648H Group	Lot No. All lots	Reference Document	H8SX/1648, H8SX/1648A, H8SX/1648L, H8SX/1648G, and H8SX/1648H Group Hardware Manual (REJ09B0365-0200)		

We would like to inform you of the correction of errors in the above listed hardware manuals. Please refer to the following for details.

<Corrections>

Section 7 Interrupt Controller

(1) Page 148, section 7.4.1 External Interrupts, (1) NMI Interrupts

[Before Change]

- Sets the ERR bit of DTCCR in the DTC to 1
- Sets the ERRF bit of DMDR_0 in the DMAC to 1
- Sets the ERRF bit of DMDR_0 in the EXDMAC* to 1
- Clears the DTE bits of DMDRs for all channels in the DMAC to 0 to forcibly terminate transfer
- Clears the DTE bits of DMDRs for all channels in the EXDMAC* to 0 to forcibly terminate transfer

Note: * Supported only by the H8SX/1648G and H8SX/1648H groups.

[After Change]

- Sets the ERR bit of DTCCR in the DTC to 1
- Sets the ERRF bit of DMDR_0 in the DMAC to 1
- Sets the ERRF bit of **EDMDR_0** in the EXDMAC* to 1
- Clears the DTE bits of DMDRs for all channels in the DMAC to 0 to forcibly terminate transfer
- Clears the DTE bits of **EDMDRs** for all channels in the EXDMAC* to 0 to forcibly terminate transfer

Note: * Supported only by the H8SX/1648G and H8SX/1648H groups.

(2) Page 163 to 164, 7.6.5 DTC and DMAC Activation by Interrupt

[Before Change]

(1) Selection of Interrupt Sources

The activation source for each DMAC channel is selected by DMRSR. The selected activation source is input to the DMAC through the select circuit. When transfer by an on-chip module interrupt is enabled (DTF1 = 1, DTF0 = 0, and DTE = 1 in DMDR) and the DTA bit in DMDR is set to 1, the interrupt source selected for the DMAC activation source is controlled by the DMAC and cannot be used as a DTC activation source or CPU interrupt source.

Interrupt sources that are not controlled by the DMAC are set for DTC activation sources or CPU interrupt sources by the DTCE bit in DTCERA to DTCERH of the DTC.

- Description omitted (no changes) –

(2) Priority Determination

- Description omitted (no changes) –

(3) Operation Order

- Description omitted (no changes) –

Table 7.6 lists the selection of interrupt sources and interrupt source clear control by setting the DTA bit in DMDR of the DMAC, the DTCE bit in DTCERA to DTCERH of the DTC, and the DISEL bit in MRB of the DTC.

[After Change]

(1) Selection of Interrupt Sources

The activation source for each DMAC channel is selected by DMRSR. The selected activation source is input to the DMAC through the select circuit. When transfer by an on-chip module interrupt is enabled (DTF1 = 1, DTF0 = 0, and DTE = 1 in DMDR) and the DTA bit in DMDR is set to 1, the interrupt source selected for the DMAC activation source is controlled by the DMAC and cannot be used as a DTC activation source or CPU interrupt source.

Interrupt sources that are not controlled by the DMAC are set for DTC activation sources or CPU interrupt sources by the DTCE bit in DTCERA to **DTCERF** of the DTC.

- Description omitted (no changes) –

(2) Priority Determination

- Description omitted (no changes) –

(3) Operation Order

- Description omitted (no changes) –

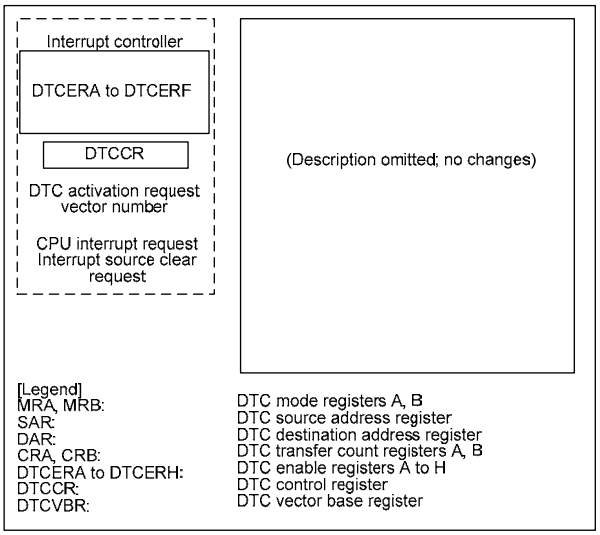
Table 7.6 lists the selection of interrupt sources and interrupt source clear control by setting the DTA bit in DMDR of the DMAC, the DTCE bit in DTCERA to **DTCERF** of the DTC, and the DISEL bit in MRB of the DTC.

Section 12 Data Transfer Controller

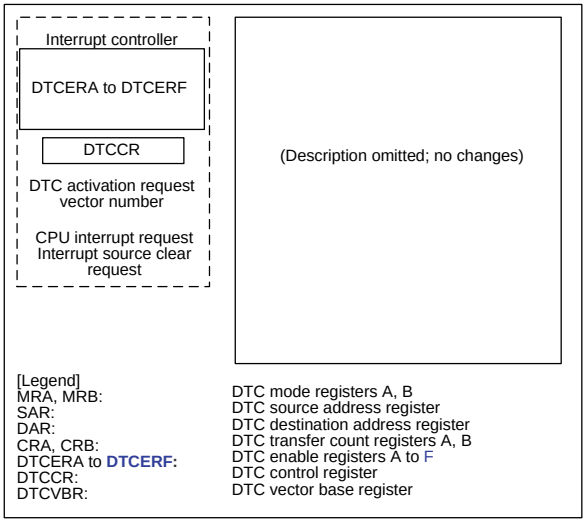
Deletion of DTCERG, and DTCERH in DTCER

(1) Page 568, DTCER description in figure 12.1, Block Diagram of DTC

[Before Change]



[After Change]



(2) Page 574, section 12.2.7, DTC Enable Register

Deletion of DTCERG, and DTCERH in DTCER

[Before Change]

12.2.7 DTC enable registers A to H (DTCERA to DTCERH)

DTCER, which is comprised of eight registers, DTCERA to DTCERH, is a register that specifies DTC activation interrupt sources.

[After Change]

12.2.7 DTC Enable Register A to **F** (DTCERA to **DTCERF**)

DTCER, which is comprised of **six** registers, DTCERA to **DTCERF**, is a register that specifies DTC activation interrupt sources.

Section 13 I/O Ports

(1) Page 613, table 13.2 Register Configuration in Each Port

[Before Change]

Port	Number of Pins	Registers					
		DDR	DR	PORT	ICR	PCR	ODR
Ports 1 to 3			- Description omitted (no changes) -				
Port 4	4	—	—	O	O	—	—
Ports 5 to B			- Description omitted (no changes) -				
Port C*1	6	O	O	O	O	—	—
Ports D*2 to K *3			- Description omitted (no changes) -				
Port M*4	5	O	O	O	O	—	—
Port N	4	O	O	O	O	—	—

[Legend]

O: Register exists

－: No register exists

Note : 1. Write the initial value to any of bits in port C registers.

2. Do not access port D or E registers when PCJKE=1.

3. Do not access port J or K registers when PCJKE=0.

4. Supported only by the H8SX/1648G Group and H8SX/1648H Group.

[After Change]

Port	Number of Pins	Registers					
		DDR	DR	PORT	ICR	PCR	ODR
Ports 1 to 3			- Description omitted (no changes) -				
Port 4*5	4	—	—	O	O	—	—
Ports 5 to B			- Description omitted (no changes) -				
Port C*1	6	O	O	O	O	—	—
Ports D*2 to K *3			- Description omitted (no changes) -				
Port M*4,*6	5	O	O	O	O	—	—
Port N*7	4	O	O	O	O	—	—

[Legend]

O: Register exists

－: No register exists

Note: 1. For port C, only the six lower-order bits are valid (the two higher-order bits are reserved). The write value should always be the initial value.

2. Do not access port D or E registers when PCJKE=1.

3. Do not access port J or K registers when PCJKE=0.

4. Supported only by the H8SX/1648G Group and H8SX/1648H Group.

5. For port 4, only the four higher-order bits are valid (the four lower-order bits are reserved). The write value should always be the initial value.

6. For port M, only the five lower-order bits are valid (the three higher-order bits are reserved). The write value should always be the initial value.

7. For port N, only the four lower-order bits are valid (the four higher-order bits are reserved). The write value should always be the initial value.

(2) Pages 642 and 644,section 13.2.7, PB7 and PB4 in port B

[Before Change]

(1) PB7/$\overline{\text{CS7}}$-D/SDϕ[*3]

		Setting		
		MCU Operating Mode	Bus Controller	I/O Port
Module Name	Pin Function	SDRAM	$\overline{\text{CS7D}}$_OE	PB7DDR
- Description omitted (no changes) -				

(4) PB4/$\overline{\text{CS4}}$-B/$\overline{\text{WE}}$[*2]

		Setting		
		Bus Controller	I/O Port	Bus Controller
Module Name	Pin Function	$\overline{\text{WE}}$_OE	$\overline{\text{CS4B}}$_OE	PB4DDR
- Description omitted (no changes) -				

[After Change]

(1) PB7/$\overline{\text{CS7}}$-D/SDϕ[*3]

		Setting		
		MCU Operating Mode	I/O Port	
Module Name	Pin Function	SDRAM	$\overline{\text{CS7D}}$_OE	PB7DDR
- Description omitted (no changes) -				

(4) PB4/$\overline{\text{CS4}}$-B/$\overline{\text{WE}}$[*2]

		Setting		
		Bus Controller	I/O Port	
Module Name	Pin Function	$\overline{\text{WE}}$_OE	$\overline{\text{CS4B}}$_OE	PB4DDR
- Description omitted (no changes) -				

Section 21 A/D Converter

(1) Page 1037, section 21.3.5 A/D Control Register (ADCR_0) Unit 0, bits 3 and 2

[Before Change]

Bit	Bit Name	Initial Value	R/W	Description
3	CKS1	0	R/W	Clock Select 1 and 0
2	CKS0	0	R/W	- Description omitted (no changes) -
				CKS1, and CKS0
				00: A/D conversion time = 530 states*3 (max.)
				01: A/D conversion time = 266 states*3 (max.)
				10: A/D conversion time = 134 states*3 (max.)
				11: A/D conversion time = 68 states*3 (max.)

[After Change]

Bit	Bit Name	Initial Value	R/W	Description
3	CKS1	0	R/W	Clock Select 1 and 0
2	CKS0	0	R/W	- Description omitted (no changes) -
				CKS1, and CKS0
				00: A/D conversion time = **528** states*3 (max.)
				01: A/D conversion time = **268** states*3 (max.)
				10: A/D conversion time = **138** states*3 (max.)
				11: A/D conversion time = **73** states*3 (max.)

(2) Page 1039, section 21.3.6 A/D Control Register (ADCR_1) Unit 1, bit 3 and 2

[Before Change]

Bit	Bit Name	Initial Value	R/W	Description
3	CKS1	0	R/W	Clock Select 1 and 0
2	CKS0	0	R/W	- Description omitted (no changes) -
				EXCKS, CKS1, and CKS0
				000: A/D conversion time = 530 states*3 (max.)
				001: A/D conversion time = 266 states*3 (max.)
				010: A/D conversion time = 134 states*3 (max.)
				011: A/D conversion time = 68 states*3 (max.)
				100: A/D conversion time = 332 states*3 (max.)
				101: A/D conversion time = 168 states*3 (max.)
				110: A/D conversion time = 87 states*3 (max.)
				111: A/D conversion time = 46 states*3 (max.)

[After Change]

Bit	Bit Name	Initial Value	R/W	Description
3	CKS1	0	R/W	Clock Select 1 and 0
2	CKS0	0	R/W	- Description omitted (no changes) -
				EXCKS, CKS1, and CKS0
				000: A/D conversion time = **528** states*3 (max.)
				001: A/D conversion time = **268** states*3 (max.)
				010: A/D conversion time = **138** states*3 (max.)
				011: A/D conversion time = **73** states*3 (max.)
				100: A/D conversion time = **336** states*3 (max.)
				101: A/D conversion time = **172** states*3 (max.)
				110: A/D conversion time = **90** states*3 (max.)
				111: A/D conversion time = **49** states*3 (max.)

(3) Page 1041, section 21.3.7 A/D Control Register (ADCR_2) Unit 2, bit 3 and 2

[Before Change]

Bit	Bit Name	Initial Value	R/W	Description
3	CKS1	0	R/W	Clock Select 1 and 0
2	CKS0	0	R/W	- Description omitted (no changes) -
				EXCKS, CKS1, and CKS0
				000: A/D conversion time = 530 states*3 (max.)
				001: A/D conversion time = 266 states*3 (max.)
				010: A/D conversion time = 134 states*3 (max.)
				011: A/D conversion time = 68 states*3 (max.)
				100: A/D conversion time = 332 states*3 (max.)
				101: A/D conversion time = 168 states*3 (max.)
				110: A/D conversion time = 87 states*3 (max.)
				111: A/D conversion time = 46 states*3 (max.)

[After Change]

Bit	Bit Name	Initial Value	R/W	Description
3	CKS1	0	R/W	Clock Select 1 and 0
2	CKS0	0	R/W	- Description omitted (no changes) -
				EXCKS, CKS1, and CKS0
				000: A/D conversion time = **528** states*3 (max.)
				001: A/D conversion time = **268** states*3 (max.)
				010: A/D conversion time = **138** states*3 (max.)
				011: A/D conversion time = **73** states*3 (max.)
				100: A/D conversion time = **336** states*3 (max.)
				101: A/D conversion time = **172** states*3 (max.)
				110: A/D conversion time = **90** states*3 (max.)
				111: A/D conversion time = **49** states*3 (max.)

(4) Page1047, table21.3 A/D Conversion Characteristics (EXCKS1 = 0), Table 21.4 A/D Conversion Characteristics (EXCKS1 = 1: Unit 1 and 2)

[Before Change]

Table 21.3 A/D Conversion Characteristics (EXCKS1 = 0)

		CKS1=0						CKS1=1					
		CKS=0			CKS=1			CKS=0			CKS=1		
Item	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
A/D conversion start delay time	t_D	4	—	14	4	—	10	4	—	8	3	—	7
Input sampling time	t_{SPL}	—	312	—	—	156	—	—	78	—	—	39	—
A/D conversion time	t_{CONV}	518	—	528	262	—	268	134	—	138	69	—	73

Table 21.4 A/D Conversion Characteristics (EXCKS1 = 1: Units 1 and 2)

		CKS1=0						CKS1=1					
		CKS=0			CKS=1			CKS=0			CKS=1		
Item	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
A/D conversion start delay time	t_D	4	—	14	4	—	10	4	—	8	3	—	7
Input sampling time	t_{SPL}	—	120	—	—	60	—	—	30	—	—	15	—
A/D conversion time	t_{CONV}	326	—	336	166	—	172	86	—	90	45	—	49

[After Change]

Table 21.3 A/D Conversion Characteristics (**Unit 0**)

		CKS1=0						CKS1=1					
		CKS0=0			**CKS0=1**			**CKS0=0**			**CKS0=1**		
Item	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
A/D conversion start delay time	t_D	**3**	—	14	**3**	—	10	**3**	—	8	3	—	7
Input sampling time	t_{SPL}	—	312	—	—	156	—	—	78	—	—	39	—
A/D conversion time	t_{CONV}	**517**	—	528	**261**	—	268	**133**	—	138	69	—	73

Table 21.4.1 A/D Conversion Characteristics (Units 1 and 2: EXCKS = 0)

		CKS1=0						**CKS1=1**					
		CKS0=0			**CKS0=1**			**CKS0=0**			**CKS0=1**		
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A/D conversion start delay time	**t_D**	**4**	**—**	**14**	**4**	**—**	**10**	**4**	**—**	**8**	**4**	**—**	**7**
Input sampling time	**t_{SPL}**	**—**	**312**	**—**	**—**	**156**	**—**	**—**	**78**	**—**	**—**	**39**	**—**
A/D conversion time	**t_{CONV}**	**518**	**—**	**528**	**262**	**—**	**268**	**134**	**—**	**138**	**70**	**—**	**73**

Table 21.4.**2** A/D Conversion Characteristics (**Units1 and 2: EXCKS = 1**)

		CKS1=0						CKS1=1					
		CKS0=0			**CKS0=1**			**CKS0=0**			**CKS0=1**		
Item	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
A/D conversion start delay time	t_D	4	—	14	4	—	10	4	—	8	**4**	—	7
Input sampling time	t_{SPL}	—	120	—	—	60	—	—	30	—	—	15	—
A/D conversion time	t_{CONV}	326	—	336	166	—	172	86	—	90	**46**	—	49

Section 28 List of Registers

(1) Page 1305, section 28.3 Register States in Each Operating Mode, description of SYSTEM module

[Before Change]

Register Abbreviation	Reset	Module Stop State	Sleep	All-Module-Clock-Stop	Software Standby	Deep Software Standby	Hardware Standby	Module
			- Description omitted (no changes) -					FLASH
DPSBYCR	Initialized	—	—	—	—	Initialized*1	Initialized	SYSTEM
DPSWCR	Initialized	—	—	—	—	Initialized*1	Initialized	
DPSIER	Initialized	—	—	—	—	Initialized*1	Initialized	
DPSIFR	Initialized	—	—	—	—	Initialized*1	Initialized	
DPSIEGR	Initialized	—	—	—	—	Initialized*1	Initialized	
RSTSR	Initialized	—	—	—	—	Initialized*1	Initialized	
LVDCR*3	Initialized*4	—	—	—	—	Initialized*1	Initialized	
			- Description omitted (no changes) -					SCI_2

[After Change]

Register Abbreviation	Reset	Module Stop State	Sleep	All-Module-Clock-Stop	Software Standby	Deep Software Standby	Hardware Standby	Module
			- Description omitted (no changes) -					FLASH
DPSBYCR	Initialized	—	—	—	—	—	Initialized	SYSTEM
DPSWCR	Initialized	—	—	—	—	—	Initialized	
DPSIER	Initialized	—	—	—	—	—	Initialized	
DPSIFR	Initialized	—	—	—	—	—	Initialized	
DPSIEGR	Initialized	—	—	—	—	—	Initialized	
RSTSR	Initialized	—	—	—	—	—	Initialized	
LVDCR*3	Initialized*4	—	—	—	—	—	Initialized	
			- Description omitted (no changes) -					SCI_2

Section 29 Electrical Characteristics

(1) Page1313, table29.1 Absolute Maximum Ratings

[Before Change]

Item	Symbol	Value	Unit
Power supply voltage	- Description omitted (no changes) -		
Input voltage (except for ports 4, 5, and N)	- Description omitted (no changes) -		
Input voltage (Port N)	V_{in}	–0.3 to V_{cc} + 6.0	V
Input voltage (port 4, 5)	V_{in}	–0.3 to + 0.3	V
Reference power supply voltage	- Description omitted (no changes) -		
Analog power supply voltage	- Description omitted (no changes) -		
Analog input voltage	- Description omitted (no changes) -		
Operating temperature	- Description omitted (no changes) -		
Storage temperature	- Description omitted (no changes) -		

[After Change]

Item	Symbol	Value	Unit
Power supply voltage	- Description omitted (no changes) -		
Input voltage (except for ports 4, 5, and N)	- Description omitted (no changes) -		
Input voltage (Port N)	V_{in}	–0.3 to + 6.0	V
Input voltage (port 4, 5)	V_{in}	–0.3 to AV_{cc} + 0.3	V
Reference power supply voltage	- Description omitted (no changes) -		
Analog power supply voltage	- Description omitted (no changes) -		
Analog input voltage	- Description omitted (no changes) -		
Operating temperature	- Description omitted (no changes) -		
Storage temperature	- Description omitted (no changes) -		