To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Mar.09.2009

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-H8*-A400A/E	Rev.	1.00
Title	Correction of errors in the H8SX/1638 and H8SX/1638L Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	H8SX/1638 and H8SX/1638L Group	Lot No. All lots	Reference Document	H8SX/1638 Group , H8SX/1638L Group Hardware Manual (REJ09B0364-0200)		

We would like to inform you of the correction of errors in the above listed hardware manuals. Please refer to the following for details.

<Corrections>

Section 1 Overview

Page 8, table 1.2 Comparison of Suoort Functions in the H8SX/1638 and H8SX/1638L Group

[Before Change]

Function		H8SX/1638Group	H8SX/1638LGroup
Package	LQFP-144	O	O

[After Change]

Function		H8SX/1638Group	H8SX/1638LGroup
Package	**LQFP-120**	O	O

Section7 Interrupt Controller

Deletion of DTCERG, and DTCERH
(1) Page 150 to 151, 7.6.5 DTC and DMAC Activation by Interrupt

[Before Change]

(1) Selection of Interrupt Sources

The activation source for each DMAC channel is selected by DMRSR. The selected activation source is input to the DMAC through the select circuit. When transfer by an on-chip module interrupt is enabled (DTF1 = 1, DTF0 = 0, and DTE = 1 in DMDR) and the DTA bit in DMDR is set to 1, the interrupt source selected for the DMAC activation source is controlled by the DMAC and cannot be used as a DTC activation source or CPU interrupt source.

Interrupt sources that are not controlled by the DMAC are set for DTC activation sources or CPU interrupt sources by the DTCE bit in DTCERA to DTCERH of the DTC.

- Description omitted (no changes) –

(2) Priority Determination

- Description omitted (no changes) –

(3) Operation Order

- Description omitted (no changes) –

Table 7.6 lists the selection of interrupt sources and interrupt source clear control by setting the DTA bit in DMDR of the DMAC, the DTCE bit in DTCERA to DTCERH of the DTC, and the DISEL bit in MRB of the DTC.

[After Change]

(1) Selection of Interrupt Sources

The activation source for each DMAC channel is selected by DMRSR. The selected activation source is input to the DMAC through the select circuit. When transfer by an on-chip module interrupt is enabled (DTF1 = 1, DTF0 = 0, and DTE = 1 in DMDR) and the DTA bit in DMDR is set to 1, the interrupt source selected for the DMAC activation source is controlled by the DMAC and cannot be used as a DTC activation source or CPU interrupt source.

Interrupt sources that are not controlled by the DMAC are set for DTC activation sources or CPU interrupt sources by the DTCE bit in DTCERA to **DTCERF** of the DTC.

- Description omitted (no changes) –

(2) Priority Determination

- Description omitted (no changes) –

(3) Operation Order

- Description omitted (no changes) –

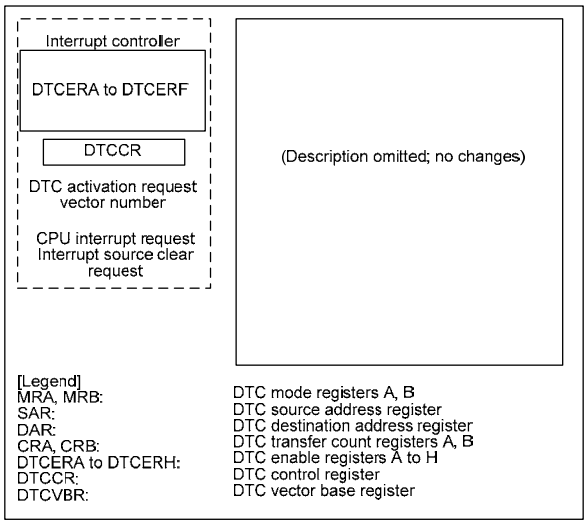
Table 7.6 lists the selection of interrupt sources and interrupt source clear control by setting the DTA bit in DMDR of the DMAC, the DTCE bit in DTCERA to **DTCERF** of the DTC, and the DISEL bit in MRB of the DTC.

Section 11 Data Transfer Controller

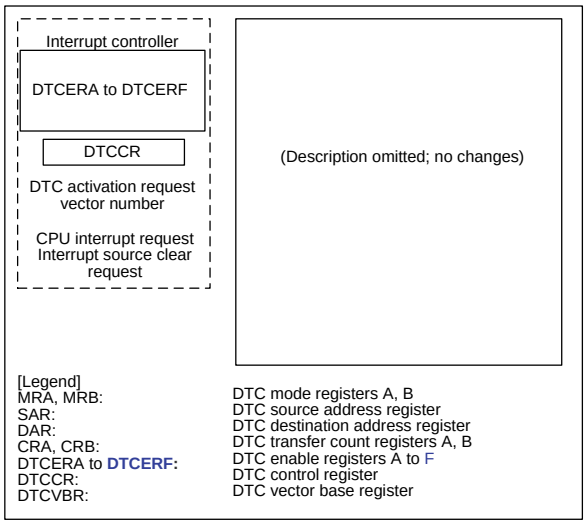
Deletion of DTCERG, and DTCERH in DTCER

(1) Page 354, DTCER description in figure 11.1, Block Diagram of DTC

[Before Change]



[After Change]



(2) Page 360, section 11.2.7, DTC Enable Register

[Before Change]

12.2.7 DTC enable registers A to H (DTCERA to DTCERF)

DTCER, which is comprised of eight registers, DTCERA to DTCERF, is a register that specifies DTC activation interrupt sources.

[After Change]

12.2.7 DTC Enable Register A to **F** (DTCERA to DTCERF)

DTCER, which is comprised of **six** registers, DTCERA to DTCERF, is a register that specifies DTC activation interrupt sources.

Section 12 I/O Ports

(1) Page 396, table 12.2 Register Configuration in Each Port

[Before Change]

Port	Number of Pins	Registers					
		DDR	DR	PORT	ICR	PCR	ODR
Ports 1 to 5		- Description omitted (no changes) -					
Port 6	6	O	O	O	O	-	-
Port A	8	O	O	O	O	-	-
Port B	4	O	O	O	O	-	-
Ports D *1 to K *2		- Description omitted (no changes) -					

[Legend]

O: Register exists

－: No register exists

Note: 1. Do not access port D or E registers when PCJKE=1.

2. Do not access port J or K registers when PCJKE=0.

[After Change]

Port	Number of Pins	Registers					
		DDR	DR	PORT	ICR	PCR	ODR
Ports 1 to 5		- Description omitted (no changes) -					
Port 6 *3	6	O	O	O	O	-	-
Port A	8	O	O	O	O	-	-
Port B *4	4	O	O	O	O	-	-
Ports D *1 to K *2		- Description omitted (no changes) -					

[Legend]

O: Register exists

－: No register exists

Note: 1. Do not access port D or E registers when PCJKE=1.

2. Do not access port J or K registers when PCJKE=0.

3. For port 6, only the six lower-order bits are valid (the two higher-order bits are reserved). The write value should always be the initial value.

4. For port B, only the four lower-order bits are valid (the four higher-order bits are reserved). The write value should always be the initial value.

(2) Page 422, 12.2.7 Port B, PB3 and PB2

[Before Change]

(1) PB3/$\overline{\text{CS3}}$/$\overline{\text{CS7}}$-A

The pin function is switched as shown below according to the combination of operating mode, EXPE bit, bus controller register, port function control register (PFCR), and the PB3DDR bit settings.

Module Name	Pin Function	Setting		
		Bus Controller		I/O Port
		$\overline{\text{CS3}}$_OE	$\overline{\text{CS7A}}$_OE	PB3DDR
- Description omitted (no changes) -				

(2) PB2/$\overline{\text{CS2}}$-A/$\overline{\text{CS6}}$-A

The pin function is switched as shown below according to the combination of operating mode, EXPE bit, bus controller register, port function control register (PFCR), and the PB2DDR bit settings.

Module Name	Pin Function	Setting		
		Bus Controller		I/O Port
		$\overline{\text{CS2A}}$_OE	$\overline{\text{CS6A}}$_OE	PB2DDR
- Description omitted (no changes) -				

[After Change]

(1) PB3/$\overline{\text{CS3}}$/$\overline{\text{CS7}}$-A

The pin function is switched as shown below according to the combination of operating mode, EXPE bit, port function control register (PFCR), and the PB3DDR bit settings.

Module Name	Pin Function	Setting		
		I/O Port		
		$\overline{\text{CS3}}$_OE	$\overline{\text{CS7A}}$_OE	PB3DDR
- Description omitted (no changes) -				

(2) PB2/$\overline{\text{CS2}}$-A/$\overline{\text{CS6}}$-A

The pin function is switched as shown below according to the combination of operating mode, EXPE bit, port function control register (PFCR), and the PB2DDR bit settings.

Module Name	Pin Function	Setting		
		I/O Port		
		$\overline{\text{CS2A}}$_OE	$\overline{\text{CS6A}}$_OE	PB2DDR
- Description omitted (no changes) -				

(3) Page 445, table 12.5 Available Output Signals and Settings in Each Port, output signal name of port F

[Before Change]

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PF	7	A23A_OE	- Description omitted (no changes) -		
		SCK5_OE			
		$\overline{CS4C}$_OE	CS4	PFCR1.CS4S[A,B]=10	SYSCR.EXPE=1,PFCR0.CS4E=1
		$\overline{CS5C}$_OE	CS5	PFCR1.CS5S[A,B]=10	SYSCR.EXPE=1,PFCR0.CS5E=1
		$\overline{CS6C}$_OE	- Description omitted (no changes) -		
		$\overline{CS7C}$_OE			

[After Change]

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
PF	7	A23A_OE	- Description omitted (no changes) -		
		SCK5_OE			
		$\overline{CS4C}$_OE	$\overline{CS4}$	PFCR1.CS4S[A,B]=10	SYSCR.EXPE=1,PFCR0.CS4E=1
		$\overline{CS5C}$_OE	$\overline{CS5}$	PFCR1.CS5S[A,B]=10	SYSCR.EXPE=1,PFCR0.CS5E=1
		$\overline{CS6C}$_OE	- Description omitted (no changes) -		
		$\overline{CS7C}$_OE			

Section 19 A/D Converter

(1) Page 784, bits 3 and 2 in ADCR_0

[Before Change]

Bit	Bit Name	Initial Value	R/W	Description
3 2	CKS1 CKS0	0 0	R/W R/W	Clock select 1 and 0 - Description omitted (no changes) - CKS1, and CKS0 00: A/D conversion time = 530 states *2 (max) 01: A/D conversion time = 266 states *2 (max) 10: A/D conversion time = 134 states *2 (max) 11: A/D conversion time = 68 states *2 (max)

[After Change]

Bit	Bit Name	Initial Value	R/W	Description
3 2	CKS1 CKS0	0 0	R/W R/W	Clock select 1 and 0 - Description omitted (no changes) - CKS1, and CKS0 00: A/D conversion time = **528** states *2 (max) 01: A/D conversion time = **268** states *2 (max) 10: A/D conversion time = **138** states *2 (max) 11: A/D conversion time = **73** states *2 (max)

(2) Page 786, bits 3 and 2 in ADCR_1

[Before Change]

Bit	Bit Name	Initial Value	R/W	Description
3 2	CKS1 CKS0	0 0	R/W R/W	Clock select 1 and 0 - Description omitted (no changes) - EXCKS, CKS1, and CKS0 000: A/D conversion time = 530 states *2 (max) 001: A/D conversion time = 266 states *2 (max) 010: A/D conversion time = 134 states *2 (max) 011: A/D conversion time = 68 states *2 (max) 100: A/D conversion time = 332 states *2 (max) 101: A/D conversion time = 168 states *2 (max) 110: A/D conversion time = 87 states *2 (max) 111: A/D conversion time = 46 states *2 (max)

[After Change]

Bit	Bit Name	Initial Value	R/W	Description
3 2	CKS1 CKS0	0 0	R/W R/W	Clock select 1 and 0 - Description omitted (no changes) - EXCKS, CKS1, and CKS0 000: A/D conversion time = **528** states *2 (max) 001: A/D conversion time = **268** states *2 (max) 010: A/D conversion time = **138** states *2 (max) 011: A/D conversion time = **73** states *2 (max) 100: A/D conversion time = **336** states *2 (max) 101: A/D conversion time = **172** states *2 (max) 110: A/D conversion time = **90** states *2 (max) 111: A/D conversion time = **49** states *2 (max)

(3) Page792, table19.3 A/D Conversion Characteristics (EXCKS1 = 0), Table 19.4 A/D Conversion Characteristics (EXCKS1 = 1: Unit 1)

[Before Change]

Table 19.3 A/D Conversion Characteristics (EXCKS1 = 0)

		CKS1=0						CKS1=1					
		CKS=0			CKS=1			CKS=0			CKS=1		
Item	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
A/D conversion start delay time	t_D	4	—	14	4	—	10	4	—	8	3	—	7
Input sampling time	t_{SPL}	—	312	—	—	156	—	—	78	—	—	39	—
A/D conversion time	t_{CONV}	518	—	528	262	—	268	134	—	138	69	—	73

Table 19.4 A/D Conversion Characteristics (EXCKS1 = 1: Unit 1)

		CKS1=0						CKS1=1					
		CKS=0			CKS=1			CKS=0			CKS=1		
Item	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
A/D conversion start delay time	t_D	4	—	14	4	—	10	4	—	8	3	—	7
Input sampling time	t_{SPL}	—	120	—	—	60	—	—	30	—	—	15	—
A/D conversion time	t_{CONV}	326	—	336	166	—	172	86	—	90	45	—	49

[After Change]

Table 19.3 A/D Conversion Characteristics (**Unit 0**)

		CKS1=0						CKS1=1					
		CKS0=0			**CKS0=1**			**CKS0=0**			**CKS0=1**		
Item	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
A/D conversion start delay time	t_D	**3**	—	14	**3**	—	10	**3**	—	8	3	—	7
Input sampling time	t_{SPL}	—	312	—	—	156	—	—	78	—	—	39	—
A/D conversion time	t_{CONV}	**517**	—	528	**261**	—	268	**133**	—	138	69	—	73

Table 19.4.1 A/D Conversion Characteristics (Unit 1:EXCKS = 0)

		CKS1=0						**CKS1=1**					
		CKS0=0			**CKS0=1**			**CKS0=0**			**CKS0=1**		
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A/D conversion start delay time	**t_D**	**4**	**—**	**14**	**4**	**—**	**10**	**4**	**—**	**8**	**4**	**—**	**7**
Input sampling time	**t_{SPL}**	**—**	**312**	**—**	**—**	**156**	**—**	**—**	**78**	**—**	**—**	**39**	**—**
A/D conversion time	**t_{CONV}**	**518**	**—**	**528**	**262**	**—**	**268**	**134**	**—**	**138**	**70**	**—**	**73**

Table 19.4.**2** A/D Conversion Characteristics (**Unit 1:EXCKS = 1**)

		CKS1=0						CKS1=1					
		CKS0=0			**CKS0=1**			**CKS0=0**			**CKS0=1**		
Item	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
A/D conversion start delay time	t_D	4	—	14	4	—	10	4	—	8	**4**	—	7
Input sampling time	t_{SPL}	—	120	—	—	60	—	—	30	—	—	15	—
A/D conversion time	t_{CONV}	326	—	336	166	—	172	86	—	90	**46**	—	49

Section 22 Flash Memory

(1) Page 843, table 22.5 On-Board Programming Mode Setting

[Before Change]

Mode Setting	EMLE	MD2	MD1	MD0
User boot mode	0	0	0	1
Boot mode	0	0	1	0
User program mode	0	1	1	0
	0	1	1	1

[After Change]

Mode Setting	EMLE	MD2	MD1	MD0
User boot mode	0	0	0	1
Boot mode	0	0	1	0
User program mode	0	1	1	0
	0	1	1	1

Section 27 Electrical Characteristics

(1) Page1045, table27.2 DC Characteristics (2)

[Before Change]

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Tree-state leakage current (off state)	– Description omitted (no changes) –								
Input pull-up MOS current	– Description omitted (no changes) –								
Input capacitance	– Description omitted (no changes) –								
Current consumption*2	Normal operation			I_{CC}*4	– Description omitted (no changes) –				
	Sleep mode				– Description omitted (no changes) –				
	Standby mode	Software standby mode*3			—	0.15	1.1		Ta ≤ 50°C
					—	—	3.5		50°C < Ta
		Deep software standby mode	RAM retained*3		– Description omitted (no changes) –				
			RAM power supply halted		– Description omitted (no changes) –				
		Hardware standby mode			—	2	7	mA	Ta ≤ 50°C
					—	—	25		50°C < Ta
	All-module-clock-stop mode*5				– Description omitted (no changes) –				
Analog power supply current	– Description omitted (no changes) –								

[After Change]

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Tree-state leakage current (off state)	– Description omitted (no changes) –								
Input pull-up MOS current	– Description omitted (no changes) –								
Input capacitance	– Description omitted (no changes) –								
Current consumption*2	Normal operation			I_{CC}*4	– Description omitted (no changes) –				
	Sleep mode				– Description omitted (no changes) –				
	Standby mode	Software standby mode*3			—	0.15	1.1	**mA**	Ta ≤ 50°C
					—	—	3.5		50°C < Ta
		Deep software standby mode	RAM retained*3		– Description omitted (no changes) –				
			RAM power supply halted		– Description omitted (no changes) –				
		Hardware standby mode			—	2	7	**µA**	Ta ≤ 50°C
					—	—	25		50°C < Ta
	All-module-clock-stop mode*5				– Description omitted (no changes) –				
Analog power supply current	– Description omitted (no changes) –								