To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)
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Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the correction of errors concerning the IrDA function of the serial communication interface (SCI, IrDA, and CRC) in the H8S/2168 Group Hardware Manual and H8S/2158 Hardware Manual as shown below.

The descriptions of the phase inversion function of the IrDA in the serial communication interface (SCI, IrDA, and CRC) are deleted.

**Correction 1:** Section 14.3.10, Serial Interface Control Register (SCICR), in the H8S/2168 Group Hardware Manual

[Before Change]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>IrE</td>
<td>0</td>
<td>R/W</td>
<td>IrDA Enable</td>
</tr>
<tr>
<td>3</td>
<td>IrTxINV</td>
<td>0</td>
<td>R/W</td>
<td>IrTx Data Invert</td>
</tr>
</tbody>
</table>

Specifies the inversion of the logic level of the output from IrTxD. When the inversion is specified, IrCKS2 to IrCKS0 specify the low-level width, not the high-level width.

0: Transmit data is output from IrTxD as it is
1: Transmit data is inverted before being output from IrTxD

| 2   | IrRxINV  | 0             | R/W | IrRx Data Invert |

Specifies the inversion of the logic level of the input to IrRxD. When the inversion is specified, IrCKS2 to IrCKS0 specify the low-level width, not the high-level width.

0: Input to IrRxD is used as receive data as it is
1: Input to IrRxD is inverted before being used as receive data
Bit | Bit Name | Initial Value | R/W | Description
--- | --- | --- | --- | ---
7 | IrE | 0 | R/W | IrDA Enable

3, 2 | All | 0 | R/W | Reserved

The initial value should not be changed.

**Correction 2:** Figure 14.36, IrDA Block Diagram, in the H8S/2168 Group Hardware Manual

**Before Change**

![IrDA Block Diagram Before Change]

**After Change**

![IrDA Block Diagram After Change]

**Correction 3:** Transmission in section 14.8, IrDA Operation, in the H8S/2168 Group Hardware Manual

**Before Change**

For serial data of level 0, a high-level pulse having a width of 3/16 of the bit rate (1-bit interval) is output (initial setting). The high-level pulse can be selected using the IrCKS2 to IrCKS0 bits in SCICR. The output waveform can also be inverted using the IrTxINV bit in SCICR.

The high-level pulse width is defined...

**After Change**

For serial data of level 0, a high-level pulse having a width of 3/16 of the bit rate (1-bit interval) is output (initial setting). The high-level pulse can be selected using the IrCKS2 to IrCKS0 bits in SCICR.

The high-level pulse width is defined...

**Correction 4:** Reception in section 14.8, IrDA Operation, in the H8S/2168 Group Hardware Manual

**Before Change**

During reception, IR frames are converted to UART frames using the IrDA interface before inputting to SCI_1. Here, the input waveform can also be inverted using the IrRxINV bit in SCICR.

Data of level 0 is output each time...

**After Change**

During reception, IR frames are converted to UART frames using the IrDA interface before inputting to SCI_1. Here, the input waveform can also be inverted using the IrRxINV bit in SCICR.

Data of level 0 is output each time...
During reception, IR frames are converted to UART frames using the IrDA interface before inputting to SCI_1.

Data of level 0 is output each time…

**Correction 5:** Section 24.2, Register Bits, in the H8S/2168 Group Hardware Manual

**[Before Change]**

<table>
<thead>
<tr>
<th>Register</th>
<th>Abbreviation</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCICR</td>
<td>IrE</td>
<td>IrCKS2</td>
<td>IrCKS1</td>
<td>IrCKS0</td>
<td>IrTxINV</td>
<td>IrRxINV</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SCI_1</td>
</tr>
</tbody>
</table>

**[After Change]**

<table>
<thead>
<tr>
<th>Register</th>
<th>Abbreviation</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCICR</td>
<td>IrE</td>
<td>IrCKS2</td>
<td>IrCKS1</td>
<td>IrCKS0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SCI_1</td>
</tr>
</tbody>
</table>

**Correction 6:** Section 16.3.10, Serial Interface Control Register (SCICR), in the H8S/2158 Hardware Manual

**[Before Change]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>IrE</td>
<td>0</td>
<td>R/W</td>
<td>IrDA Enable</td>
</tr>
<tr>
<td>3</td>
<td>IrTxINV</td>
<td>0</td>
<td>R/W</td>
<td>IrTx Data Invert</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Specifies the inversion of the logic level of the output from IrTxD. When the inversion is specified, IrCKS2 to IrCKS0 specify the low-level width, not the high-level width.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: Transmit data is output from IrTxD as it is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: Transmit data is inverted before being output from IrTxD</td>
</tr>
<tr>
<td>2</td>
<td>IrRxINV</td>
<td>0</td>
<td>R/W</td>
<td>IrRx Data Invert</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Specifies the inversion of the logic level of the input to IrRxD. When the inversion is specified, IrCKS2 to IrCKS0 specify the low-level width, not the high-level width.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: Input to IrRxD is used as receive data as it is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: Input to IrRxD is inverted before being used as receive data</td>
</tr>
</tbody>
</table>
Correction 7: Figure 16.36, IrDA Block Diagram, in the H8S/2158 Hardware Manual

Before Change

For serial data of level 0, a high-level pulse having a width of 3/16 of the bit rate (1-bit interval) is output (initial setting). The high-level pulse can be selected using the IrCKS2 to IrCKS0 bits in SCICR. The output waveform can also be inverted using the IrTxINV bit in SCICR.

The high-level pulse width is defined...

After Change

For serial data of level 0, a high-level pulse having a width of 3/16 of the bit rate (1-bit interval) is output (initial setting). The high-level pulse can be selected using the IrCKS2 to IrCKS0 bits in SCICR.

The high-level pulse width is defined...

Correction 8: Transmission in section 16.8, IrDA Operation, in the H8S/2158 Hardware Manual

Before Change

During reception, IR frames are converted to UART frames using the IrDA interface before inputting to SCI_1. Here, the input waveform can also be inverted using the IrRxINV bit in SCICR.

Data of level 0 is output each time...

After Change

During reception, IR frames are converted to UART frames using the IrDA interface before inputting to SCI_1. Here, the input waveform can also be inverted using the IrRxINV bit in SCICR.

Data of level 0 is output each time...
During reception, IR frames are converted to UART frames using the IrDA interface before inputting to SCI_1. Data of level 0 is output each time…

**Correction 10:** Section 28.2, Register Bits, in the H8S/2158 Hardware Manual

<table>
<thead>
<tr>
<th>Register Abbreviation</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCICR</td>
<td>IrE</td>
<td>IrCKS2</td>
<td>IrCKS1</td>
<td>IrCKS0</td>
<td>IrTxINV</td>
<td>IrRxINV</td>
<td>—</td>
<td>—</td>
<td>SCI_1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register Abbreviation</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
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<th>Bit 1</th>
<th>Bit 0</th>
<th>Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCICR</td>
<td>IrE</td>
<td>IrCKS2</td>
<td>IrCKS1</td>
<td>IrCKS0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SCI_1</td>
</tr>
</tbody>
</table>