Date: Jul. 12, 2022

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A0928A/E	Rev.	1.00
Title	Correction of Errors and Addition of the Usage Note on the Ethernet Controller and the Ethernet Controller DMA Controller		Information Category	Technical Notification		
Applicable Product	SH7214 Group SH7216 Group	Lot No. All lots	Reference Document	SH7214 Group, SH7216 Group User's Manual: Hardware Rev. 4.00 (R01UH0230EJ0400)		

This update is to inform you of the corrections to errors and addition of the usage note on the Ethernet Controller (EtherC) and the Ethernet Controller DMA Controller (E-DMAC) in the hardware manual of the above applicable products.

<Corrections>

25.3.1 EtherC Mode Register (ECMR)

The description of the TPC bit is corrected as follows.

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
20	TPC	0	R/W	PAUSE Frame Transmission 0: PAUSE frame is not transmitted in a PAUSE period 1: PAUSE frame is transmitted even in a PAUSE period

[After change]

Bit	Bit Name	Initial Value	R/W	Description
20	TPC	0	R/W	PAUSE Frame Transmission 0: PAUSE frame is transmitted in a PAUSE period 1: PAUSE frame is not transmitted in a PAUSE period

25.3.2 EtherC Status Register (ECSR)

The description of the BFR bit is changed as follows.

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
5	BFR	0	R/W	Continuous Broadcast Frame Reception Interrupt (Interrupt Source) Indicates that broadcast frames have been continuously received.

[After change]

Bit	Bit Name	Initial Value	R/W	Description
5	BFR	0	R/W	Continuous Broadcast Frame Reception 0: The number of continuously received broadcast frames is less than the value set in the BCFRR register. 1: The number of continuously received broadcast frames is greater than or equal to the value set in the BCFRR register.

25.3.2 EtherC Status Register (ECSR)

The description of this register is changed as follows.

[Before change]

ECSR is a 32-bit readable/writable register that indicates the status in the EtherC. This status can be notified to the CPU by interrupts. When 1 is written to the PSRTO, LCHNG, MPD, and ICD bits, the corresponding flags can be cleared to 0.

[After change]

ECSR is a 32-bit readable/writable register that indicates the status in the EtherC. This status can be notified to the CPU by interrupts. When 1 is written to the BFR, PSRTO, LCHNG, MPD, and ICD bits, the corresponding flags can be cleared to 0.

25.3.3 EtherC Interrupt Enable Register (ECSIPR)

The description of the BFSIPR bit is corrected as follows.

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
5	BFSIPR	0	R/W	Continuous Broadcast Frame Reception Interrupt Enable 0: Enables an interrupt requested by the BFR bit in ECSR 1: Disables an interrupt requested by the BFR bit in ECSR

[After change]

Bit	Bit Name	Initial Value	R/W	Description
5	BFSIPR	0	R/W	Continuous Broadcast Frame Reception Interrupt Enable 0: Interrupt notification by the BFR bit is disabled 1: Interrupt notification by the BFR bit is enabled

26.2.8 Transmit/Receive Status Copy Enable Register (TRSCER)

The description of this register is changed as follows.

[Before change]

TRSCER specifies whether to reflect the transmit/receive status information reported by bits in the EtherC/E-DMAC status register (EESR) in bits TFS25 to TFS0 or RFS26 to RFS0 of the corresponding descriptor. The bits in this register correspond to bits 11 to 0 in EESR. When a bit is cleared to 0, the transmit status (bits 11 to 8 in EESR) is reflected in the TFS3 to TFS0 bits of the transmit descriptor, and the receive status (bits 7 to 0 in EESR) is reflected in the RFS7 to RFS0 bits of the receive descriptor. When a bit is set to 1, the occurrence of the corresponding source is not reflected in the descriptor. After this LSI is reset, all bits are cleared to 0.

[After change]

TRSCER specifies whether to reflect the receive status indicated in bits in the EtherC/E-DMAC status register (EESR) in the RFE bit of the receive descriptor.

The bits in TRSCER correspond to the bits with the same numbers in EESR.

When a bit in TRSCER is cleared to 0, the corresponding receive status (bit 7 or bit 4 in EESR) is reflected in the RFE bit of the receive descriptor.

When a bit is set to 1, the receive status is not reflected in the RFE bit. After a power-on reset, all bits are cleared to 0.

26.2.8 Transmit/Receive Status Copy Enable Register (TRSCER)

Bits 11 to 8 and 3 to 0 of this register are changed to reserved bits as follows. In addition, "RFS" in the Description column is corrected to "RFE".

[Before change]

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CND CE	DLC CE	CD CE	TRO CE	RMAF CE	—	—	RRF CE	RTLF CE	RTSF CE	PRE CE	CERF CE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	CNDCE	0	R/W	CND Bit Copy Directive 0: Reflects the CND bit status in the TFS bit of the transmit descriptor 1: Occurrence of the corresponding source is not reflected in the TFS bit of the transmit descriptor
10	DLCCE	0	R/W	DLC Bit Copy Directive 0: Reflects the DLC bit status in the TFS bit of the transmit descriptor 1: Occurrence of the corresponding source is not reflected in the TFS bit of the transmit descriptor
9	CDCE	0	R/W	CD Bit Copy Directive 0: Reflects the CD bit status in the TFS bit of the transmit descriptor 1: Occurrence of the corresponding source is not reflected in the TFS bit of the transmit descriptor
8	TROCE	0	R/W	TRO Bit Copy Directive 0: Reflects the TRO bit status in the TFS bit of the transmit descriptor 1: Occurrence of the corresponding source is not reflected in the TFS bit of the transmit descriptor
7	RMAFCE	0	R/W	RMAF Bit Copy Directive 0: Reflects the RMAF bit status in the RFS bit of the receive descriptor 1: Occurrence of the corresponding source is not reflected in the RFS bit of the receive descriptor
6, 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RRFCE	0	R/W	RRF Bit Copy Directive 0: Reflects the RRF bit status in the RFS bit of the receive descriptor 1: Occurrence of the corresponding source is not reflected in the RFS bit of the receive descriptor
3	RTLFCE	0	R/W	RTLF Bit Copy Directive 0: Reflects the RTLF bit status in the RFS bit of the receive descriptor 1: Occurrence of the corresponding source is not reflected in the RFS bit of the receive descriptor
2	RTSFCE	0	R/W	RTSF Bit Copy Directive 0: Reflects the RTSF bit status in the RFS bit of the receive descriptor 1: Occurrence of the corresponding source is not reflected in the RFS bit of the receive descriptor
1	PRECE	0	R/W	PRE Bit Copy Directive 0: Reflects the PRE bit status in the RFS bit of the receive descriptor 1: Occurrence of the corresponding source is not reflected in the RFS bit of the receive descriptor
0	CERFCE	0	R/W	CERF Bit Copy Directive 0: Reflects the CERF bit status in the RFS bit of the receive descriptor 1: Occurrence of the corresponding source is not reflected in the RFS bit of the receive descriptor

[After change]

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RMAFCE	—	—	RRFCE	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	RMAFCE	0	R/W	RMAF Bit Copy Directive 0: Reflects the RMAF bit status in the RFE bit of the receive descriptor 1: Occurrence of the corresponding source is not reflected in the RFE bit of the receive descriptor
6, 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RRFCE	0	R/W	RRF Bit Copy Directive 0: Reflects the RRF bit status in the RFE bit of the receive descriptor 1: Occurrence of the corresponding source is not reflected in the RFE bit of the receive descriptor
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

26.2.9 Receive Missed-Frame Counter Register (RMFCR)

The description of this register is corrected as follows.

[Before change]

RMFCR is a 16-bit counter that indicates the number of frames that were not saved in the receive buffer and so were discarded during reception. When the receive FIFO overflows, the receive frames in the FIFO are discarded. The number of frames discarded at this time is counted. When the value in this register reaches H'FFFF, the counter stops incrementing. The counter value is cleared to 0 by writing any value to this register.

[After change]

RMFCR is a 16-bit counter that indicates the number of frames that were not saved in the receive buffer and so were discarded during reception. When the receive FIFO overflows, it suspends the acceptance of data and discards the subsequent frames.

The number of frames discarded at this time is counted. When the value in this register reaches H'FFFF, the counter stops incrementing. The counter value is cleared to 0 by writing any value to this register.

26.2.11 FIFO Depth Register (FDR)

Corrected as follows.

[Before change]

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	TFD[4:0]					—	—	—	RFD[4:0]				
Initial value:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
12 to 8	TFD[4:0]	00111	R/W	Transmit FIFO Size Specifies the size of the transmit FIFO. The setting must not be changed during transmission or reception. 00000: 256 bytes 00001: 512 bytes 00010: 768 bytes 00011: 1024 bytes 00100: 1280 bytes 00101: 1536 bytes 00110: 1792 bytes 00111: 2048 bytes Other than above: Setting prohibited
4 to 0	RFD[4:0]	00111	R/W	Receive FIFO Size Specifies the size of the receive FIFO. The setting must not be changed during transmission or reception. 00000: 256 bytes 00001: 512 bytes 00010: 768 bytes 00011: 1024 bytes 00100: 1280 bytes 00101: 1536 bytes 00110: 1792 bytes 00111: 2048 bytes Other than above: Setting prohibited

[After change]

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	TFD[4:0]					—	—	—	RFD[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
12 to 8	TFD[4:0]	00000	R/W	Transmit FIFO Size Specifies the size of the transmit FIFO. The setting must not be changed during transmission or reception. 00000: 256 bytes 00001: 512 bytes 00010: 768 bytes 00011: 1024 bytes 00100: 1280 bytes 00101: 1536 bytes 00110: 1792 bytes 00111: 2048 bytes Other than above: Setting prohibited
4 to 0	RFD[4:0]	00000	R/W	Receive FIFO Size Specifies the size of the receive FIFO. The setting must not be changed during transmission or reception. 00000: 256* bytes 00001: 512* bytes 00010: 768* bytes 00011: 1024* bytes 00100: 1280* bytes 00101: 1536* bytes 00110: 1792* bytes 00111: 2048* bytes Other than above: Setting prohibited Note: * 80 bytes of the receive FIFO size are used as the receive frame management area.

26.2.19 Flow Control Start FIFO Threshold Setting Register (FCFTR)

Corrected as follows.

[Before change]

FCFTR is a 32-bit readable/writable register that sets the flow control of the EtherC (automatic PAUSE transmission threshold setting). FCFTR can set the threshold values for the receive FIFO data size (RFDO[2:0]) and the number of receive frames (RFFO[2:0]). The flow control starts when either the receive FIFO data size threshold or the receive frame count threshold is determined.

If the same receive FIFO size as set by the FIFO depth register (FDR) is set when the flow control is to be turned on according to the RFDO setting condition, flow control is turned on with (FIFO data size − 64) bytes. When RFD = 00111 in FDR and RFDO = 111 in this register, for instance, the flow control is turned on when (2,048 − 64) bytes of data are stored in the receive FIFO. Set a value equal to or less than the RFD value in FDR for the RFDO bits in this register.

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	RFFO[2:0]	111	R/W	Receive Frame Count Overflow BSY Output Threshold 000: When two frames have been stored in the receive FIFO. 001: When four frames have been stored in the receive FIFO. 010: When six frames have been stored in the receive FIFO. : 110: When 14 frames have been stored in the receive FIFO. 111: When 16 frames have been stored in the receive FIFO.
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	RFDO[2:0]	111	R/W	Receive FIFO Overflow BSY Output Threshold 000: When (256 − 32)-byte data is stored in the receive FIFO. 001: When (512 − 32)-byte data is stored in the receive FIFO. : 110: When (1792 − 32)-byte data is stored in the receive FIFO. 111: When (2048 − 64)-byte data is stored in the receive FIFO.

[After change]

FCFTR is a 32-bit readable/writable register that sets the flow control of the EtherC (automatic PAUSE transmission threshold setting). RFDO[2:0] of FCFTR can set the threshold value for the amount of receive data stored in receive FIFO and RFFO[2:0] can set the threshold value for the number of receive frames. The flow control starts when either the receive FIFO data size threshold or the receive frame count threshold is determined.

If the value of RFDO is the same as the value of the receive FIFO size (RFD) set by the FIFO depth register (FDR) when the flow control is to be turned on according to the RFDO setting condition, flow control is turned on with (FIFO data size − 96) bytes. When RFD = 00111 in FDR and RFDO = 111 in this register, for instance, the flow control is turned on when (2,048 − 96) bytes of data are stored in the receive FIFO. Set a value equal to or less than the RFD value in FDR for the RFDO bits in this register.

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	RFFO[2:0]	111	R/W	Receive Frame Count Overflow PAUSE Output Threshold 000: When two frames have been stored in the receive FIFO. 001: When four frames have been stored in the receive FIFO. 010: When six frames have been stored in the receive FIFO. : 110: When 14 frames have been stored in the receive FIFO. 111: When 16 frames have been stored in the receive FIFO.
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	RFDO[2:0]	111	R/W	Receive FIFO Overflow PAUSE Output Threshold 000: When (256 − (32 or 96)*) -byte data is stored in the receive FIFO. 001: When (512 − (32 or 96)*)-byte data is stored in the receive FIFO. : 110: When (1792 − (32 or 96)*)-byte data is stored in the receive FIFO. 111: When (2048 − 96*)-byte data is stored in the receive FIFO. Note: * Usually, flow control is turned on when (the FIFO data size – 32) bytes of data are stored in the receive FIFO. If the value of RFDO is the same as the value of the receive FIFO size (RFD) set by the FIFO depth register (FDR), flow control is turned on when (the FIFO data size – 96) bytes of data are stored.

26.3.1 Descriptor Lists and Data Buffers

(1) Transmit Descriptor

(a) Transmit Descriptor 0 (TD0)

The descriptions of bits 27 to 0 are corrected.

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
27	TFE	0	R/W	Transmit Frame Error When set to 1, this bit indicates that an error is indicated by any of the TFS bits. (For TFS7 to TFS0, it is possible to prevent this bit from being set by TRSCER. This is not possible, however, if a source indicated by TFS7 to TFS0 also causes TFS8 to be set.) 1: Frame transmission has been aborted.
26	TWBI	0	R/W	Write-Back Completion Interrupt Notification (This bit is valid when TRIMD is set so.) 0: No operation 1: An interrupt is generated upon completion of write-back to this descriptor.
25 to 0	TFS	All 0	R/W	Transmit Frame Status TFS25 toTFS9 [Reserved (The write value should always be 0.)] TFS8 [Transmit Abort Detect]: When set to 1, this bit indicates that the abort signal is set to 1 during frame transmission (causing TFE to be set). TFS7 to TFS4 [Reserved (The write value should always be 0.)] TFS3 [No Carrier Detect (corresponding to the CND bit in EESR)] TFS2 [Carrier Loss Detect (corresponding to the DLC bit in EESR)] TFS1 [Delayed Collision Detect during Transmission (corresponding to the CD bit in EESR)] TFS0 [Transmit Retry Over (corresponding to the TRO bit in EESR)]: When set to 1, these bits indicate that TFS8 to TFS1 have been set to 1 during frame transmission. (Although TFE is normally set when these bits are set to 1, it can be prevented from being set by so setting TRSCER.)

[After change]

Bit	Bit Name	Initial Value	R/W	Description
27	TFE	0	R/W	Transmit Frame Error 0: Frame transmission has ended normally. 1: Frame transmission has been aborted and an error is indicated by any of the TFS bits.
26	TWBI	0	R/W	Write-Back Completion Interrupt Notification (This bit is valid when the TIM or TIS bit in TRIMD or the TWBIP bit in EESIPR is set so.) 0: An interrupt is not generated upon completion of write-back to this descriptor. 1: An interrupt is generated upon completion of write-back to this descriptor.
25 to 0	TFS	All 0	R/W	Transmit Frame Status TFS25 toTFS9 [Reserved (The write value should always be 0.)] TFS8 [Transmit Abort Detect]: When set to 1, this bit indicates that the abort signal is set to 1 during frame transmission (causing TFE to be set). TFS7 to TFS4 [Reserved (The write value should always be 0.)] TFS3 [No Carrier Detect (corresponding to the CND bit in EESR)] TFS2 [Carrier Loss Detect (corresponding to the DLC bit in EESR)] TFS1 [Delayed Collision Detect during Transmission (corresponding to the CD bit in EESR)] TFS0 [Transmit Retry Over (corresponding to the TRO bit in EESR)]: When set to 1, these bits indicate that the corresponding bit in EESR has been set to 1 during frame transmission. (TFE is normally set when these bits are set to 1.)

(2) Receive Descriptor

(a) Receive Descriptor 0 (RD0)

The descriptions of bits 27 to 0 are corrected.

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
27	RFE	0	R/W	Receive Frame Error When set to 1, this bit indicates that an error is indicated by any of the RFS bits. (For RFS7 to RFS0, it is possible to prevent this bit from being set by TRSCER. This is not possible, however, if a source indicated by RFS7 to RFS0 also causes RFS8 to be set.)
26 to 0	RFS	All 0	R/W	Receive Frame Status RF26 to RF10 [Reserved (The write value should always be 0.)] RFS9 [Receive FIFO Overflow (corresponding to the RFOF bit in EESR)]: When set to 1, this bit indicates that a receive FIFO overflow has occurred terminating the frame halfway and that the frame has been written back (causing RFE to be set). RFS8 [Receive Abort Detect]: When set to 1, this bit indicates that the abort signal is set to 1 during frame reception (causing RFE to be set). RFS7 [Multicast Address Frame Received (corresponding to the RMAF bit in EESR)] RFS6 and RFS5 [Reserved (The write value should always be 0.)] RFS4 [Residual-Bit Frame Receive Error (corresponding to the RRF bit in EESR)] RFS3 [Long Frame Receive Error (corresponding to the RTLF bit in EESR)] RFS2 [Short Frame Receive Error (corresponding to the RTSF bit in EESR)] RFS1 [PHY-LSI Receive Error (corresponding to the PRE bit in EESR)] RFS0 [Receive Frame CRC Error Detect (corresponding to the CERF bit in EESR)]: When set to 1, these bits indicate that RFS8 to RFS1 have been set to 1 during frame reception. (Although RFE is normally set when these bits are set to 1, it can be prevented from being set by so setting TRSCER.)

[After change]

Bit	Bit Name	Initial Value	R/W	Description
27	RFE	0	R/W	Receive Frame Error 0: The receive frame has no error. 1: The receive frame has an error and an error is indicated by any of the RFS bits. (For RFS7 and RFS4, it is possible to prevent this bit from being set by TRSCER.)
26 to 0	RFS	All 0	R/W	Receive Frame Status RF26 to RF10 [Reserved (The write value should always be 0.)] RFS9 [Receive FIFO Overflow (corresponding to the RFOF bit in EESR)]: When set to 1, this bit indicates that a receive FIFO overflow has occurred terminating the frame halfway and that the frame has been written back (causing RFE to be set). RFS8 [Receive Abort Detect]: When set to 1, this bit indicates that the abort signal is set to 1 during frame reception (causing RFE to be set). RFS7 [Multicast Address Frame Received (corresponding to the RMAF bit in EESR)] RFS6 and RFS5 [Reserved (The write value should always be 0.)] RFS4 [Residual-Bit Frame Receive Error (corresponding to the RRF bit in EESR)] RFS3 [Long Frame Receive Error (corresponding to the RTLF bit in EESR)] RFS2 [Short Frame Receive Error (corresponding to the RTSF bit in EESR)] RFS1 [PHY-LSI Receive Error (corresponding to the PRE bit in EESR)] RFS0 [Receive Frame CRC Error Detect (corresponding to the CERF bit in EESR)]: When set to 1, these bits indicate that the corresponding bit in EESR has been set to 1 during frame reception. (RFE is normally set when these bits are set to 1.)

26.4 Usage Notes

The following note is added.

• Software reset during frame transmission/reception

If a software reset is executed by setting EDMR.SWR = 1 while frame transmission/reception is in progress (i.e. EDTRR.TR = 1 or EDRRR.RR = 1), an undefined value may be written to the transmit/receive descriptor and the transmit/receive buffer during processing.

At this time, the data in the receive buffer are not guaranteed. When resuming transmission/reception of frames following a software reset, re-set the transmit/receive descriptor and the transmit buffer.