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RENESAS TECHNICAL UPDATE

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Product Category	SOC		Document No.	TN-RE*-A0007A/E	Rev.	1.00
Title	Correction of errers and addition of electrical characteristic items in RE01Group User's Manual:Hardware		Information Category	Technical Notification		
Applicable Product	RE01 Products with 256-Kbyte Flash Memory	Lot No. All	Reference Document	RE01 Group User's Manual:Hardware Rev.1.00 (R01UH0894EJ0100)		

This document describes corrections and additions to the RE01 Group User's Manual: Hardware, Rev.1.00.
The corrections are indicated in red.

No	Chapter	Title	Content
1	13	Option-Setting Memorys	Added note about ALeRASE command
	50	Flash Memory	
2	13	Power-Saving Functions	13.2.6 PWSTCR : Power Supply State Control Register The description in the PWST [2:0] bit is added.
3	36	Quad Serial Peripheral Interface (QSPI)	36.2.11 SFMSPC : SPI Protocol Control Register The SFMSDE bit is deleted.
4	51	Electrical Characteristics	Table 51.4, I/O output characteristics (V_{OH}, V_{OL}) (1) is corrected.
5	51	Electrical Characteristics	51.2.4 Permissible output current is added.
6	51	Electrical Characteristics	Table 51.29 IIC timing The condition is corrected.
7	51	Electrical Characteristics	Table 51.47 Boundary scan characteristics The condition is corrected.

For No.1, the measures to prohibit the ALeRASE command when using the RE Software Development Kit (Driver Configuration Tool, CMSIS Driver Package) are described.

No.1 Added note about ALeRASE command

Notes on the ALeRASE command will be added as follows.

(1) 7.2.5 OSIS : OCD/Serial Programmer ID Setting Register

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Before correction

Table 7.4 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection to programmer or on-chip debugger
Serial programming mode (SCI) On-chip debug mode (SWD boot mode))	0xFF, …, 0xFF (all bytes are 0xFF)	Protection disabled	The ID code is not checked, the ID code always matches, and the connection to the serial programmer or on-chip debugger is permitted.
	Bit [127] = 1, bit [126] = 1, and at least one of the 16 bytes is not 0xFF	Protection enabled	Matching ID code indicates that authentication is complete and connection to the serial programmer or the on-chip debugger is permitted. Mismatching ID code indicates transition to the ID code protection wait state. When the ID code sent from the serial programmer or the on-chip debugger is ALeRASE in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased and all bits in the OSIS register are 1. However, when the AWS.FSPR bit is 0 or security MPU is enabled, the content of the user flash area is not erased.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code indicates that authentication is complete and connection to the serial programmer or the on-chip debugger is permitted. Mismatching ID code indicates transition to the ID code protection wait state.
	Bit [127] = 0	Protection enabled	The ID code is not checked, the ID code is always mismatching, the connection to the serial programmer or the on-chip debugger is prohibited, and Renesas cannot access the test mode.

After correction

Table 7.4 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection to programmer or on-chip debugger
Serial programming mode (SCI) On-chip debug mode (SWD boot mode))	0xFF, …, 0xFF (all bytes are 0xFF)	Protection disabled	The ID code is not checked, the ID code always matches, and the connection to the serial programmer or on-chip debugger is permitted.
	Bit [127] = 1, bit [126] = 1, and at least one of the 16 bytes is not 0xFF	Protection enabled	Matching ID code indicates that authentication is complete and connection to the serial programmer or the on-chip debugger is permitted. Mismatching ID code indicates transition to the ID code protection wait state. When the ID code sent from the serial programmer or the on-chip debugger is ALeRASE in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased and all bits in the OSIS register are 1. However, when the AWS.FSPR bit is 0 or security MPU is enabled (set any value other than 0xFFFF to the SECMPUAC register), the content of the user flash area is not erased.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code indicates that authentication is complete and connection to the serial programmer or the on-chip debugger is permitted. Mismatching ID code indicates transition to the ID code protection wait state. Although on-chip debugger (OCD) cannot connect to the device when bit 127 of the OSIS register is set as 0, only ALeRASE command will be accepted. If ALeRASE command is executed, User region and Option memory region are initialized. OSIS register is initialized, so that the on-chip debugger (OCD) can be connected. To prohibit the ALeRASE command, set the AWS.FSPR bit to 0 or enable the security MPU (set any value other than 0xFFFF to the SECMPUAC register). When the AWS.FSPR bit is 1 and the security MPU is not used, the SECMPUPCS0 and SECMPUPCE0 registers specify region that do not affect operation, so set the security MPU as follows. ・SECMPUAC = 0xFEFF ・SECMPUPCS0 = 0xFFFF_FFFF ・SECMPUPCE0 = 0xFFFF_FFFF
	Bit [127] = 0	Protection enabled	The ID code is not checked, the ID code is always mismatching, the connection to the serial programmer or the on-chip debugger is prohibited, and Renesas cannot access the test mode.

(2) 50.6.5.3 Protection by ID Code

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Before correction

Table 50.16 Specifications for ID Code Protection

Operating Mode at Startup	ID Code	ALeRASE Command	ID Authentication	Connection between OCD/Serial Programmer and the device
Serial programming mode (SCI boot mode) On-chip debug mode (SWD boot mode)	Bit 127 = 1 and Bit 126 = 1	Available *1	Passed	The on-chip debugger (OCD) or the serial programmer can be connected with the device.
			Failed	The on-chip debugger (OCD) or the serial programmer cannot be connected with the device.
	Bit 127 = 1 and Bit 126 = 0	Not available	Passed	The on-chip debugger (OCD) or the serial programmer can be connected with the device.
			Failed	The on-chip debugger (OCD) or the serial programmer cannot be connected with the device.
	Bit 127 = 0	Not available	Failed	The on-chip debugger (OCD) or the serial programmer cannot be connected with the device.

Note 1. When the ID code sent from the on-chip debugger (OCD) or the serial programmer is ALeRASE in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased and all bits in the OSIS register become 1. However, the content of the user flash area is not erased when the AWS.FSPR flag is 0 or the security MPU is enabled. For details on the AWS.FSPR flag, see section 7.2.4. AWS : Access Window Setting Register.

After correction

Table 50.16 Specifications for ID Code Protection

Operating Mode at Startup	ID Code	ALeRASE Command	ID Authentication	Connection between OCD/Serial Programmer and the device
Serial programming mode (SCI boot mode) On-chip debug mode (SWD boot mode)	Bit 127 = 1 and Bit 126 = 1	Available *1	Passed	The on-chip debugger (OCD) or the serial programmer can be connected with the device.
			Failed	The on-chip debugger (OCD) or the serial programmer cannot be connected with the device.
	Bit 127 = 1 and Bit 126 = 0	Not available	Passed	The on-chip debugger (OCD) or the serial programmer can be connected with the device.
			Failed	The on-chip debugger (OCD) or the serial programmer cannot be connected with the device.
	Bit 127 = 0	Not Available *2	Failed	The on-chip debugger (OCD) or the serial programmer cannot be connected with the device.

Note 1. When the ID code sent from the on-chip debugger (OCD) or the serial programmer is ALeRASE in ASCII code (0x414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFF), the content of the user flash area is erased and all bits in the OSIS register become 1. However, the content of the user flash area is not erased when the AWS.FSPR flag is 0 or the security MPU is enabled (set any value other than 0xFFFF to the SECMPUAC register). For details on the AWS.FSPR flag, see section 7.2.4. AWS : Access Window Setting Register.

Note 2. Although on-chip debugger (OCD) cannot connect to the device when bit 127 of the OSIS register is set as 0, only ALeRASE command will be accepted. If ALeRASE command is executed, User region and Option memory region are initialized. OSIS register is initialized, so that the on-chip debugger (OCD) can be connected.
To prohibit the ALeRASE command, set the AWS.FSPR flag to 0 or enable the security MPU (set any value other than 0xFFFF to the SECMPUAC register). When the AWS.FSPR flag is 1 and the security MPU is not used, the SECMPUPCS0 and SECMPUPCE0 registers specify region that do not affect operation, so set the security MPU as follows.
・SECMPUAC = 0xFEFF, SECMPUPCS0 = 0xFFFF_FFFF, SECMPUPCE0 = 0xFFFF_FFFF

(3) Measures to prohibit the ALeRASE command when using the RE Software Development Kit

When all the following conditions are met, it is necessary to set the security MPU registers to prohibit the ALeRASE command.

[Conditions]

- Bit 127 of the OSIS register is set as 0.
- The AWS.FSPR flag is set as 1.
- Do not use the security MPU.

[Setting the security MPU registers required to prohibit the ALeRASE command]

- SECMPUAC = 0xFEFF
- SECMPUCS0 = 0xFFFF_FFFF
- SECMPUCE0 = 0xFFFF_FFFF

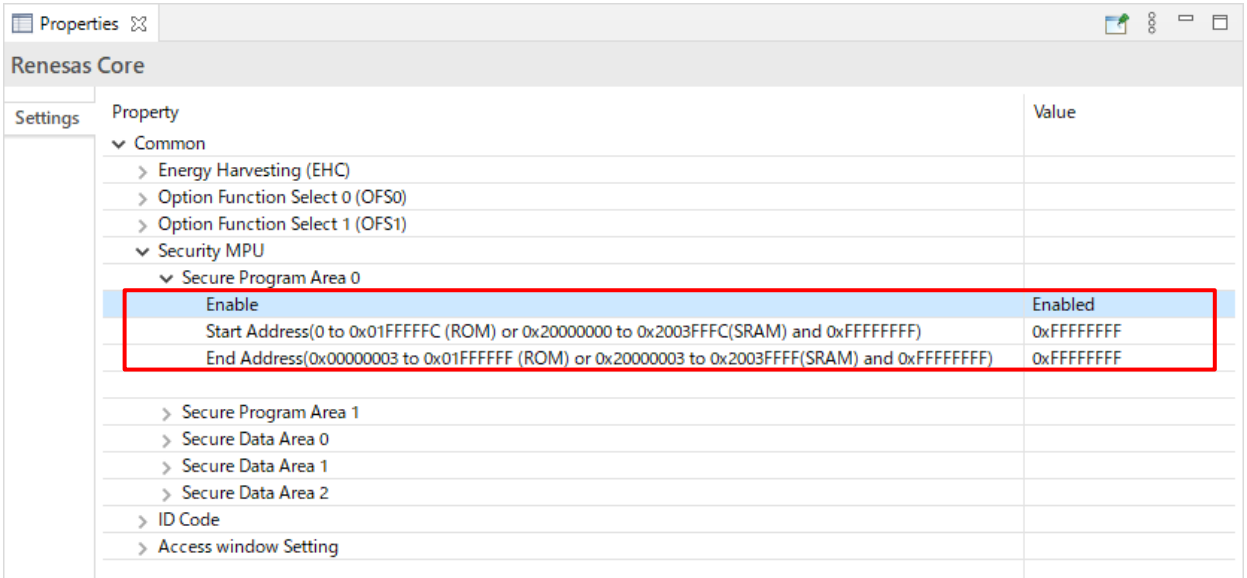
The following shows how to implement [Setting the security MPU registers required to prohibit the ALeRASE command] when using the RE Software Development Kit (Driver Configuration Tool, CMSIS Driver Package).

A) When using Driver Configuration Tool

① From the Configuration Editor window, open the properties of “Renesas Core”.

② Open “Common” > “Security MPU” > “Secure Program Area 0” and set the following values.

- Enable: Enabled
- Start Address: 0xFFFFFFFF
- End Address: 0xFFFFFFFF



B) When using the CMSIS Driver Package

Set the security MPU configuration described in the configuration definition file "r_core_cfg.h" according to the following example:

```
#define SYSTEM_CFG_SECMPU_PC0_START         (0xFFFFFFFF)
#define SYSTEM_CFG_SECMPU_PC0_END           (0xFFFFFFFF)
#define SYSTEM_CFG_SECMPU_PC1_START         (0xFFFFFFFF)
#define SYSTEM_CFG_SECMPU_PC1_END           (0xFFFFFFFF)
#define SYSTEM_CFG_SECMPU_REGION0_START      (0xFFFFFFFF)
#define SYSTEM_CFG_SECMPU_REGION0_END       (0xFFFFFFFF)
#define SYSTEM_CFG_SECMPU_REGION1_START      (0xFFFFFFFF)
#define SYSTEM_CFG_SECMPU_REGION1_END       (0xFFFFFFFF)
#define SYSTEM_CFG_SECMPU_REGION2_START      (0xFFFFFFFF)
#define SYSTEM_CFG_SECMPU_REGION2_END       (0xFFFFFFFF)
#define SYSTEM_CFG_SECMPU_CONTROL_SETTING    (0xFEFF)
```

No.2 13.2.6 PWSTCR : Power Supply State Control Register

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The description in the PWST [2:0] bit (Power Supply State Select) will be added as follows.

After correction

For details on switching of the power supply mode and power control mode, see section 13.5. Functions for Reducing Power and also section 13.7.14. Notes on Switching Power Supply, Power Control, and Low Power Consumption Modes.
While the chip is in NORMAL OPE ALLPWON with the power reduction function of flash memory enabled (OFS1.SLPWMN=0), set the frequency divisor of ICLK to 1 (before transition to VBB OPE ALLPWON, set the SCKDIVCR.ICK[2:0] bits in the clock generation circuit to 000b).

No.3 36.2.11 SFMSPC : SPI Protocol Control Register

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The SFMSPC.SFMSDE bit will be deleted and corrected as follows.

Before correction

Base address: QSPI = 0x6400_0000

Offset address: 0x030

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	SFMSDE	—	—	SFMSPI[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SFMSPI[1:0]	SPI protocol select*1 0 0: Single SPI Protocol, Extended SPI protocol 0 1: Dual SPI protocol 1 0: Quad SPI protocol 1 1: Setting prohibited	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	SFMSDE	QSPCLK extended selection bit when switching I/O of QIOn pin 0: No QSPCLK extension 1: QSPCLK expansion when switching I/O direction of QIOn pin	R/W
31:5	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The states of the QIO2 and QIO3 pins change depending on the settings of the SFMSMD.SFMRM[2:0] and SFMSPI[1:0] bits. For details, see section 36.9. QIO2 and QIO3 Pin States.

After correction

Base address: QSPI = 0x6400_0000

Offset address: 0x030

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SFMSPI[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SFMSPI[1:0]	SPI protocol select[*1] 0 0: Single SPI Protocol, Extended SPI protocol 0 1: Dual SPI protocol 1 0: Quad SPI protocol 1 1: Setting prohibited	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	—	This bit is read as 1. The write value should be 1.	R/W
31:5	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The states of the QIO2 and QIO3 pins change depending on the settings of the SFMSMD.SFMRM[2:0] and SFMSPI[1:0] bits. For details, see section 36.9. QIO2 and QIO3 Pin States.

No.4 51.2.2 I/O output characteristics (V_{OH}, V_{OL}) (1)

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Table 51.4, I/O output characteristics (V_{OH}, V_{OL}) (1) will be corrected as follows.

Before correction

Item	Register settings	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Output high level voltage	Standard drive (PmnPFS.DSCR[1:0] = 10b)	V_{OH}	VCC - 0.6	—	—	V	I_{OH} = 2mA
	High drive (PmnPFS.DSCR[1:0] = 11b)		VCC - 0.5	—	—		I_{OH} = 2mA
Output low level voltage	Standard drive (PmnPFS.DSCR[1:0] = 10b)	V_{OL}	—	—	0.6		I_{OL} = 2mA
	High drive (PmnPFS.DSCR[1:0] = 11b)		—	—	0.5		I_{OL} = 2mA

After correction

Item	Register settings	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions
Output high level voltage	Standard drive (PmnPFS.DSCR = 0b)	V_{OH}	VCC - 0.6	—	—	V	I_{OH} = 2mA
	High drive (PmnPFS.DSCR = 1b)		VCC - 0.5	—	—		I_{OH} = 2mA
Output low level voltage	Standard drive (PmnPFS.DSCR = 0b)	V_{OL}	—	—	0.6		I_{OL} = 2mA
	High drive (PmnPFS.DSCR = 1b)		—	—	0.5		I_{OL} = 2mA

No.5 51.2 DC Characteristics

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Section 51.2.4 will be added as follows.

51.2.4 Permissible output current

Table 51.6 Permissible output current

Condition: VCC = 1.62 to 3.6V

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output current (average value per pin	All output pins	Standard drive*1	I_{OH}	—	—	-2.0	mA
			I_{OL}	—	—	2.0	mA
		High drive*2	I_{OH}	—	—	4.0	mA
			I_{OL}	—	—	4.0	mA
Permissible output current (max. value per pin)	All output pins	Standard drive*1	I_{OH}	—	—	-4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*2	I_{OH}	—	—	-8.0	mA
			I_{OL}	—	—	8.0	mA
Permissible output current (max. value of total of all pins)	Maximum of all output pins*3		$\Sigma I_{OH\ (max)}$*4	—	—	-40	mA
			$\Sigma I_{OL\ (max)}$*4	—	—	40	mA

Note 1. This is the value when standard driving ability is selected in the Port Drive Capability bit in the PmnPFS register.

Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register.

Note 3. This is the value for each of IOVCC, IOVCC0, and IOVCC1. The maximum values for AVCC0 are ΣIOH = -20mA and ΣI_{OL} = 20mA.

Note 4. The maximum values for IOVCC of 72-pin WLBGA are ΣI_{OH} = -10mA and ΣI_{OL} = 10mA.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table.
The average output current indicates the average value of current measured during 100 µs.

No.6 51.3.12 IIC Timing

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The condition in Table 51.29, IIC timing will be deleted and corrected as follows.

Before correction

Condition: VCC = 3.0 to 3.6 V, V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3, V_{OH} = 0.6 V, I_{OL} = 6 mA

Condition: Normal drive output is selected in the drive capability control bits in PmnPFS register. (PmnPFS.DSCR[1:0] = 10b)

After correction

Condition: VCC = 3.0 to 3.6 V, V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3, V_{OH} = 0.6 V, I_{OL} = 6 mA

No.7 51.12 Boundary Scan Characteristics

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The condition in Table 51.47, Boundary scan characteristics will be corrected as follows.

Before correction

Condition: High drive output is selected in the drive capability control bits in PmnPFS register. (PmnPFS.DSCR[1:0] = 11b)

After correction

Condition: High drive output is selected in the drive capability control bits in PmnPFS register. (PmnPFS.DSCR = 1b)

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