Date: Jul. 14, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0088A/E	Rev.	1.00
Title	Correction on DOC interrupt enable setting		Information Category	Technical Notification		
Applicable Product	RA6T2 Group	Lot No. All	Reference Document	RA6T2 Group User's Manual : Hardware Rev.1.30		

This document describes correction on DOC interrupt enable setting.

Changes list is as follows.

1) Figure 40.1 DOC block diagram
2) 40.2.1 DOCR : DOC Control Register
3) 40.3.1 Data Comparison Mode
4) Figure 40.2 Example of Operation in Data Comparison Mode (Detection condition: Mismatch)
   Figure 40.3 Example of Operation in Data Comparison Mode (Detection condition: Match)
   Figure 40.4 Example of Operation in Data Comparison Mode (Detection condition: Lower)
   Figure 40.5 Example of Operation in Data Comparison Mode (Detection condition: Upper)
   Figure 40.6 Example of Operation in Data Comparison Mode (Detection condition: Inside window)
   Figure 40.7 Example of Operation in Data Comparison Mode (Detection condition: Outside window)
5) 40.3.2 Data Addition Mode
6) Figure 40.8 Example of Operation in Data Addition Mode
7) 40.3.3 Data Subtraction Mode
8) Figure 40.9 Example of Operation in Data Subtraction Mode
9) 40.4 Interrupt Source
10) 40.6 Interrupt Handling and Event Linking

Before correction

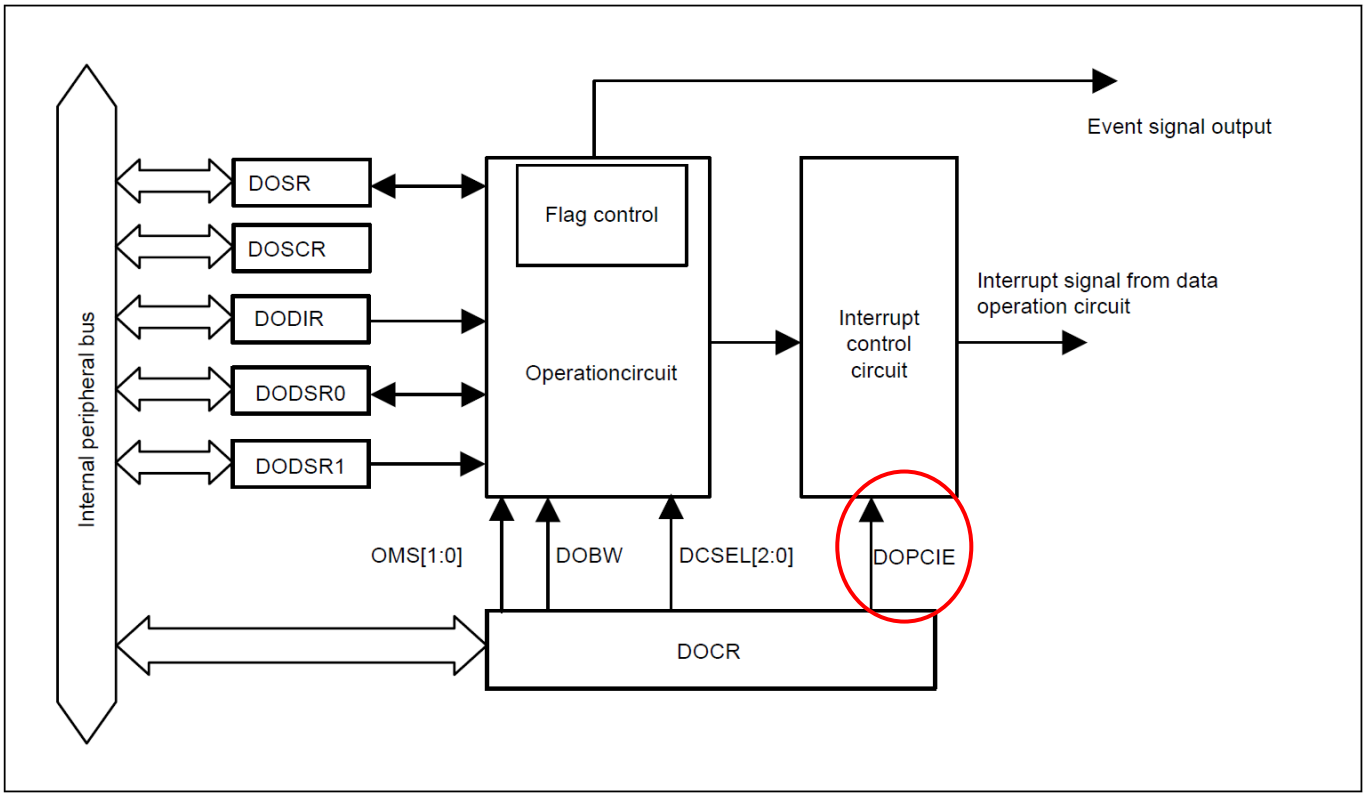

Figure 40.1 DOC block diagram

After correction

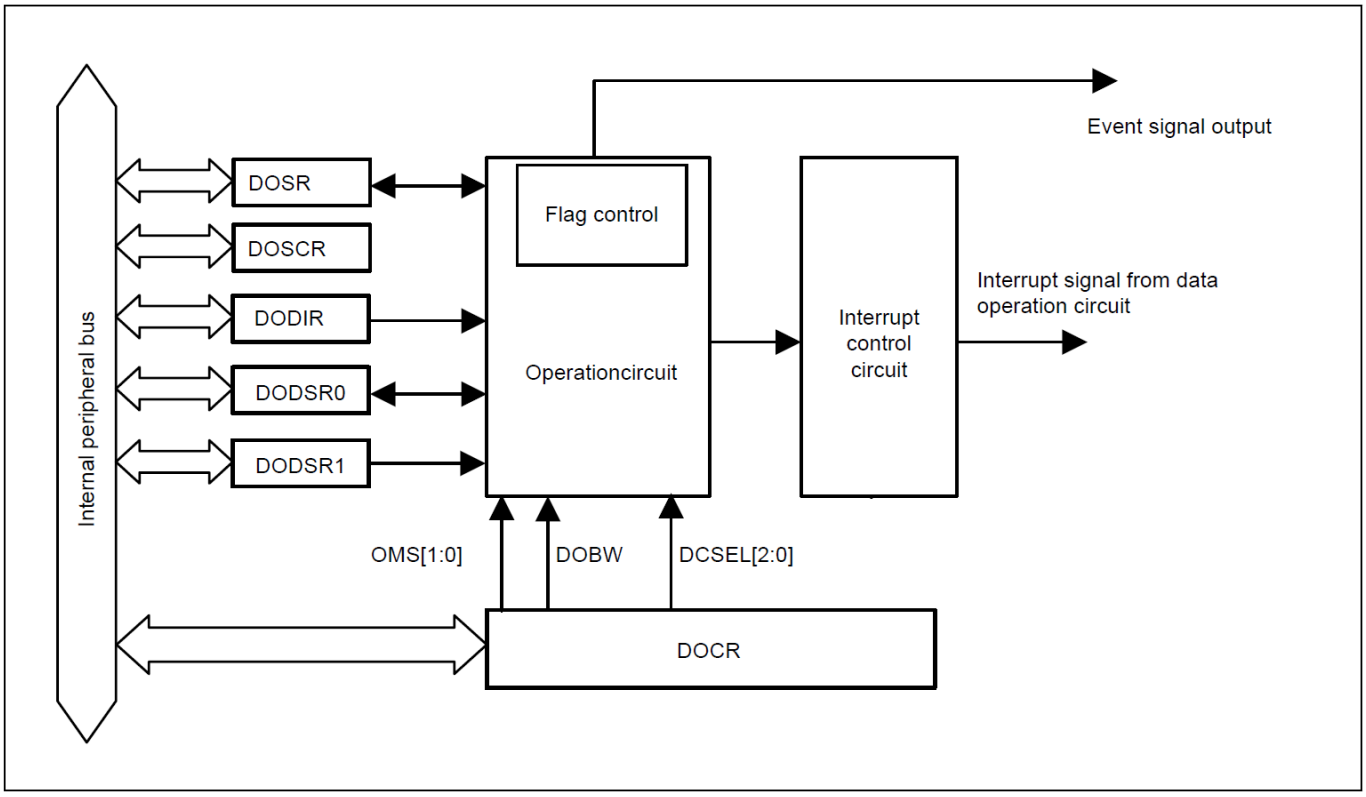

Figure 40.1 DOC block diagram

Before correction

40.2.1 DOCR : DOC Control Register

Base address: DOC_B = 0x4010_9000
Offset address: 0x00

Bit position	7	6	5	4	3	2	1	0
Bit field	DOPCIE	DCSEL[2:0]			DOBW	-	OMS[1:0]	
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7	DOPCIE	Data Operation Circuit Interrupt Enable 0: Disables interrupts from the data operation circuit. 1: Enables interrupts from the data operation circuit.	R/W

Note 1. Valid only when data comparison mode is selected.

The DOCR is a register which can set the operation mode of data operation circuit and interrupt enable/disable.

OMS[1:0] bits (Operating Mode Select)
These bits select the operating mode of the data operation circuit.

DOBW bit (Data Operation Bit Width Select)
This bit selects the bit width of data operation.

DCSEL[2:0] bits (Detection Condition Select)
These bits are valid only when data comparison mode is selected.
These bits select the condition for detection in data comparison mode.

DOPCIE bit (Data Operation Circuit Interrupt Enable)
Setting this bit to 1 enables interrupts from the data operation circuit.

After correction

40.2.1 DOCR : DOC Control Register

Base address: DOC_B = 0x4010_9000
Offset address: 0x00

Bit position	7	6	5	4	3	2	1	0
Bit field	-	DCSEL[2:0]			DOBW	-	OMS[1:0]	
Value after reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7	-	This bit is read as 0. The write value should be 0.	R/W

Note 1. Valid only when data comparison mode is selected.

The DOCR is a register which can set the operation mode of data operation circuit and interrupt enable/disable.

OMS[1:0] bits (Operating Mode Select)
These bits select the operating mode of the data operation circuit.

DOBW bit (Data Operation Bit Width Select)
This bit selects the bit width of data operation.

DCSEL[2:0] bits (Detection Condition Select)
These bits are valid only when data comparison mode is selected.
These bits select the condition for detection in data comparison mode.

(Deleted)

Before correction

40.3.1 Data Comparison Mode

Figure 40.2 to Figure 40.7 shows an example of the steps involved in data comparison mode operation by the data operation circuit.

The following is an example of operation when the bit width of data operation is 32-bit.

1. Writing 00b to the DOCR.OMS[1:0] bits selects data comparison mode, and setting the DOCR.DCSEL[2:0] to selects detection condition.
2. The 32-bit reference data is set in DODSR0 and DODSR1.*1
3. 32-bit data for comparison is written to DODIR.
4. If a value written to DODIR match the detection condition set by DOCR.DCSEL[2:0], the DOCR.DOPCF flag is set to 1 and an ELC event is generated. When the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also generated.

After correction

40.3.1 Data Comparison Mode

Figure 40.2 to Figure 40.7 shows an example of the steps involved in data comparison mode operation by the data operation circuit.

The following is an example of operation when the bit width of data operation is 32-bit.

1. Writing 00b to the DOCR.OMS[1:0] bits selects data comparison mode, and setting the DOCR.DCSEL[2:0] to selects detection condition.
2. The 32-bit reference data is set in DODSR0 and DODSR1.*1
3. 32-bit data for comparison is written to DODIR.
4. If a value written to DODIR match the detection condition set by DOCR.DCSEL[2:0], the DOCR.DOPCF flag is set to 1 and an ELC event and Data operation circuit interrupt are generated.

Before correction

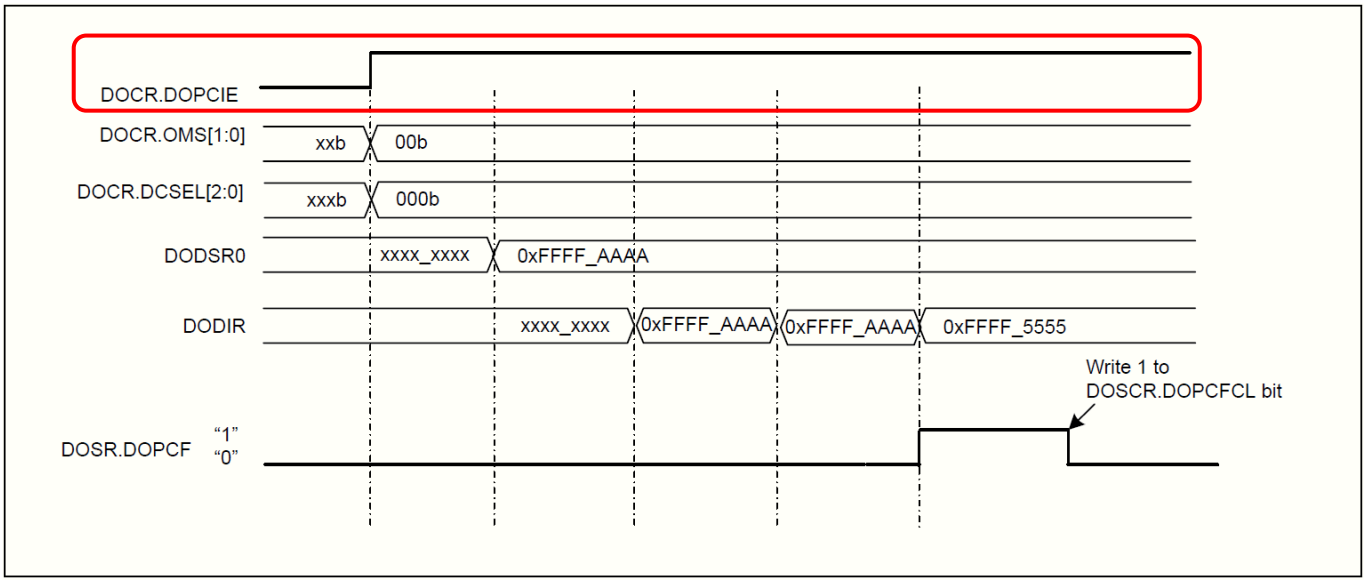

Figure 40.2 Example of Operation in Data Comparison Mode (Detection condition: Mismatch)

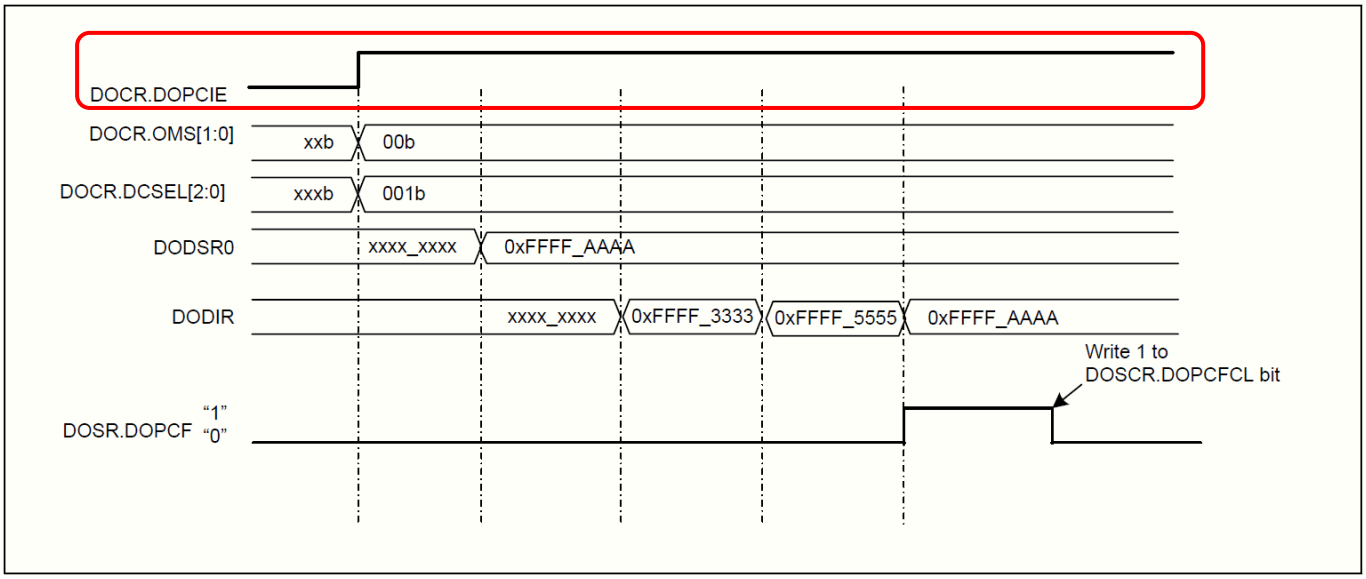

Figure 40.3 Example of Operation in Data Comparison Mode (Detection condition: Match)

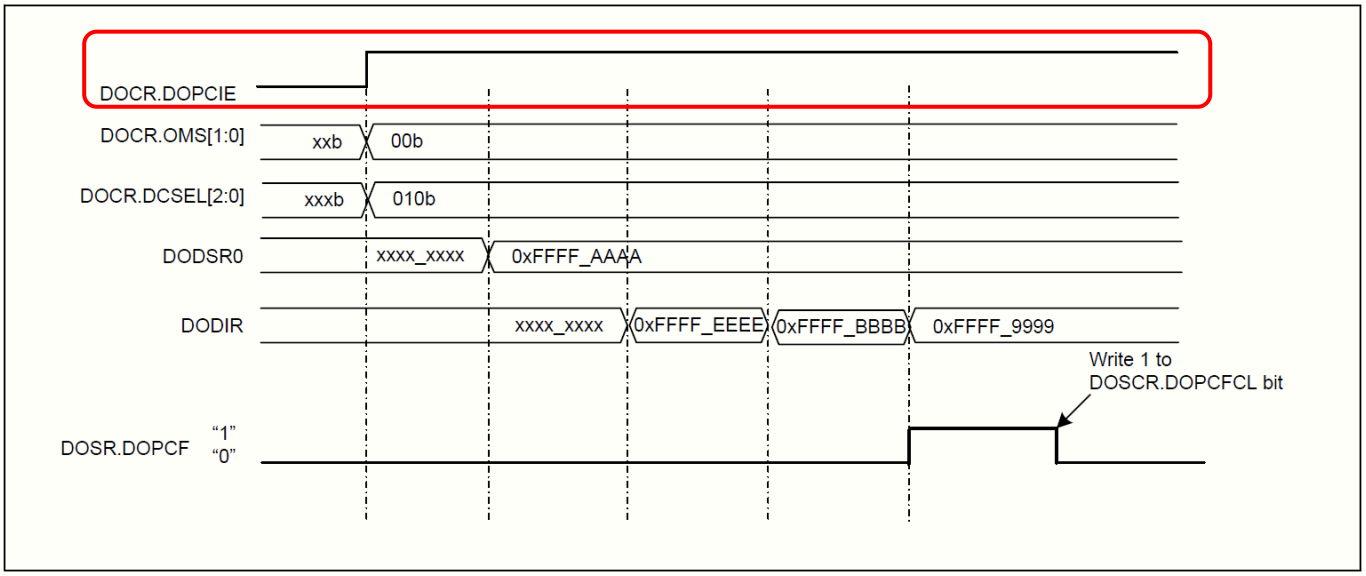

Figure 40.4 Example of Operation in Data Comparison Mode (Detection condition: Lower)

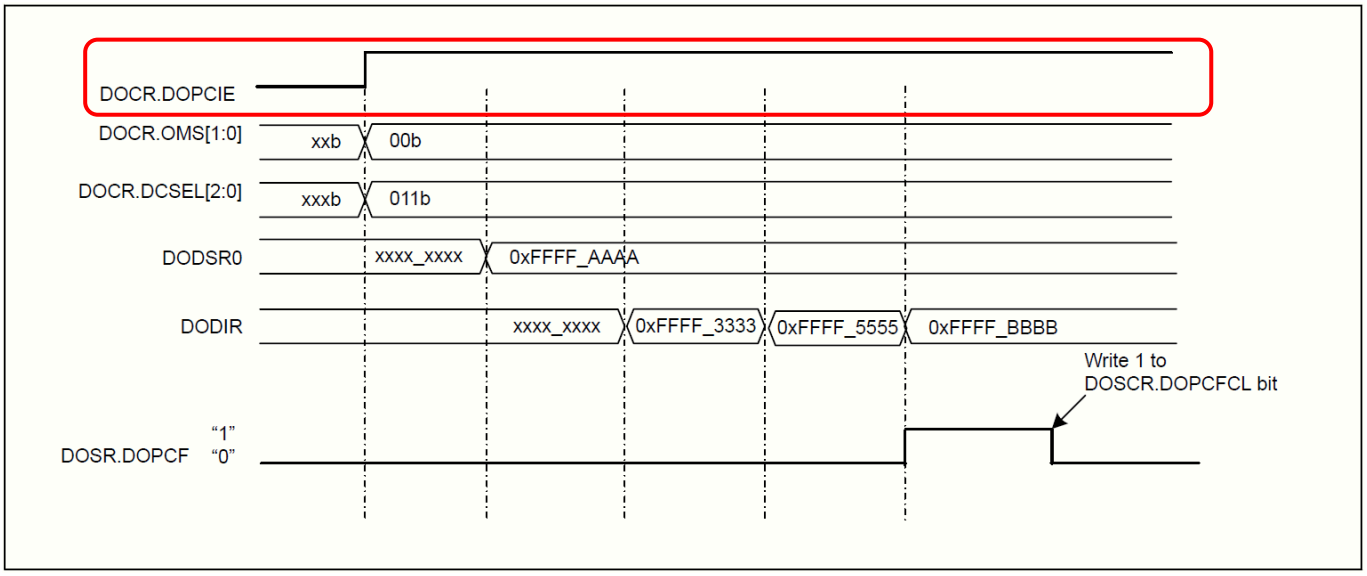

Figure 40.5 Example of Operation in Data Comparison Mode (Detection condition: Upper)

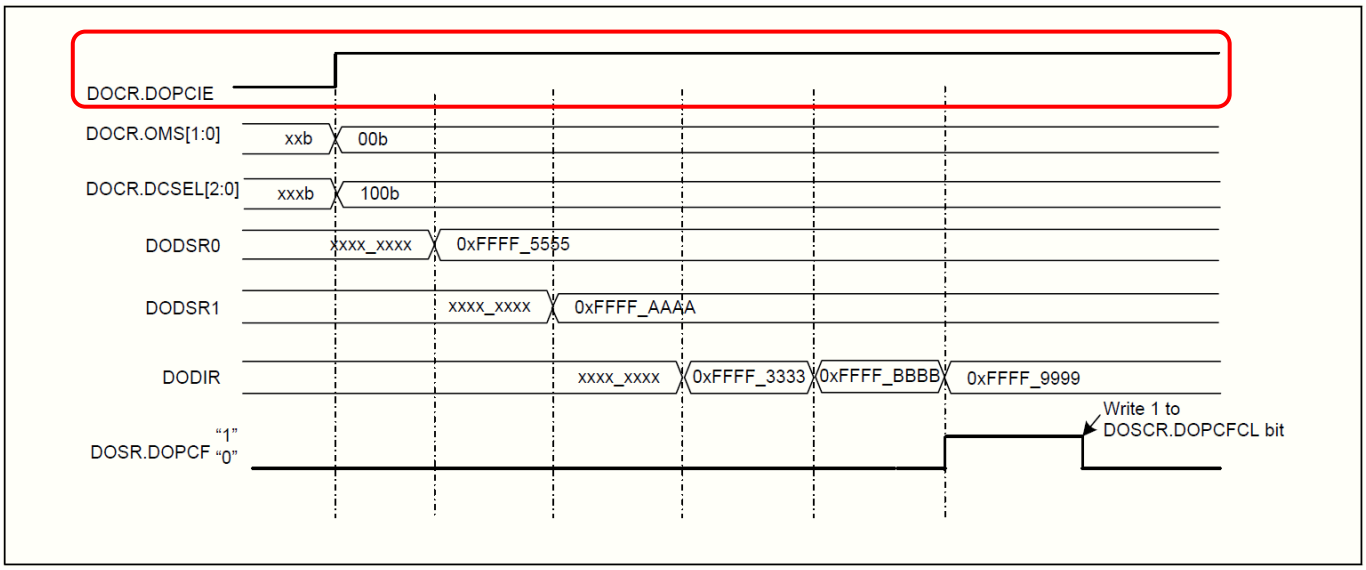

Figure 40.6 Example of Operation in Data Comparison Mode (Detection condition: Inside window)

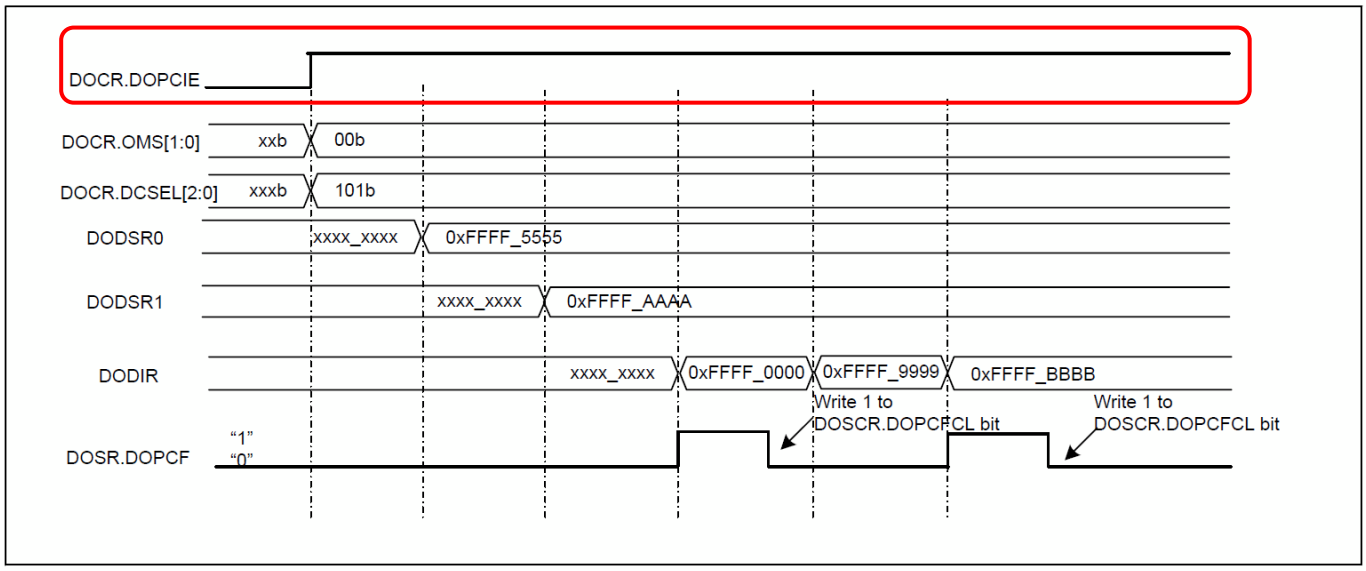

Figure 40.7 Example of Operation in Data Comparison Mode (Detection condition: Outside window)

After correction

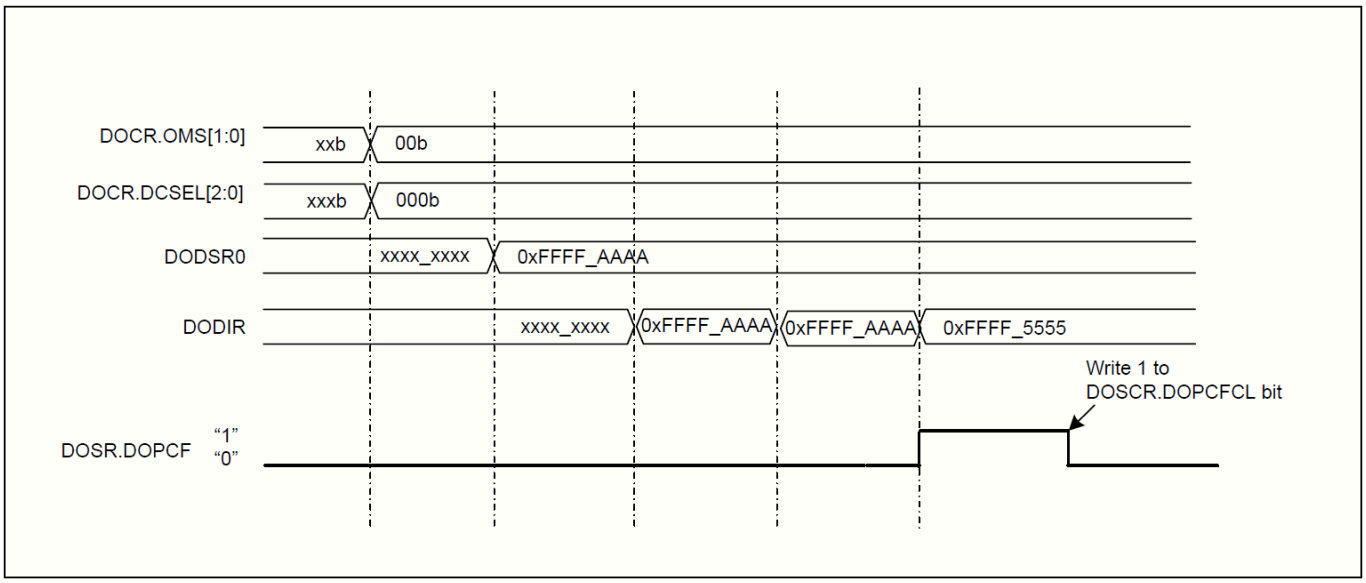

Figure 40.2 Example of Operation in Data Comparison Mode (Detection condition: Mismatch)

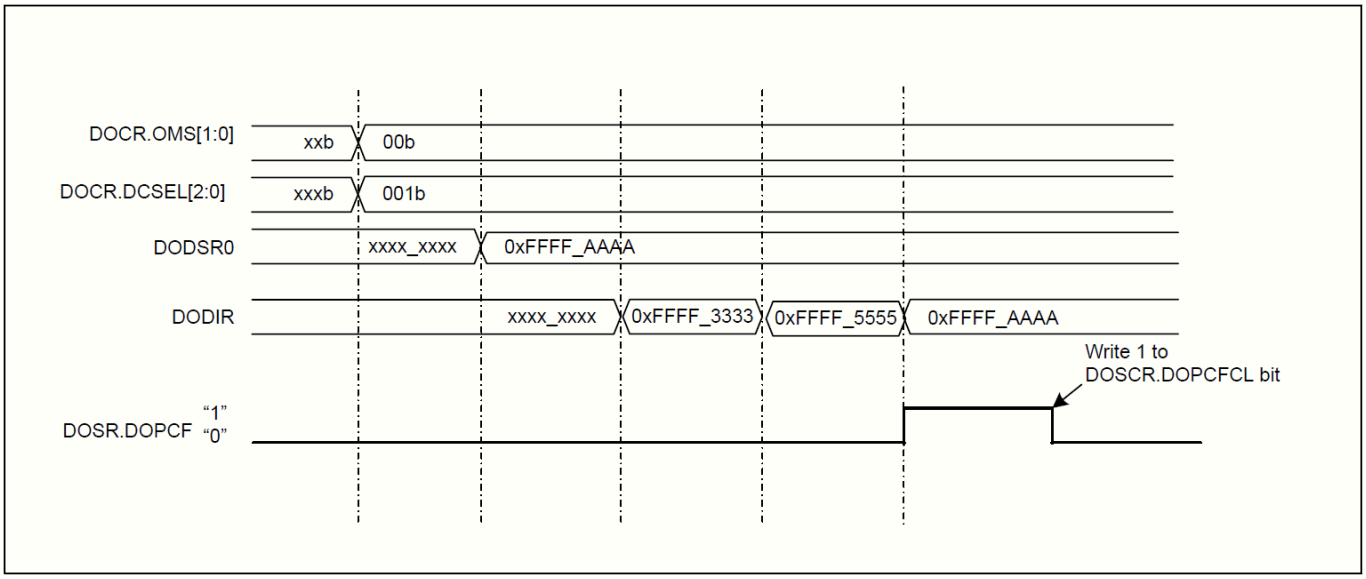

Figure 40.3 Example of Operation in Data Comparison Mode (Detection condition: Match)

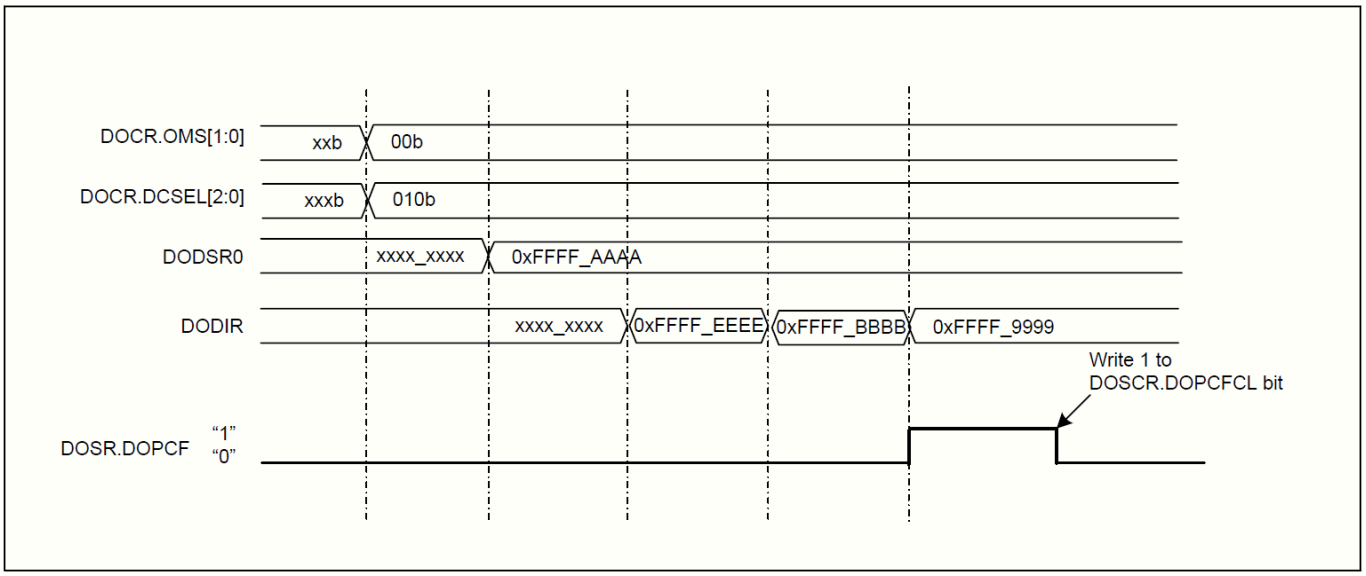

Figure 40.4 Example of Operation in Data Comparison Mode (Detection condition: Lower)

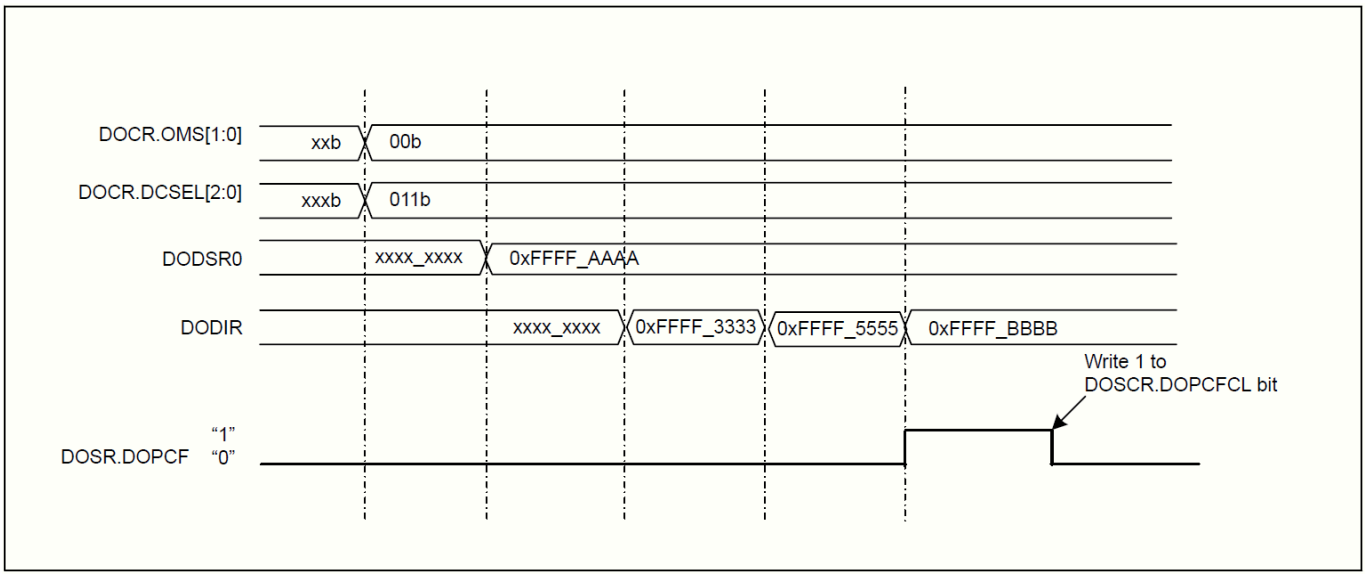

Figure 40.5 Example of Operation in Data Comparison Mode (Detection condition: Upper)

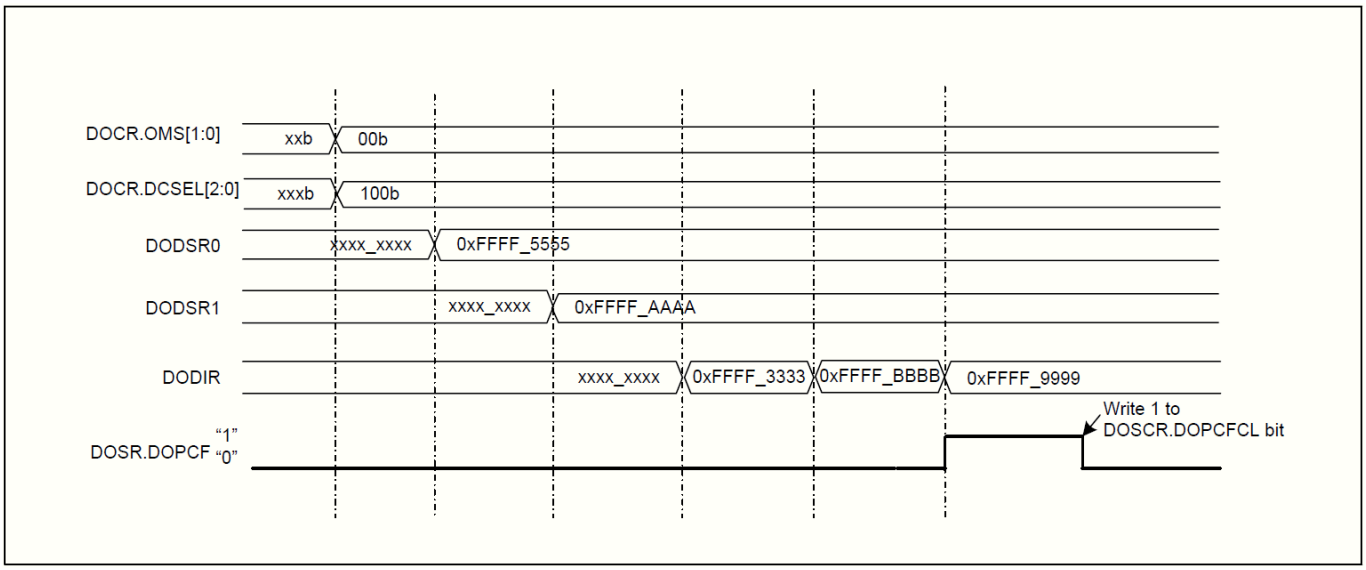

Figure 40.6 Example of Operation in Data Comparison Mode (Detection condition: Inside window)

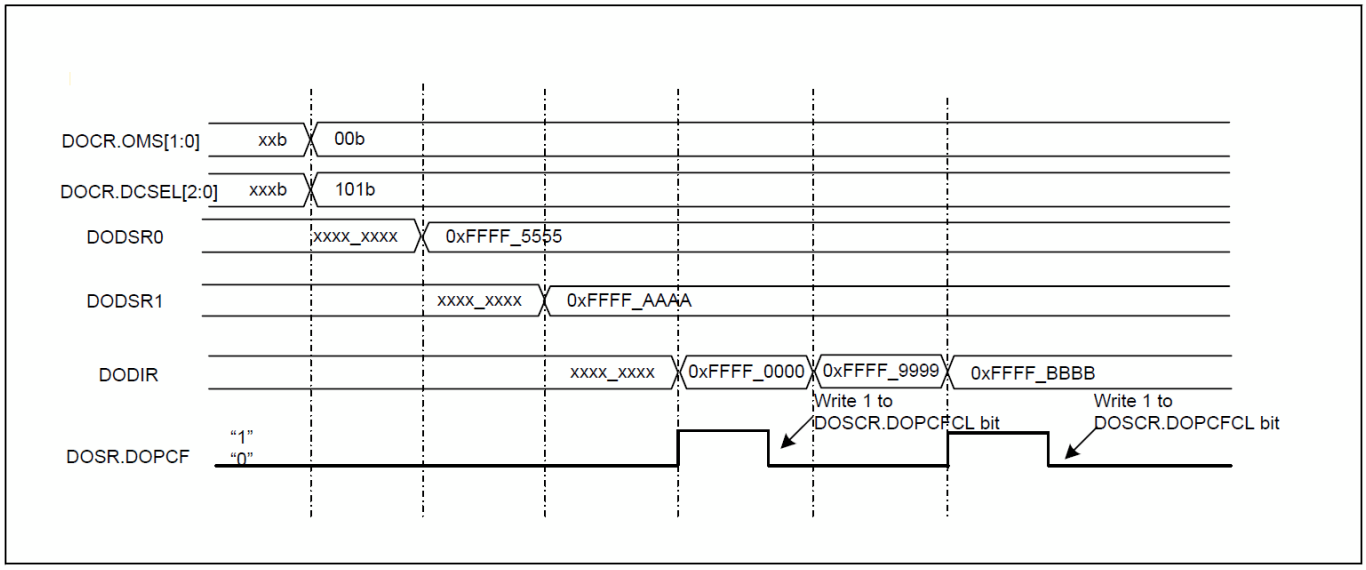

Figure 40.7 Example of Operation in Data Comparison Mode (Detection condition: Outside window)

Before correction

40.3.2 Data Addition Mode

Figure 40.8 shows an example of the steps involved in data addition mode *1 operation by the data operation circuit.
The following is an example of operation when the bit width of data operation is 32-bit.

1. Writing 01b to the DOCR.OMS[1:0] bits selects data addition mode.
2. 32-bit data is set in the DODSR0 register as the initial value.
3. 32-bit data to be added is written to DODIR. The result of the operation is stored in DODSR0.
4. Writing of 32-bit data continues until all data for addition have been written to DODIR.
5. If the result of an operation is greater than 0xFFFF_FFFF, the DOSR.DOPCF flag is set to 1 and an ELC event is generated. When the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also generated.

After correction

40.3.2 Data Addition Mode

Figure 40.8 shows an example of the steps involved in data addition mode *1 operation by the data operation circuit.
The following is an example of operation when the bit width of data operation is 32-bit.

1. Writing 01b to the DOCR.OMS[1:0] bits selects data addition mode.
2. 32-bit data is set in the DODSR0 register as the initial value.
3. 32-bit data to be added is written to DODIR. The result of the operation is stored in DODSR0.
4. Writing of 32-bit data continues until all data for addition have been written to DODIR.
5. If the result of an operation is greater than 0xFFFF_FFFF, the DOSR.DOPCF flag is set to 1 and an ELC event and Data operation circuit interrupt are generated.

Before correction

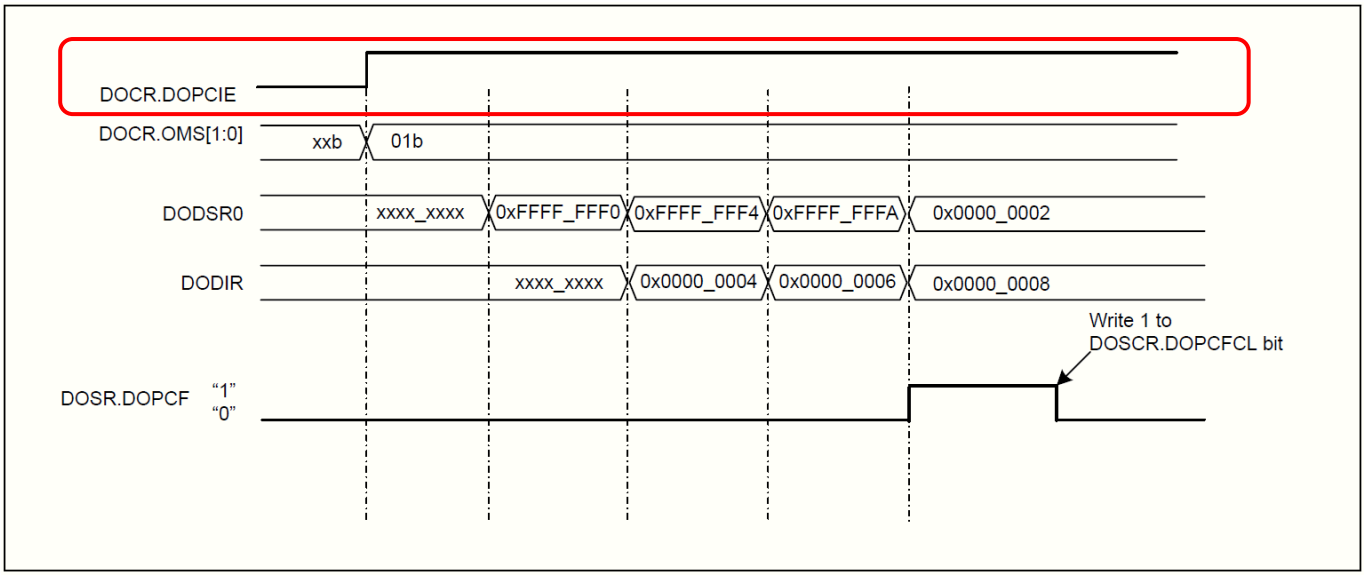

Figure 40.8 Example of Operation in Data Addition Mode

After correction

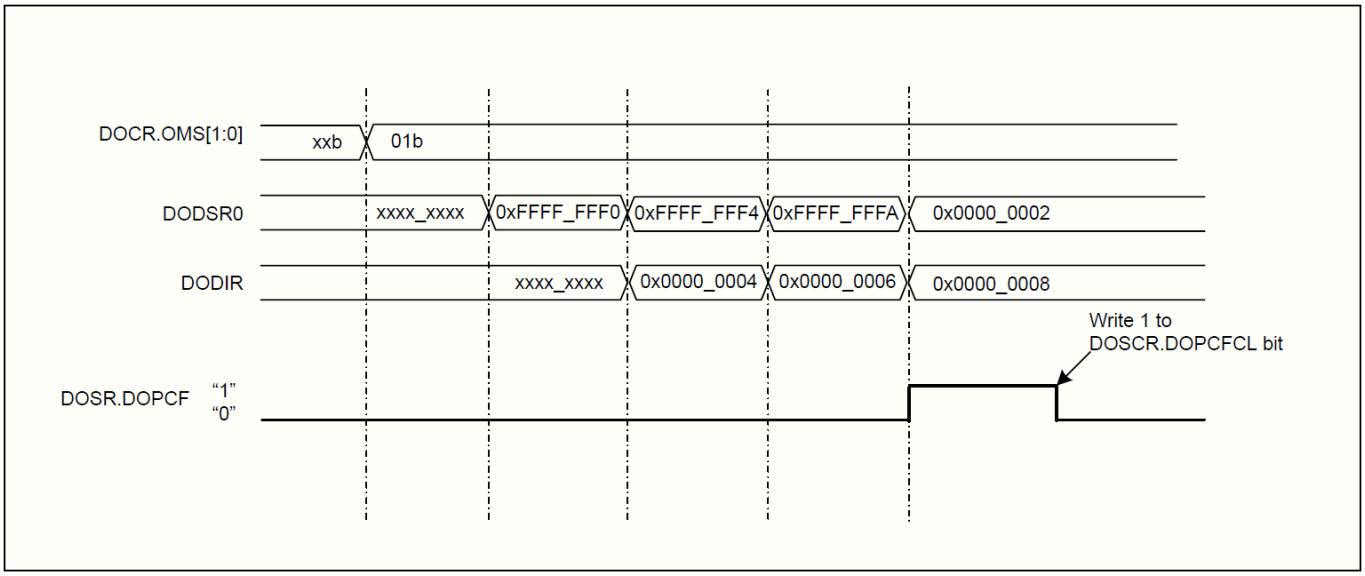

Figure 40.8 Example of Operation in Data Addition Mode

Before correction

40.3.3 Data Subtraction Mode

Figure 40.9 shows an example of the steps involved in data subtraction mode *1 operation by the data operation circuit.
The following is an example of operation when the bit width of data operation is 32-bit.

1. Writing 10b to the DOCR.OMS[1:0] bits selects data subtraction mode.
2. 32-bit data is set in the DODSR0 register as the initial value.
3. 32-bit data to be subtracted is written to DODIR. The result of the operation is stored in DODSR0.
4. Writing of 32-bit data continues until all data for subtraction have been written to DODIR.
5. If the result of an operation is less than 0x0000_0000, the DOSR.DOPCF flag is set to 1 and an ELC event is generated. When the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also generated.

After correction

40.3.3 Data Subtraction Mode

Figure 40.9 shows an example of the steps involved in data subtraction mode *1 operation by the data operation circuit.
The following is an example of operation when the bit width of data operation is 32-bit.

1. Writing 10b to the DOCR.OMS[1:0] bits selects data subtraction mode.
2. 32-bit data is set in the DODSR0 register as the initial value.
3. 32-bit data to be subtracted is written to DODIR. The result of the operation is stored in DODSR0.
4. Writing of 32-bit data continues until all data for subtraction have been written to DODIR.
5. If the result of an operation is less than 0x0000_0000, the DOSR.DOPCF flag is set to 1 and an ELC event and Data operation circuit interrupt are generated.

Before correction

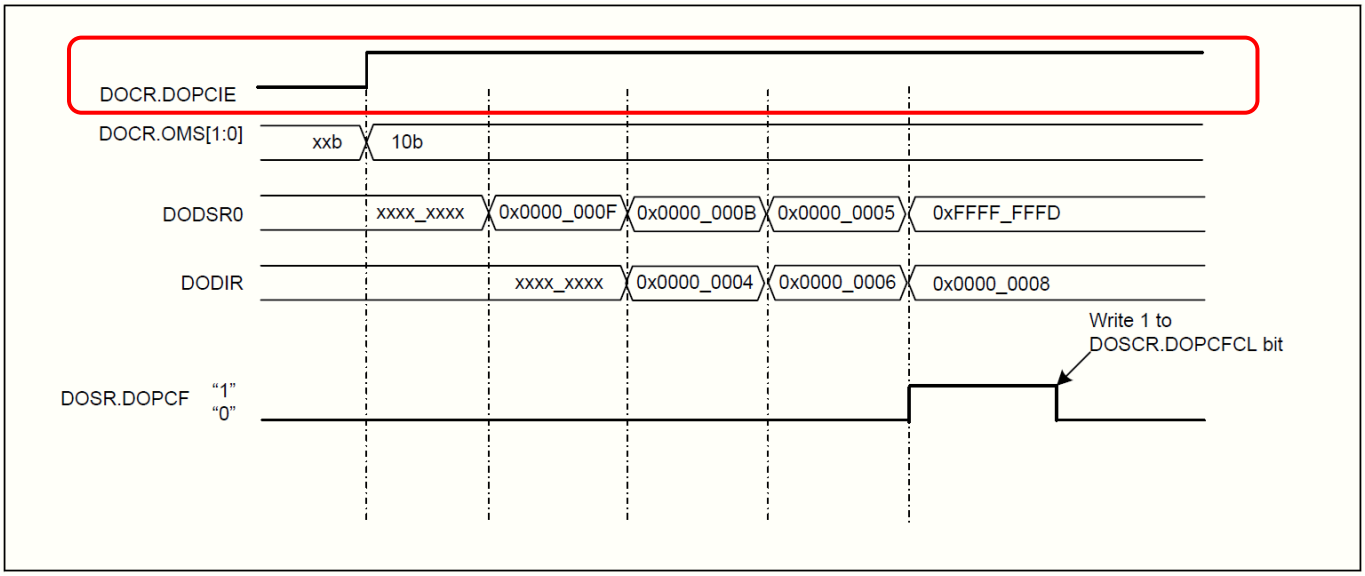

Figure 40.9 Example of Operation in Data Subtraction Mode

After correction

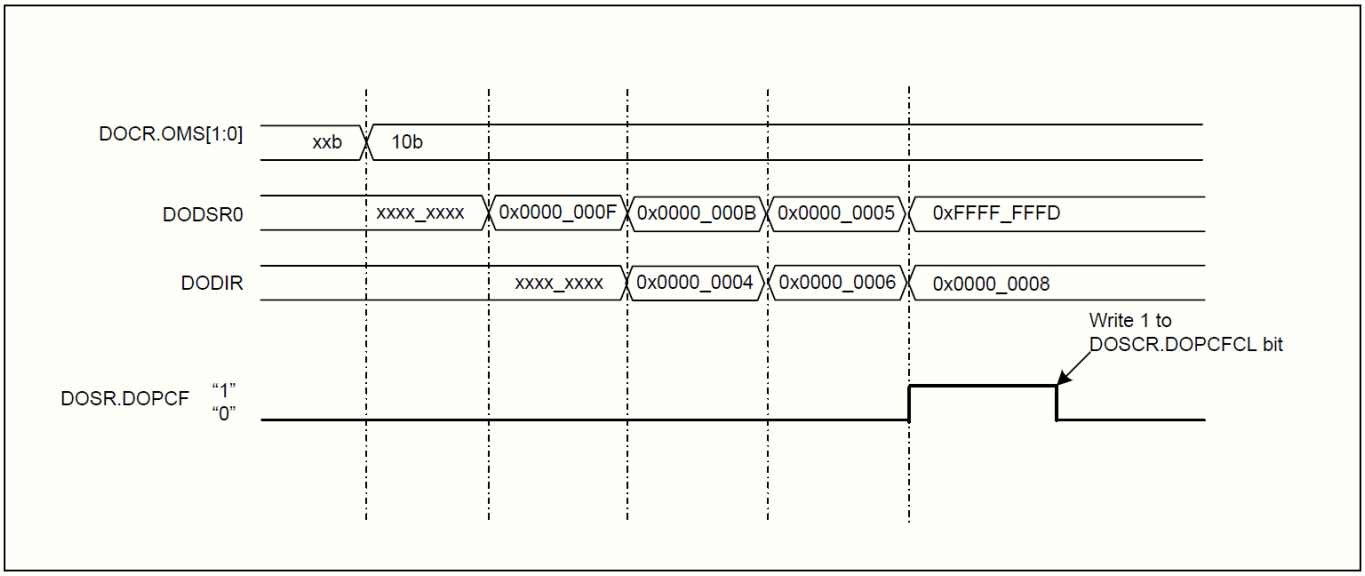

Figure 40.9 Example of Operation in Data Subtraction Mode

Before correction

40.4 Interrupt Source

The data operation circuit generates the data operation circuit interrupt (DOC_DOPCI) as an interrupt request. When an interrupt source is generated, the data operation circuit flag corresponding to the interrupt is set to 1, when the data operation circuit interrupt enable bit is enabled, interrupt request signal is generated. Table 40.2 describes the interrupt request.

After correction

40.4 Interrupt Source

The data operation circuit generates the data operation circuit interrupt (DOC_DOPCI) as an interrupt request. When an interrupt source is generated, the data operation circuit flag corresponding to the interrupt is set to 1, interrupt request signal is generated. Table 40.2 describes the interrupt request.

Before correction

40.6 Interrupt Handling and Event Linking

The DOC has a bit to enable or disable interrupts. An interrupt request signal is output for the CPU when an interrupt source is generated while the corresponding enable bit is enabled.
In contrast, an event link output signal is sent to other modules as an event signal via the ELC when an interrupt source is generated, regardless of the setting of the corresponding interrupt enable bit.

After correction

(Deleted)