Date: Sep. 5, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0097A/E	Rev.	1.00
Title	Correction for “CoreSight ROM table” in RA2 group User’s Manual		Information Category	Technical Notification		
Applicable Product	RA Family RA2A1/RA2L1/RA2E1/RA2E2 Group	Lot No. All lots	Reference Document	-Renesas RA2A1 Group User’s Manual: Hardware R01UH0888EJ0110 Rev.1.10 -Renesas RA2L1 Group User’s Manual: Hardware R01UH0853EJ0130 Rev.1.30 -Renesas RA2E1 Group User’s Manual: Hardware R01UH0852EJ0130 Rev.1.30 -Renesas RA2E2 Group User’s Manual: Hardware R01UH0919EJ0120 Rev.1.20		

CoreSight ROM table errata in the chapter of “CPU” are corrected.

The details are shown from the next page.

Group:RA2A1

2. CPU

Before

(1) 2.6.4.1 ROM entries sentence and title of Table 2.7 “CoreSight ROM Table”

2.6.4.1 ROM entries

Table 2.7 shows the ROM entries in the CoreSight ROM Table. The OCD emulator can use the ROM entries to determine which components are implemented in a system. See reference 4. for details.

Table 2.7 CoreSight ROM Table

#	Address	Access size	R/W	Value	Target module pointer
0	4001 A000h	32 bits	R	9FFF 4003h	SCS
1	4001 A004h	32 bits	R	9FFE 7003h	DWT
2	4001 A008h	32 bits	R	9FFE 8003h	FPB
3	4001 A00Ch	32 bits	R	FFFF F003h	MTB
4	4001 A010h	32 bits	R	0000 0000h	End of entries

(2) Registers name and Address of table 2.8

Table 2.8 CoreSight component registers in the CoreSight ROM Table

Name	Address	Access size	R/W	Initial value
DEVTYPE	E00F FFCCh	32 bits	R	0000 0001h
PID4	E00F FFD0h	32 bits	R	0000 0004h
PID5	E00F FFD4h	32 bits	R	0000 0000h
PID6	E00F FFD8h	32 bits	R	0000 0000h
PID7	E00F FFDCh	32 bits	R	0000 0000h
PID0	E00F FFE0h	32 bits	R	0000 001Bh
PID1	E00F FFE4h	32 bits	R	0000 0030h
PID2	E00F FFE8h	32 bits	R	0000 000Ah
PID3	E00F FFECh	32 bits	R	0000 0000h
CID0	E00F FFF0h	32 bits	R	0000 000Dh
CID1	E00F FFF4h	32 bits	R	0000 0010h
CID2	E00F FFF8h	32 bits	R	0000 0005h
CID3	E00F FFFCh	32 bits	R	0000 00B1h

After

(1) Deleted “in the CoreSight ROM Table” in the 2.6.4.1 ROM entries sentence and correct title of Table 2.7 to “ROM entries”

2.6.4.1 ROM entries

Table 2.7 shows the ROM entries. The OCD emulator can use the ROM entries to determine which components are implemented in a system. See reference 4. for details.

Table 2.7 ROM entries

#	Address	Access size	R/W	Value	Target module pointer
0	4001 A000h	32 bits	R	9FFF 4003h	SCS
1	4001 A004h	32 bits	R	9FFE 7003h	DWT
2	4001 A008h	32 bits	R	9FFE 8003h	FPB
3	4001 A00Ch	32 bits	R	FFFF F003h	MTB
4	4001 A010h	32 bits	R	0000 0000h	End of entries

(2) Correct registers name and address of table 2.8 as below

Table 2.8 CoreSight component registers in the CoreSight ROM Table

Name	Address	Access size	R/W	Initial value
MEMTYPE	0x4001_AFCC	32 bits	R	0000 0001h
PIDR4	0x4001_AFD0	32 bits	R	0000 0004h
PIDR5	0x4001_AFD4	32 bits	R	0000 0000h
PIDR6	0x4001_AFD8	32 bits	R	0000 0000h
PIDR7	0x4001_AFDC	32 bits	R	0000 0000h
PIDR0	0x4001_AFE0	32 bits	R	0000 001Bh
PIDR1	0x4001_AFE4	32 bits	R	0000 0030h
PIDR2	0x4001_AFE8	32 bits	R	0000 000Ah
PIDR3	0x4001_AFEC	32 bits	R	0000 0000h
CIDR0	0x4001_AFF0	32 bits	R	0000 000Dh
CIDR1	0x4001_AFF4	32 bits	R	0000 0010h
CIDR2	0x4001_AFF8	32 bits	R	0000 0005h
CIDR3	0x4001_AFFC	32 bits	R	0000 00B1h

(3) Registers name of table 2.10

Table 2.10 DBGREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	4001 BFD0h	32 bits	R	0000 0004h
PID5	4001 BFD4h	32 bits	R	0000 0000h
PID6	4001 BFD8h	32 bits	R	0000 0000h
PID7	4001 BFDCh	32 bits	R	0000 0000h
PID0	4001 BFE0h	32 bits	R	0000 0005h
PID1	4001 BFE4h	32 bits	R	0000 0030h
PID2	4001 BFE8h	32 bits	R	0000 001Ah
PID3	4001 BFECh	32 bits	R	0000 0000h
CID0	4001 BFF0h	32 bits	R	0000 000Dh
CID1	4001 BFF4h	32 bits	R	0000 00F0h
CID2	4001 BFF8h	32 bits	R	0000 0005h
CID3	4001 BFFCh	32 bits	R	0000 00B1h

(4) Registers name of table 2.12

Table 2.12 OCDREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	8000 0FD0h	32 bits	R	0000 0004h
PID5	8000 0FD4h	32 bits	R	0000 0000h
PID6	8000 0FD8h	32 bits	R	0000 0000h
PID7	8000 0FDCh	32 bits	R	0000 0000h
PID0	8000 0FE0h	32 bits	R	0000 0004h
PID1	8000 0FE4h	32 bits	R	0000 0030h
PID2	8000 0FE8h	32 bits	R	0000 000Ah
PID3	8000 0FECh	32 bits	R	0000 0000h
CID0	8000 0FF0h	32 bits	R	0000 000Dh
CID1	8000 0FF4h	32 bits	R	0000 00F0h
CID2	8000 0FF8h	32 bits	R	0000 0005h
CID3	8000 0FFCh	32 bits	R	0000 00B1h

(3) Correct registers name of table 2.10 as below

Table 2.10 DBGREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PIDR4	4001 BFD0h	32 bits	R	0000 0004h
PIDR5	4001 BFD4h	32 bits	R	0000 0000h
PIDR6	4001 BFD8h	32 bits	R	0000 0000h
PIDR7	4001 BFDCh	32 bits	R	0000 0000h
PIDR0	4001 BFE0h	32 bits	R	0000 0005h
PIDR1	4001 BFE4h	32 bits	R	0000 0030h
PIDR2	4001 BFE8h	32 bits	R	0000 001Ah
PIDR3	4001 BFECh	32 bits	R	0000 0000h
CIDR0	4001 BFF0h	32 bits	R	0000 000Dh
CIDR1	4001 BFF4h	32 bits	R	0000 00F0h
CIDR2	4001 BFF8h	32 bits	R	0000 0005h
CIDR3	4001 BFFCh	32 bits	R	0000 00B1h

(4) Correct registers name of table 2.12 as below

Table 2.12 OCDREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PIDR4	8000 0FD0h	32 bits	R	0000 0004h
PIDR5	8000 0FD4h	32 bits	R	0000 0000h
PIDR6	8000 0FD8h	32 bits	R	0000 0000h
PIDR7	8000 0FDCh	32 bits	R	0000 0000h
PIDR0	8000 0FE0h	32 bits	R	0000 0004h
PIDR1	8000 0FE4h	32 bits	R	0000 0030h
PIDR2	8000 0FE8h	32 bits	R	0000 000Ah
PIDR3	8000 0FECh	32 bits	R	0000 0000h
CIDR0	8000 0FF0h	32 bits	R	0000 000Dh
CIDR1	8000 0FF4h	32 bits	R	0000 00F0h
CIDR2	8000 0FF8h	32 bits	R	0000 0005h
CIDR3	8000 0FFCh	32 bits	R	0000 00B1h

Group:RA2L1

2. CPU

Before

(1) 2.5.4.1 ROM entries sentence and title of Table 2.7 “CoreSight ROM Table”

2.5.4.1 ROM entries

Table 2.7 shows the ROM entries in the CoreSight ROM Table. The OCD emulator can use the ROM entries to determine which components are implemented in a system. See reference 4. for details.

Table 2.7 CoreSight ROM Table

#	Address	Access size	R/W	Value	Target module pointer
0	0x4001_A000	32 bits	R	0x9FFF4003	SCS
1	0x4001_A004	32 bits	R	0x9FFE7003	DWT
2	0x4001_A008	32 bits	R	0x9FFE8003	FPB
3	0x4001_A00C	32 bits	R	0xFFFFF003	MTB
4	0x4001_A010	32 bits	R	0x00000000	End of entries

(2) Registers name and Address of table 2.8

Table 2.8 CoreSight component registers in the CoreSight ROM Table (1 of 2)

Name	Address	Access size	R/W	Initial value
DEVTYPE	0xE00F_FFCC	32 bits	R	0x00000001
PID4	0xE00F_FFD0	32 bits	R	0x00000004
PID5	0xE00F_FFD4	32 bits	R	0x00000000
PID6	0xE00F_FFD8	32 bits	R	0x00000000

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PID7	0xE00F_FFDC	32 bits	R	0x00000000
PID0	0xE00F_FFE0	32 bits	R	0x0000002F
PID1	0xE00F_FFE4	32 bits	R	0x00000030
PID2	0xE00F_FFE8	32 bits	R	0x0000000A
PID3	0xE00F_FFEC	32 bits	R	0x00000000
CID0	0xE00F_FFF0	32 bits	R	0x0000000D
CID1	0xE00F_FFF4	32 bits	R	0x00000010
CID2	0xE00F_FFF8	32 bits	R	0x00000005
CID3	0xE00F_FFFC	32 bits	R	0x000000B1

After

(1) Deleted “in the CoreSight ROM Table” in the 2.5.4.1 ROM entries sentence and correct title of Table 2.7 to “ROM entries”

2.5.4.1 ROM entries

Table 2.7 shows the ROM entries. The OCD emulator can use the ROM entries to determine which components are implemented in a system. See reference 4. for details.

Table 2.7 ROM entries

#	Address	Access size	R/W	Value	Target module pointer
0	0x4001_A000	32 bits	R	0x9FFF4003	SCS
1	0x4001_A004	32 bits	R	0x9FFE7003	DWT
2	0x4001_A008	32 bits	R	0x9FFE8003	FPB
3	0x4001_A00C	32 bits	R	0xFFFFF003	MTB
4	0x4001_A010	32 bits	R	0x00000000	End of entries

(2) Correct registers name and address of table 2.8 as below

Table 2.8 CoreSight component registers in the CoreSight ROM Table (1 of 2)

Name	Address	Access size	R/W	Initial value
MEMTYPE	0x4001_AFCC	32 bits	R	0x00000001
PIDR4	0x4001_AFD0	32 bits	R	0x00000004
PIDR5	0x4001_AFD4	32 bits	R	0x00000000
PIDR6	0x4001_AFD8	32 bits	R	0x00000000

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PIDR7	0x4001_AFDC	32 bits	R	0x00000000
PIDR0	0x4001_AFE0	32 bits	R	0x0000002F
PIDR1	0x4001_AFE4	32 bits	R	0x00000030
PIDR2	0x4001_AFE8	32 bits	R	0x0000000A
PIDR3	0x4001_AFEC	32 bits	R	0x00000000
CIDR0	0x4001_AFF0	32 bits	R	0x0000000D
CIDR1	0x4001_AFF4	32 bits	R	0x00000010
CIDR2	0x4001_AFF8	32 bits	R	0x00000005
CIDR3	0x4001_AFFC	32 bits	R	0x000000B1

(3) Registers name of table 2.10

Table 2.10 DBGREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	0x4001_BFD0	32 bits	R	0x00000004
PID5	0x4001_BFD4	32 bits	R	0x00000000
PID6	0x4001_BFD8	32 bits	R	0x00000000
PID7	0x4001_BFDC	32 bits	R	0x00000000
PID0	0x4001_BFE0	32 bits	R	0x00000005
PID1	0x4001_BFE4	32 bits	R	0x00000030
PID2	0x4001_BFE8	32 bits	R	0x0000001A
PID3	0x4001_BFEC	32 bits	R	0x00000000
CID0	0x4001_BFF0	32 bits	R	0x0000000D
CID1	0x4001_BFF4	32 bits	R	0x000000F0
CID2	0x4001_BFF8	32 bits	R	0x00000005
CID3	0x4001_BFFC	32 bits	R	0x000000B1

(4) Registers name of table 2.12

Table 2.12 OCDREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	0x8000_0FD0	32 bits	R	0x00000004
PID5	0x8000_0FD4	32 bits	R	0x00000000
PID6	0x8000_0FD8	32 bits	R	0x00000000
PID7	0x8000_0FDC	32 bits	R	0x00000000
PID0	0x8000_0FE0	32 bits	R	0x00000004
PID1	0x8000_0FE4	32 bits	R	0x00000030
PID2	0x8000_0FE8	32 bits	R	0x0000000A
PID3	0x8000_0FEC	32 bits	R	0x00000000
CID0	0x8000_0FF0	32 bits	R	0x0000000D
CID1	0x8000_0FF4	32 bits	R	0x000000F0
CID2	0x8000_0FF8	32 bits	R	0x00000005
CID3	0x8000_0FFC	32 bits	R	0x000000B1

(3) Correct registers name of table 2.10 as below

Table 2.10 DBGREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PIDR4	0x4001_BFD0	32 bits	R	0x00000004
PIDR5	0x4001_BFD4	32 bits	R	0x00000000
PIDR6	0x4001_BFD8	32 bits	R	0x00000000
PIDR7	0x4001_BFDC	32 bits	R	0x00000000
PIDR0	0x4001_BFE0	32 bits	R	0x00000005
PIDR1	0x4001_BFE4	32 bits	R	0x00000030
PIDR2	0x4001_BFE8	32 bits	R	0x0000001A
PIDR3	0x4001_BFEC	32 bits	R	0x00000000
CIDR0	0x4001_BFF0	32 bits	R	0x0000000D
CIDR1	0x4001_BFF4	32 bits	R	0x000000F0
CIDR2	0x4001_BFF8	32 bits	R	0x00000005
CIDR3	0x4001_BFFC	32 bits	R	0x000000B1

(4) Correct registers name of table 2.12 as below

Table 2.12 OCDREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PIDR4	0x8000_0FD0	32 bits	R	0x00000004
PIDR5	0x8000_0FD4	32 bits	R	0x00000000
PIDR6	0x8000_0FD8	32 bits	R	0x00000000
PIDR7	0x8000_0FDC	32 bits	R	0x00000000
PIDR0	0x8000_0FE0	32 bits	R	0x00000004
PIDR1	0x8000_0FE4	32 bits	R	0x00000030
PIDR2	0x8000_0FE8	32 bits	R	0x0000000A
PIDR3	0x8000_0FEC	32 bits	R	0x00000000
CIDR0	0x8000_0FF0	32 bits	R	0x0000000D
CIDR1	0x8000_0FF4	32 bits	R	0x000000F0
CIDR2	0x8000_0FF8	32 bits	R	0x00000005
CIDR3	0x8000_0FFC	32 bits	R	0x000000B1

Group:RA2E1

2. CPU

Before

(1) 2.5.4.1 ROM entries sentence and title of Table 2.7 “CoreSight ROM Table”

2.5.4.1 ROM entries

Table 2.7 shows the ROM entries in the CoreSight ROM Table. The OCD emulator can use the ROM entries to determine which components are implemented in a system. See reference 4. for details.

Table 2.7 CoreSight ROM Table

#	Address	Access size	R/W	Value	Target module pointer
0	0x4001_A000	32 bits	R	0x9FFF4003	SCS
1	0x4001_A004	32 bits	R	0x9FFE7003	DWT
2	0x4001_A008	32 bits	R	0x9FFE8003	FPB
3	0x4001_A00C	32 bits	R	0xFFFFF003	MTB
4	0x4001_A010	32 bits	R	0x00000000	End of entries

(2) Registers name and Address of table 2.8

Table 2.8 CoreSight component registers in the CoreSight ROM Table (1 of 2)

Name	Address	Access size	R/W	Initial value
DEVTYPE	0xE00F_FFCC	32 bits	R	0x00000001
PID4	0xE00F_FFD0	32 bits	R	0x00000004
PID5	0xE00F_FFD4	32 bits	R	0x00000000
PID6	0xE00F_FFD8	32 bits	R	0x00000000

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PID7	0xE00F_FFDC	32 bits	R	0x00000000
PID0	0xE00F_FFE0	32 bits	R	0x00000039
PID1	0xE00F_FFE4	32 bits	R	0x00000030
PID2	0xE00F_FFE8	32 bits	R	0x0000000A
PID3	0xE00F_FFEC	32 bits	R	0x00000000
CID0	0xE00F_FFF0	32 bits	R	0x0000000D
CID1	0xE00F_FFF4	32 bits	R	0x00000010
CID2	0xE00F_FFF8	32 bits	R	0x00000005
CID3	0xE00F_FFFC	32 bits	R	0x000000B1

After

(1) Deleted “in the CoreSight ROM Table” in the 2.5.4.1 ROM entries sentence and correct title of Table 2.7 to “ROM entries”

2.5.4.1 ROM entries

Table 2.7 shows the ROM entries. The OCD emulator can use the ROM entries to determine which components are implemented in a system. See reference 4. for details.

Table 2.7 ROM entries

#	Address	Access size	R/W	Value	Target module pointer
0	0x4001_A000	32 bits	R	0x9FFF4003	SCS
1	0x4001_A004	32 bits	R	0x9FFE7003	DWT
2	0x4001_A008	32 bits	R	0x9FFE8003	FPB
3	0x4001_A00C	32 bits	R	0xFFFFF003	MTB
4	0x4001_A010	32 bits	R	0x00000000	End of entries

(2) Correct registers name and address of table 2.8 as below

Table 2.8 CoreSight component registers in the CoreSight ROM Table (1 of 2)

Name	Address	Access size	R/W	Initial value
MEMTYPE	0x4001_AFCC	32 bits	R	0x00000001
PIDR4	0x4001_AFD0	32 bits	R	0x00000004
PIDR5	0x4001_AFD4	32 bits	R	0x00000000
PIDR6	0x4001_AFD8	32 bits	R	0x00000000

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PIDR7	0x4001_AFDC	32 bits	R	0x00000000
PIDR0	0x4001_AFE0	32 bits	R	0x00000039
PIDR1	0x4001_AFE4	32 bits	R	0x00000030
PIDR2	0x4001_AFE8	32 bits	R	0x0000000A
PIDR3	0x4001_AFEC	32 bits	R	0x00000000
CIDR0	0x4001_AFF0	32 bits	R	0x0000000D
CIDR1	0x4001_AFF4	32 bits	R	0x00000010
CIDR2	0x4001_AFF8	32 bits	R	0x00000005
CIDR3	0x4001_AFFC	32 bits	R	0x000000B1

(3) Registers name of table 2.10

Table 2.10 DBGREG CoreSight component registers (1 of 2)

Name	Address	Access size	R/W	Initial value
PID4	0x4001_BFD0	32 bits	R	0x00000004
PID5	0x4001_BFD4	32 bits	R	0x00000000

Table 2.10 DBGREG CoreSight component registers (2 of 2)

Name	Address	Access size	R/W	Initial value
PID6	0x4001_BFD8	32 bits	R	0x00000000
PID7	0x4001_BFDC	32 bits	R	0x00000000
PID0	0x4001_BFE0	32 bits	R	0x00000005
PID1	0x4001_BFE4	32 bits	R	0x00000030
PID2	0x4001_BFE8	32 bits	R	0x0000001A
PID3	0x4001_BFEC	32 bits	R	0x00000000
CID0	0x4001_BFF0	32 bits	R	0x0000000D
CID1	0x4001_BFF4	32 bits	R	0x000000F0
CID2	0x4001_BFF8	32 bits	R	0x00000005
CID3	0x4001_BFFC	32 bits	R	0x000000B1

(4) Registers name of table 2.12

Table 2.12 OCDREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	0x8000_0FD0	32 bits	R	0x00000004
PID5	0x8000_0FD4	32 bits	R	0x00000000
PID6	0x8000_0FD8	32 bits	R	0x00000000
PID7	0x8000_0FDC	32 bits	R	0x00000000
PID0	0x8000_0FE0	32 bits	R	0x00000004
PID1	0x8000_0FE4	32 bits	R	0x00000030
PID2	0x8000_0FE8	32 bits	R	0x0000000A
PID3	0x8000_0FEC	32 bits	R	0x00000000
CID0	0x8000_0FF0	32 bits	R	0x0000000D
CID1	0x8000_0FF4	32 bits	R	0x000000F0
CID2	0x8000_0FF8	32 bits	R	0x00000005
CID3	0x8000_0FFC	32 bits	R	0x000000B1

(3) Correct registers name of table 2.10 as below

Table 2.10 DBGREG CoreSight component registers (1 of 2)

Name	Address	Access size	R/W	Initial value
PIDR4	0x4001_BFD0	32 bits	R	0x00000004
PIDR5	0x4001_BFD4	32 bits	R	0x00000000

Table 2.10 DBGREG CoreSight component registers (2 of 2)

Name	Address	Access size	R/W	Initial value
PIDR6	0x4001_BFD8	32 bits	R	0x00000000
PIDR7	0x4001_BFDC	32 bits	R	0x00000000
PIDR0	0x4001_BFE0	32 bits	R	0x00000005
PIDR1	0x4001_BFE4	32 bits	R	0x00000030
PIDR2	0x4001_BFE8	32 bits	R	0x0000001A
PIDR3	0x4001_BFEC	32 bits	R	0x00000000
CIDR0	0x4001_BFF0	32 bits	R	0x0000000D
CIDR1	0x4001_BFF4	32 bits	R	0x000000F0
CIDR2	0x4001_BFF8	32 bits	R	0x00000005
CIDR3	0x4001_BFFC	32 bits	R	0x000000B1

(4) Correct registers name of table 2.12 as below

Table 2.12 OCDREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PIDR4	0x8000_0FD0	32 bits	R	0x00000004
PIDR5	0x8000_0FD4	32 bits	R	0x00000000
PIDR6	0x8000_0FD8	32 bits	R	0x00000000
PIDR7	0x8000_0FDC	32 bits	R	0x00000000
PIDR0	0x8000_0FE0	32 bits	R	0x00000004
PIDR1	0x8000_0FE4	32 bits	R	0x00000030
PIDR2	0x8000_0FE8	32 bits	R	0x0000000A
PIDR3	0x8000_0FEC	32 bits	R	0x00000000
CIDR0	0x8000_0FF0	32 bits	R	0x0000000D
CIDR1	0x8000_0FF4	32 bits	R	0x000000F0
CIDR2	0x8000_0FF8	32 bits	R	0x00000005
CIDR3	0x8000_0FFC	32 bits	R	0x000000B1

Group:RA2E2

2. CPU

Before

(1) 2.5.4.1 ROM entries sentence and title of Table 2.7 “CoreSight ROM Table”

2.5.4.1 ROM entries

Table 2.7 shows the ROM entries in the CoreSight ROM Table. The OCD emulator can use the ROM entries to determine which components are implemented in a system. See reference 4. for details.

Table 2.7 CoreSight ROM Table

#	Address	Access size	R/W	Value	Target module pointer
0	0x4001_A000	32 bits	R	0x9FFF4003	SCS
1	0x4001_A004	32 bits	R	0x9FFE7003	DWT
2	0x4001_A008	32 bits	R	0x9FFE8003	FPB
3	0x4001_A00C	32 bits	R	0xFFFFF003	MTB
4	0x4001_A010	32 bits	R	0x00000000	End of entries

(2) Registers name and Address of table 2.8

Table 2.8 CoreSight component registers in the CoreSight ROM Table (1 of 2)

Name	Address	Access size	R/W	Initial value
DEVTYPE	0xE00F_FFCC	32 bits	R	0x00000001
PID4	0xE00F_FFD0	32 bits	R	0x00000004
PID5	0xE00F_FFD4	32 bits	R	0x00000000
PID6	0xE00F_FFD8	32 bits	R	0x00000000

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PID7	0xE00F_FFDC	32 bits	R	0x00000000
PID0	0xE00F_FFE0	32 bits	R	0x0000003D
PID1	0xE00F_FFE4	32 bits	R	0x00000030
PID2	0xE00F_FFE8	32 bits	R	0x0000000A
PID3	0xE00F_FFEC	32 bits	R	0x00000000
CID0	0xE00F_FFF0	32 bits	R	0x0000000D
CID1	0xE00F_FFF4	32 bits	R	0x00000010
CID2	0xE00F_FFF8	32 bits	R	0x00000005
CID3	0xE00F_FFFC	32 bits	R	0x000000B1

After

(1) Deleted “in the CoreSight ROM Table” in the 2.5.4.1 ROM entries sentence and correct title of Table 2.7 to “ROM entries”

2.5.4.1 ROM entries

Table 2.7 shows the ROM entries. The OCD emulator can use the ROM entries to determine which components are implemented in a system. See reference 4. for details.

Table 2.7 ROM entries

#	Address	Access size	R/W	Value	Target module pointer
0	0x4001_A000	32 bits	R	0x9FFF4003	SCS
1	0x4001_A004	32 bits	R	0x9FFE7003	DWT
2	0x4001_A008	32 bits	R	0x9FFE8003	FPB
3	0x4001_A00C	32 bits	R	0xFFFFF003	MTB
4	0x4001_A010	32 bits	R	0x00000000	End of entries

(2) Correct registers name and address of table 2.8 as below

Table 2.8 CoreSight component registers in the CoreSight ROM Table (1 of 2)

Name	Address	Access size	R/W	Initial value
MEMTYPE	0x4001_AFCC	32 bits	R	0x00000001
PIDR4	0x4001_AFD0	32 bits	R	0x00000004
PIDR5	0x4001_AFD4	32 bits	R	0x00000000
PIDR6	0x4001_AFD8	32 bits	R	0x00000000

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PIDR7	0x4001_AFDC	32 bits	R	0x00000000
PIDR0	0x4001_AFE0	32 bits	R	0x0000003D
PIDR1	0x4001_AFE4	32 bits	R	0x00000030
PIDR2	0x4001_AFE8	32 bits	R	0x0000000A
PIDR3	0x4001_AFEC	32 bits	R	0x00000000
CIDR0	0x4001_AFF0	32 bits	R	0x0000000D
CIDR1	0x4001_AFF4	32 bits	R	0x00000010
CIDR2	0x4001_AFF8	32 bits	R	0x00000005
CIDR3	0x4001_AFFC	32 bits	R	0x000000B1

(3) Registers name of table 2.10

Table 2.10 DBGREG CoreSight component registers (1 of 2)

Name	Address	Access size	R/W	Initial value
PID4	0x4001_BFD0	32 bits	R	0x00000004
PID5	0x4001_BFD4	32 bits	R	0x00000000

Table 2.10 DBGREG CoreSight component registers (2 of 2)

Name	Address	Access size	R/W	Initial value
PID6	0x4001_BFD8	32 bits	R	0x00000000
PID7	0x4001_BFDC	32 bits	R	0x00000000
PID0	0x4001_BFE0	32 bits	R	0x00000005
PID1	0x4001_BFE4	32 bits	R	0x00000030
PID2	0x4001_BFE8	32 bits	R	0x0000001A
PID3	0x4001_BFEC	32 bits	R	0x00000000
CID0	0x4001_BFF0	32 bits	R	0x0000000D
CID1	0x4001_BFF4	32 bits	R	0x000000F0
CID2	0x4001_BFF8	32 bits	R	0x00000005
CID3	0x4001_BFFC	32 bits	R	0x000000B1

(4) Registers name of table 2.12

Table 2.12 OCDREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	0x8000_0FD0	32 bits	R	0x00000004
PID5	0x8000_0FD4	32 bits	R	0x00000000
PID6	0x8000_0FD8	32 bits	R	0x00000000
PID7	0x8000_0FDC	32 bits	R	0x00000000
PID0	0x8000_0FE0	32 bits	R	0x00000004
PID1	0x8000_0FE4	32 bits	R	0x00000030
PID2	0x8000_0FE8	32 bits	R	0x0000000A
PID3	0x8000_0FEC	32 bits	R	0x00000000
CID0	0x8000_0FF0	32 bits	R	0x0000000D
CID1	0x8000_0FF4	32 bits	R	0x000000F0
CID2	0x8000_0FF8	32 bits	R	0x00000005
CID3	0x8000_0FFC	32 bits	R	0x000000B1

(3) Correct registers name of table 2.10 as below

Table 2.10 DBGREG CoreSight component registers (1 of 2)

Name	Address	Access size	R/W	Initial value
PIDR4	0x4001_BFD0	32 bits	R	0x00000004
PIDR5	0x4001_BFD4	32 bits	R	0x00000000

Table 2.10 DBGREG CoreSight component registers (2 of 2)

Name	Address	Access size	R/W	Initial value
PIDR6	0x4001_BFD8	32 bits	R	0x00000000
PIDR7	0x4001_BFDC	32 bits	R	0x00000000
PIDR0	0x4001_BFE0	32 bits	R	0x00000005
PIDR1	0x4001_BFE4	32 bits	R	0x00000030
PIDR2	0x4001_BFE8	32 bits	R	0x0000001A
PIDR3	0x4001_BFEC	32 bits	R	0x00000000
CIDR0	0x4001_BFF0	32 bits	R	0x0000000D
CIDR1	0x4001_BFF4	32 bits	R	0x000000F0
CIDR2	0x4001_BFF8	32 bits	R	0x00000005
CIDR3	0x4001_BFFC	32 bits	R	0x000000B1

(4) Correct registers name of table 2.12 as below

Table 2.12 OCDREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PIDR4	0x8000_0FD0	32 bits	R	0x00000004
PIDR5	0x8000_0FD4	32 bits	R	0x00000000
PIDR6	0x8000_0FD8	32 bits	R	0x00000000
PIDR7	0x8000_0FDC	32 bits	R	0x00000000
PIDR0	0x8000_0FE0	32 bits	R	0x00000004
PIDR1	0x8000_0FE4	32 bits	R	0x00000030
PIDR2	0x8000_0FE8	32 bits	R	0x0000000A
PIDR3	0x8000_0FEC	32 bits	R	0x00000000
CIDR0	0x8000_0FF0	32 bits	R	0x0000000D
CIDR1	0x8000_0FF4	32 bits	R	0x000000F0
CIDR2	0x8000_0FF8	32 bits	R	0x00000005
CIDR3	0x8000_0FFC	32 bits	R	0x000000B1