Date: Aug. 10, 2022

# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | Document No. | TN-RA*-A0060A/E | Rev. | 1.00 |
|---|---|---|---|---|---|
| Title | Correction for “Arm MPU” descriptions in RA2 series User’s Manual | | Information Category | Technical Notification | |
| Applicable Product | RA2A1 Group<br>RA2L1 Group<br>RA2E1 Group<br>RA2E2 Group | Lot No.<br>All lots | Reference Document | Refer to Table1 as below | |

Table 1

| Product Group | Reference Document | Version |
|---|---|---|
| RA2L1 | Renesas RA2L1 Group User’s Manual: Hardware<br>R01UH0853EJ0120 (May 20, 2022) | Rev.1.20 |
| RA2E1 | Renesas RA2E1 Group User’s Manual: Hardware<br>R01UH0852EJ0120 (Feb 4,2022) | Rev.1.20 |
| RA2E2 | Renesas RA2E2 Group User’s Manual: Hardware<br>R01UH0919EJ0110 (Mar 31, 2022) | Rev.1.10 |
| RA2A1 | Renesas RA2A1 Group User’s Manual: Hardware<br>R01UH0888EJ0100 (Oct 8, 2019) | Rev.1.00 |

Corrections in the User’s Manual: Hardware

| Group & Page | Applicable Item | Revised content |
|---|---|---|
| RA2L1 / p.229 | 14. Memory Protection Unit (MPU)<br>14.3 Arm MPU | Deleted Description about Overlap of Arm MPU |
| RA2E1 / p.223 | | |
| RA2E2 / p.189 | | |
| RA2A1 / p.228 | 15. Memory Protection Unit (MPU)<br>15.3 Arm MPU | |

## Group: RA2L1/RA2E1/RA2E2

**Incorrect）**

14.3 Arm MPU

The Arm MPU monitors the addresses accessed by the CPU across the entire address space (0x0000_0000 to 0xFFFF_FFFF) and provides support for:

- 8 protected regions
- **Overlapping protected regions, with ascending region priority:**
  **7 = highest priority**
  **0 = lowest priority.**
- Setting access permissions to protected region (Read, Write, Execution)
- Export of memory attributes to the system.

Arm MPU mismatches and permission violations invoke the programmable-priority MemManage fault (Hard Fault)
handler. For details, see section 14.8. References.

**Correct）**

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**(Deleted Description about Overlap)**

- Setting access permissions to protected region (Read, Write, Execution)
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Arm MPU mismatches and permission violations invoke the programmable-priority MemManage fault (Hard Fault)
handler. For details, see section 14.8. References.

## Group: RA2A1

**Incorrect）**

15.3 Arm MPU

The Arm MPU provides full support for:
- 8 protection regions
- **Overlapping protection regions, with ascending region priority:**
  **7 = highest priority**
  **0 = lowest priority**

. • Access permissions
- Exporting memory attributes to the system.

Arm MPU mismatches and permission violations invoke the programmable-priority MemManage fault (HardFault) handler. For details, see 2. in section 15.7, References.

**Correct）**

15.3 Arm MPU

The Arm MPU provides full support for:
- 8 protection regions

**(Deleted description about Overlap)**

. • Access permissions
- Exporting memory attributes to the system.

Arm MPU mismatches and permission violations invoke the programmable-priority MemManage fault (HardFault) handler. For details, see 2. in section 15.7, References.