Date: Aug. 29, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0090A/E	Rev.	1.00
Title	The correction and the additional specification of CANFD		Information Category	Technical Notification		
Applicable Product	RA6T2 Group	Lot No. All	Reference Document	RA6T2 Group User's Manual : Hardware Rev.1.30		

This document describes the corrections and additional specification of Message buffer RAM in CANFD.

Before correction

28.2.57 CFDGLOCKK : Global Lock Key Register
(omission)
LOCK[15:0] bits (Lock Key)
The unlock key sequence must be written in the LOCK[15:0] bits to configure the CANFD module in FIFO OTB disable and RAM test modes.

After correction

28.2.57 CFDGLOCKK : Global Lock Key Register
(omission)
LOCK[15:0] bits (Lock Key)
The unlock key sequence must be written in the LOCK[15:0] bits to configure the CANFD module in RAM test modes.

Before correction

28.6.2.1 FIFO Buffers Configuration
(omission)
(3) FIFO depth configuration
(omission)
The RAM allocation for RX message buffers along with FIFO buffers is limited to 16 messages with 64 data bytes.
(omission)
(4) FIFO payload size configuration
(omission)
The RAM allocation for RX message buffers along with FIFO buffers is limited to 16 messages with 64 data bytes.

After correction

28.6.2.1 FIFO Buffers Configuration
(omission)
(3) FIFO depth configuration
(omission)
The RAM allocation for RX message buffers along with FIFO buffers is limited to 16 messages with 64 data bytes (76 bytes including ID, etc.).
(omission)
(4) FIFO payload size configuration
(omission)
The RAM allocation for RX message buffers along with FIFO buffers is limited to 16 messages with 64 data bytes (76 bytes including ID, etc.).

Before correction

28.9.2.1 RAM Test Mode
(omission)

The pn and CFDGTSTCFG.RTMPS[3:0] values for the MB RAMs are calculated in the following way:
pn = ceil (total RAM size in bytes / number of bytes per page)

- MB RAM:
  pn = ceil (2328 / 256) = 10 pages
  CFDGTSTCFG.RTMPS[3:0] = 0 to 9 inclusive

After correction

28.9.2.1 RAM Test Mode
(omission)

The pn and CFDGTSTCFG.RTMPS[3:0] values for the MB RAMs are calculated in the following way:
pn = ceil (total RAM size in bytes / number of bytes per page)

- MB RAM:
  pn = ceil (2328 / 256) = 10 pages
  CFDGTSTCFG.RTMPS[3:0] = 0 to 9 inclusive

(User should not access more than 24 Bytes in the last page)

Before correction

(Chapter 28.10 is not listed.)

After correction

28.10 RAM area configuration

The RAM area used in CANFD (referred to as MRAM) can be split into the following groups as shown below in Figure 28.55:

AFL Rule Table area
PFL Rule Table area
Message Buffer*1 area (RX MB + FIFO Buffer)
OTB area
THL area
TX MB area

Physically the RAM is the Message Buffer RAM*2 (RX MB, RX FIFO, Common FIFO*3, TX MB, THL, OTB, AFL Rule Table, PFL Rule Table).

*1: Referred to as MB
*2: Referred to as MRAM
*3: Referred to as CFIFO

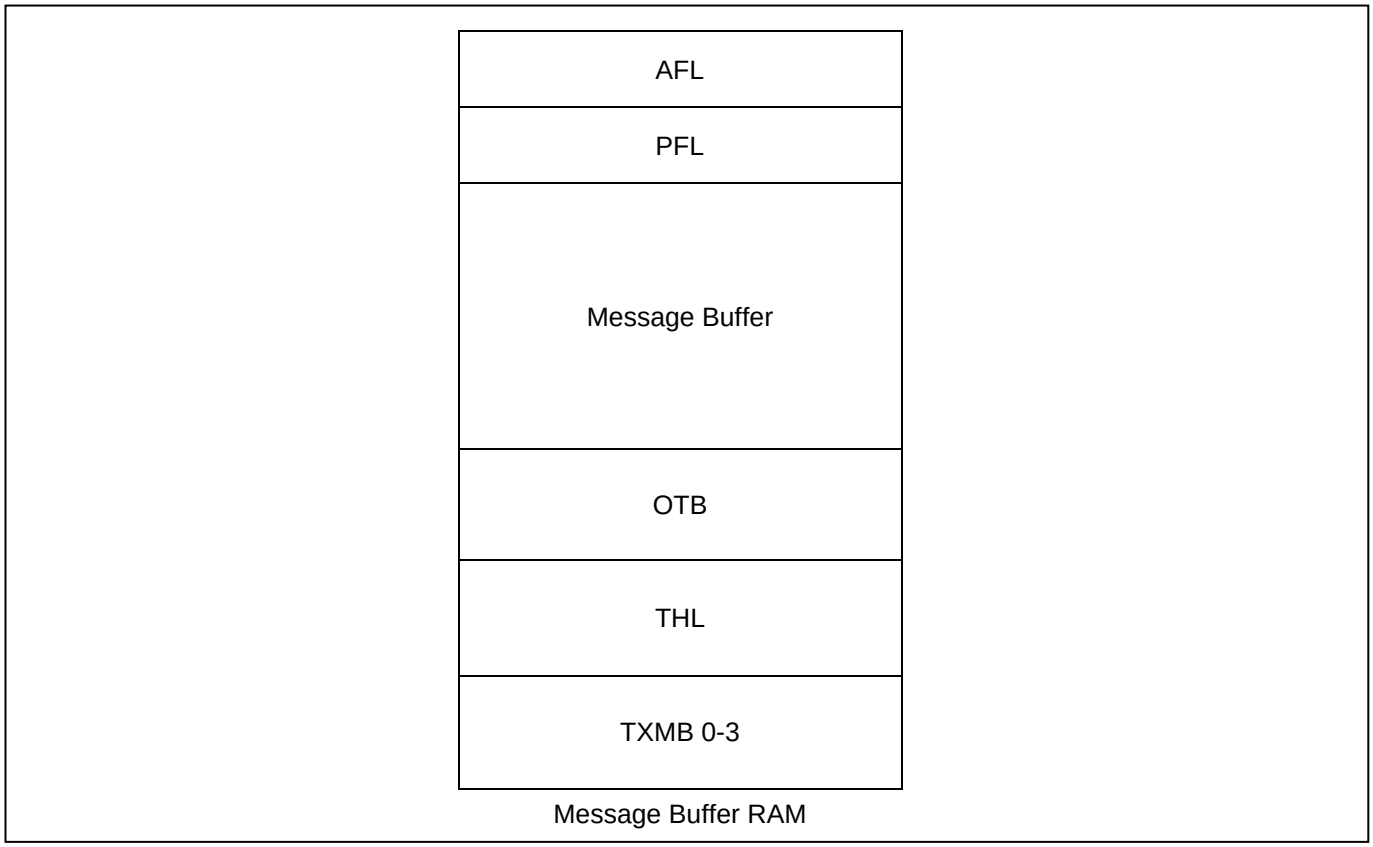

Figure 28.55: RAM area grouping

The MRAM area starts with the TX MB area at address 0x0000. The TX MB area is followed immediately by the THL area which is then followed immediately by the OTB area. The size of the TX MB, THL and OTB area is fixed. The OTB area is followed by the message buffer area. The message buffer area size depends on the configuration of the flat RXMBs, RXFIFOs and CFIFO. When all are configured the RX MB area is followed by the RXFIFO area which is followed by the CFIFO area.

The configured MRAM area can be calculated then as follows.

MRAM_cfg = RXMB_MRAM_cfg + RXFIFO_MRAM_cfg + CFIFO_MRAM_cfg +
TXMB_MRAM_cfg +THL_MRAM_cfg + OTB_MRAM_cfg +
AFL_MRAM_cfg + PFL_MRAM_cfg

RXMB_MRAM_cfg = (12 Bytes + CFDRMNB.RMPLS) * CFDRMNB.NRXMB
RXFIFO_MRAM_cfg = SUM((12 Bytes + CFDRFCCa.RFPLS) * CFDRFCCa.RFDC)
CFIFO_MRAM_cfg = (12 Bytes + CFDCFCC.CFPLS) * CFDCFCC.CFDC
TXMB_MRAM_cfg = 304 Bytes
THL_MRAM_cfg = 64 Bytes
OTB_MRAM_cfg = 160 Bytes
PFL_MRAM_cfg = 72 Bytes
AFL_MRAM_cfg = 512 Bytes

“a” means RX FIFO index = [0…no_of_RFIFOs-1]
no_of_RFIFOs : Number of configured RX FIFOs

Note: For CFDRFCCa.RFDC, CFDCFCC.CFDC, CFDRMNB.RMPLS, CFDRMNB.NRXMB, CFDRFCCa.RFPLS and CFDCFCC.CFPLS the related number of bytes must be used.

The Table 28.30 shows the calculation of the different RAM areas used for the AFL entries, OTB buffers, TX/RX message buffers, RX/Common FIFOs and PFL entries.

Table 28.30 MRAM area calculation

RAM Name	RAM Property	RAM Area Calculation Method	RAM Values
AFL	Avg. rule entries		32
	No. of Bytes in a rule entry	Fixed	16
	No. of Bytes in AFL area	Avg. rule entries * No. of Bytes in a rule entry	512
PFL	Avg. rule entries		2
	No. of Bytes in a rule entry	Fixed	36
	No. of Bytes in PFL area	Avg. rule entries * No. of Bytes in a rule entry	72
TX MB	No. of TX MBs	Fixed	4
	No. of Bytes needed for each TX MB	Fixed	76
	No. of Bytes in TX MB area	No. of TXMBs * No. of Bytes needed for each TXMB	304
THL	No. of entries in 1 THL buffer	Fixed	8
	No. of Bytes needed for each THL entry	Fixed	8
	No. of Bytes in THL area	No. of entries in 1 THL buffer * No. of Bytes needed for each THL entry	64
OTB	Avg. No. of buffers		2
	No. of Bytes for OTB entry	Fixed	80
	No.of Bytes in OTB area	Avg. No. of buffers * No. of Bytes for OTB entry	160
Message Buffer	No. of RXMBs	Fixed	32
	No. of RXFIFOs	Fixed	2
	No. of Common FIFO	Fixed	1
	Avg. No. of messages for RXMB and FIFO buffers		16
	No. of Bytes for each stored message	Fixed	-
	Average size of a Message Buffer in Bytes		76
	No. of Bytes in Message Pool area	Avg. No. of messages for RXMB and FIFO buffers * Average size of a Message Buffer in Bytes	1216
	No. of Bytes Message RAM	No. of Bytes in Message Pool area + No. of Bytes in OTB area + No. of Bytes in THL area + No. of Bytes in TXMB area + No. of Bytes in PFL area + No. of Bytes in AFL area	2328

28.10.1 Examples

The Figure 28.56 below shows one possible configuration.

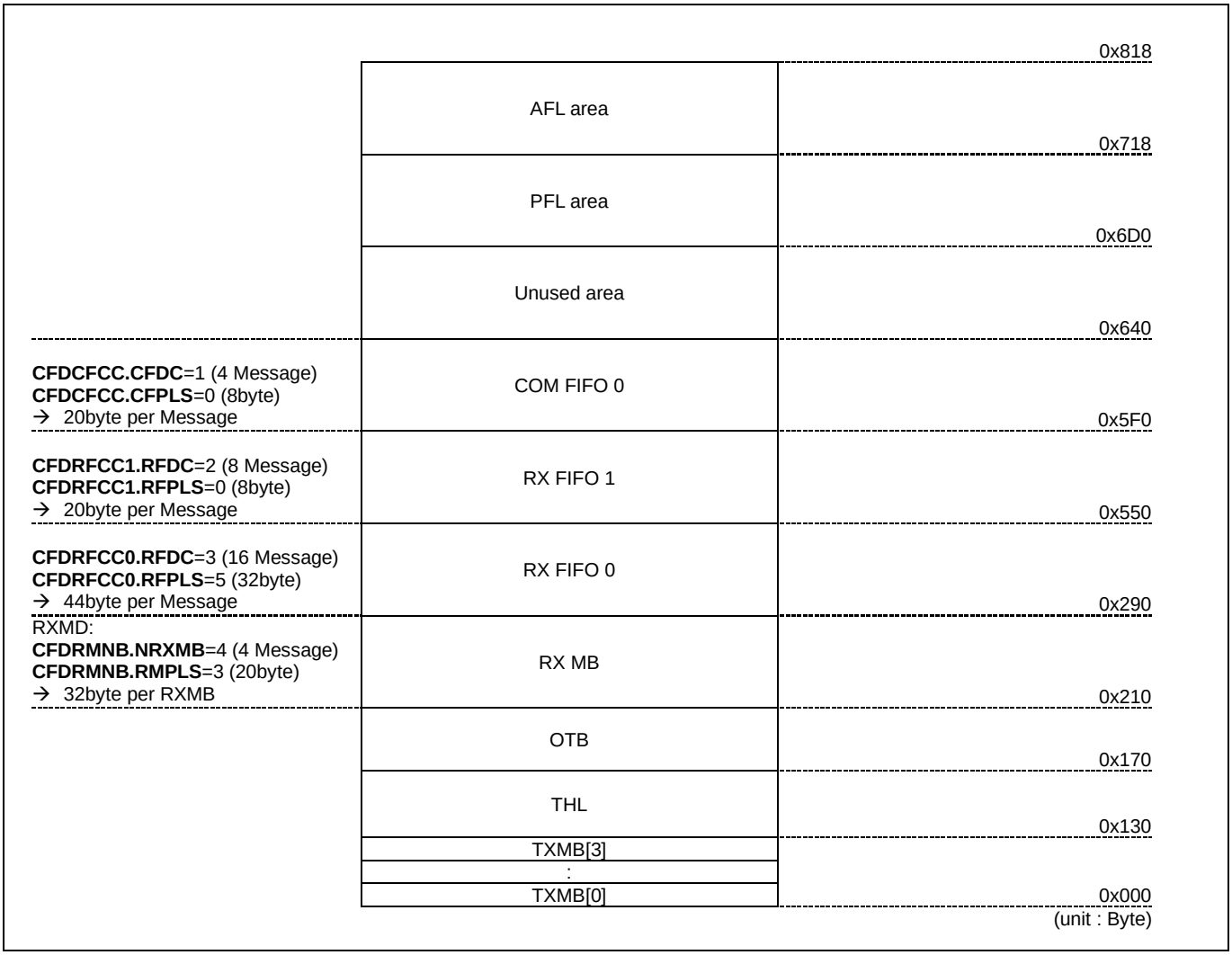

Figure 28.56: RX MB + FIFO buffers RAM area configuration examples

28.10.2 OTB Area

The OTB area starts immediately after the area allocated for THL Buffers. The OTB is a special purpose buffer used by the CANFD. This section of RAM area can be accessed only by the CPU in RAM Test mode. Buffer needs 80 Bytes and the average number of buffers is 2. Hence, the total number of Bytes allocated for the OTB is 2*80 Bytes.

28.10.3 RAM initialization cycle

The number of RAM initialization cycles and the RAM number of pages are shown below.

MRAM area size	RAM initialisation cycles	RAM Test RTMPS range (*1)
2328	584	0x0 .. 0x9

(pclk cycle)