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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0091A/E	Rev.	1.00
Title	The correction and the additional specification of CANFD		Information Category	Technical Notification		
Applicable Product	RA6M5 Group	Lot No. All	Reference Document	RA6M5 Group User's Manual : Hardware Rev.1.30		

This document describes the corrections and additional specification of Message buffer RAM in CANFD.

Before correction

32.2.83 CFDGLOCKK : Global Lock Key Register
(omission)

LOCK[15:0] bits (Lock Key)
The unlock key sequence must be written in the LOCK[15:0] bits to configure the CANFD module in FIFO OTB disable and RAM test modes.

After correction

32.2.83 CFDGLOCKK : Global Lock Key Register
(omission)

LOCK[15:0] bits (Lock Key)
The unlock key sequence must be written in the LOCK[15:0] bits to configure the CANFD module RAM test modes.

Before correction

32.8.1.2 Message Storage in FIFO Buffers

(omission)

Do not modify this bit when the CFDCFCCn.CFE bit is 1.

Common FIFO can set the interrupt when CAN frame reception is completed.

Common FIFO can set the interrupt when FIFO is in full status in RX mode or GW mode.

Note: The message lost can be set only in RX or GW mode by CAN, and the flag is not set when the CPU is overloading the FIFO buffers.

Note: When CFDGAFLP0n.GAFLSRD i (i = 0 to 2) is set and the CFDTXQCCin.TXQGWE (i = 0 to 2, n = 0 to 7) is also set, a receiving frame is stored in the target TXQ as send data by routing.

The RX FIFO buffers and the Common FIFO buffers configured in RX or GW mode can be disabled at any time by clearing the CFDRFCCn.RFE or CFDCFCCn.CFE bit in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers.

After correction

32.8.1.2 Message Storage in FIFO Buffers

(omission)

Do not modify this bit when the CFDCFCCn.CFE bit is 1.

Common FIFO can set the interrupt when CAN frame reception is completed.

Common FIFO can set the interrupt when FIFO is in full status in RX mode or GW mode.

Note: The message lost can be set only in RX or GW mode by CAN, and the flag is not set when the CPU is overloading the FIFO buffers.

Note: When CFDGAFLP0n.GAFLSRD i (i = 0 to 2) is set and the CFDTXQCCin.TXQGWE (i = 0 to 2, n = 0 to 1) is also set, a receiving frame is stored in the target TXQ as send data by routing.

The RX FIFO buffers and the Common FIFO buffers configured in RX or GW mode can be disabled at any time by clearing the CFDRFCCn.RFE or CFDCFCCn.CFE bit in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers.

Before correction

32.8.2.4 TX Queue

(omission)

When using TXQ1 and TXQ0 simultaneously, the depth of TXQ is 8 or less in total.

When using TXQ3 and TXQ2 simultaneously, the depth of TXQ is 8 or less in total.

Do not access all the TX message buffers forming the TX Queue directly (except TX Message Buffer No. 39, TX Message Buffer No. 32, TX Message Buffer No. 7 and TX Message Buffer No. 0, which act as TX Queue access window).

When CFDGAFLP0n.GAFLSRD i (i = 0 to 2) is set and the CFDTXQCCin.TXQGWE (i = 0 to 3, n = 0 to 1) is also set, a receiving frame is stored in the target TXQ as send data by routing.

After correction

32.8.2.4 TX Queue

(omission)

When using TXQ1 and TXQ0 simultaneously, the depth of TXQ is 8 or less in total.

When using TXQ3 and TXQ2 simultaneously, the depth of TXQ is 8 or less in total.

Do not access all the TX message buffers forming the TX Queue directly (except TX Message Buffer No. 39, TX Message Buffer No. 32, TX Message Buffer No. 7 and TX Message Buffer No. 0, which act as TX Queue access window).

When CFDGAFLP0n.GAFLSRD i (i = 0 to 2) is set and the CFDTXQCCin.TXQGWE (i = 0 to 2, n = 0 to 1) is also set, a receiving frame is stored in the target TXQ as send data by routing.

Before correction

32.9.2.1 RAM Test Mode

(omission)

The pn and CFDGTSTCFG.RTMPS[9:0] values for the AFL and MB RAMs are calculated in the following way:
pn = ceil (total RAM size in bytes / number of bytes per page)

- AFL RAM:
  pn = ceil (2048 / 256) = 8 pages
  CFDGTSTCFG.RTMPS[9:0] = 0 to 7 (0x00F) inclusive
- MB RAM:
  pn = ceil (8192 / 256) = 32 pages
  CFDGTSTCFG.RTMPS[9:0] = 8 to 39 (0x27) inclusive

After correction

32.9.2.1 RAM Test Mode

(omission)

The pn and CFDGTSTCFG.RTMPS[9:0] values for the AFL and MB RAMs are calculated in the following way:
pn = ceil (total RAM size in bytes / number of bytes per page)

- AFL RAM:
  pn = ceil (2048 / 256) = 8 pages
  CFDGTSTCFG.RTMPS[9:0] = 0 to 7 (0x00F) inclusive
- MB RAM:
  pn = ceil (8192 / 256) = 32 pages
  CFDGTSTCFG.RTMPS[9:0] = 8 to 39 (0x27) inclusive

（User should not access more than 64 Bytes in the last page）

Before correction

(There is no description in chapter 32)

After correction

32.x RAM area configuration

The RAM area used in CANFD can be split into the following groups as shown below in Figure 32.x1:

AFL Rule Table area
PFL Rule Table area
Message Buffer[*1] area (RX MB + FIFO Buffer)
OTB area
THL area
TX MB area

*1: Referred to as MB

Physically the RAM is split in three RAMs, PFL Rule Table RAM[*2], AFL Rule Table RAM0[*3] (CFDGAFLID and CFDGAFLP0)+AFL Rule Table RAM1[*3] (CFDGAFLM and CFDGAFLP1), and Message Buffer RAM[*4] (RX MB, RX FIFO, Common FIFO[*5], TX MB, THL and OTB)

*2: Referred to as PFL RAM
*3: RAM0 and RAM1 together are referred to as AFL RAM
*4: Referred to as MRAM
*5: Referred to as CFIFO

The size of PFL RAM, AFL RAM, and MRAM changes with the number of channels[*6].

*6: Referred to as n (n=0 means the number of channels =1, n=1 means the number of channels=2)

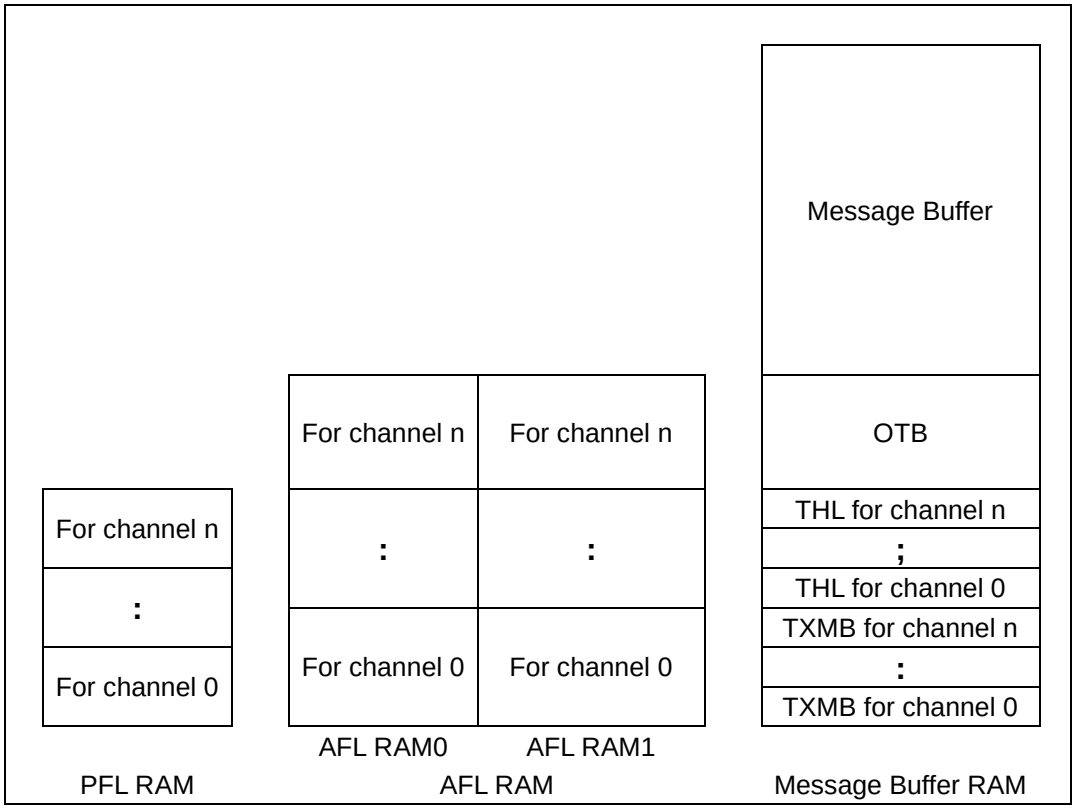

Figure 32.x1: RAM area grouping

The Rule Table area always starts at AFL RAM address 0x0000 and has a fixed size for a given number of channels.
The MRAM area starts with the TX MB area at address 0x0000. The TX MB area is followed immediately by the THL area which is then followed immediately by the OTB area. The size of the TX MB, THL and OTB area is fixed for a given number of channels.
The OTB area is followed by the message buffer area. The massage buffer area size depends on the configuration of the flat RXMBs, RXFIFOs and CFIFOs. When all are configured, the RXMB area is followed by the RXFIFO area which is followed by the CFIFO area.

The configured MRAM area can be calculated then as follows.

MRAM_cfg = RXMB_MRAM_cfg + RXFIFO_MRAM_cfg + CFIFO_MRAM_cfg +
TXMB_MRAM_cfg +THL_MRAM_cfg + OTB_MRAM_cfg

RXMB_MRAM_cfg = (12 Bytes + CFDRMNB.RMPLS) * CFDRMNB.NRXMB
RXFIFO_MRAM_cfg = SUM((12 Bytes + CFDRFCCa.RFPLS) * CFDRFCCa.RFDC)
CFIFO_MRAM_cfg = SUM((12 Bytes + CFDCFCCd.CFPLS) * CFDCFCCd.CFDC)
TXMB_MRAM_cfg = 4864 Bytes * (n+1)
THL_MRAM_cfg = 256 Bytes * (n+1)
OTB_MRAM_cfg = 160 Bytes * (n+1)

“a” means RX FIFO index = [0…no_of_RFIFOs-1]
“d” means Common FIFO index = [0 .. no_of_CFIFOs -1]
no_of_RFIFOs : Number of configured RX FIFOs
no_of_CFIFOs: Number of configured CFIFOs

Note: For CFDRFCCa.RFDC, CFDCFCCd.CFDC, CFDRMNB.RMPLS, CFDRMNB.NRXMB, CFDRFCCa.RFPLS and CFDCFCCd.CFPLS the related number of bytes must be used.

The PFL Rule Table area always starts at PFL RAM address 0x0000 and has a fixed size for a given number of channels.

Table 32.x1 shows the calculation of the different RAM areas used for the AFL entries, OTB buffers, TX/RX message buffers, RX/Common FIFOs and PFL entries. Table 32.x2 shows the cycles for RAM initialization.

Table 32.x1 PFL RAM area, AFL RAM area, and MRAM area calculation

RAM Name	RAM Property	RAM Area Calculation Method	PFL RAM Values
	No. of Channels	(n+1)	2
PFL	Avg. rule entries per channel	Fixed	20
	Max Rule entries	(n+1) * Avg. tule entries per channel	40
	No. of Bytes in a rule entry	Fixed	36
	Number of Bytes PFL RAM	Max Rule entries * No. of Bytes in a rule entry	1440

RAM Name	RAM Property	RAM Area Calculation Method	AFL RAM Values
	No. of Channels	(n+1)	2
AFL	Avg. rule entries per channel	64/ch	64
	Max Rule entries	(n+1) * Avg. tule entries per channel	128
	No. of Bytes in a rule entry	Fixed	16
	Number of Bytes AFL RAM	Max Rule entries * No. of Bytes in a rule entry	2048

RAM Name	RAM Property	RAM Area Calculation Method	MRAM Values
	No. of Channels	(n+1)	2
TXMB	No. of TX MBs per channel	16/ch	16
	Max no. of TX MBs	(n+1) * No. of TX MBs per channel	32
	No. of Bytes needed for each TX MB	Fixed	76
	Number of Bytes in TX MB area	(n+1) * No. of TX MBs per channel * No. of Bytes needed for each TX MB	2432
THL	No. of entries in 1 THL buffer	Fixed	32
	Max no of THL entries	(n+1) * No. of entries in 1 THL buffer	64
	No. of Bytes needed for each THL entry	Fixed	8
	Number of Bytes in THL area	Max no. of THL entries * No. of Bytes needed for each THL entry	512
OTB	Avg. number of buffers for each channel		2
	Max no. of OTB entries	(n+1) * Avg. number of buffers for each channel	4
	No. of Bytes for OTB entry	Fixed	80
	Number of Bytes in OTB area	Max no. of OTB entries * No. of Bytes for OTB entry	320
Message Buffer	No. of RX MBs per channel	Fixed	16
	Max no. of RX MBs	(n+1) * No. of RXMBs per channel	32
	No. of RX FIFOs	Fixed	8
	No. of Common FIFOs per channel	Fixed	3
	Max no. of common FIFOs	(n+1) * No. of Common FIFOs per channel	6
	Avg. number of messages for RXMB and FIFO buffers for each channel	32/ch	32
	No. of Bytes for each stored message	Fixed	-
	Average size of a Message Buffer in Bytes		76
	Number of Bytes in Message Pool area	(n+1) * Avg. number of messages for RXMB and FIFO buffers for each channel * (No. of Bytes for each stored message or Average size of a Message Buffer in Bytes)	4864
	Number of Bytes Message RAM	Number of Bytes in Message Pool area + Number of Bytes in OTB area + Number of Bytes in THL area	8128

Table 32.x2 RAM initialization cycle

RAM initialization cycles (pclk cycle)	2034

32.x.1 Examples

The Figure 32.x2 below shows one possible configuration of a **2 channel version.**

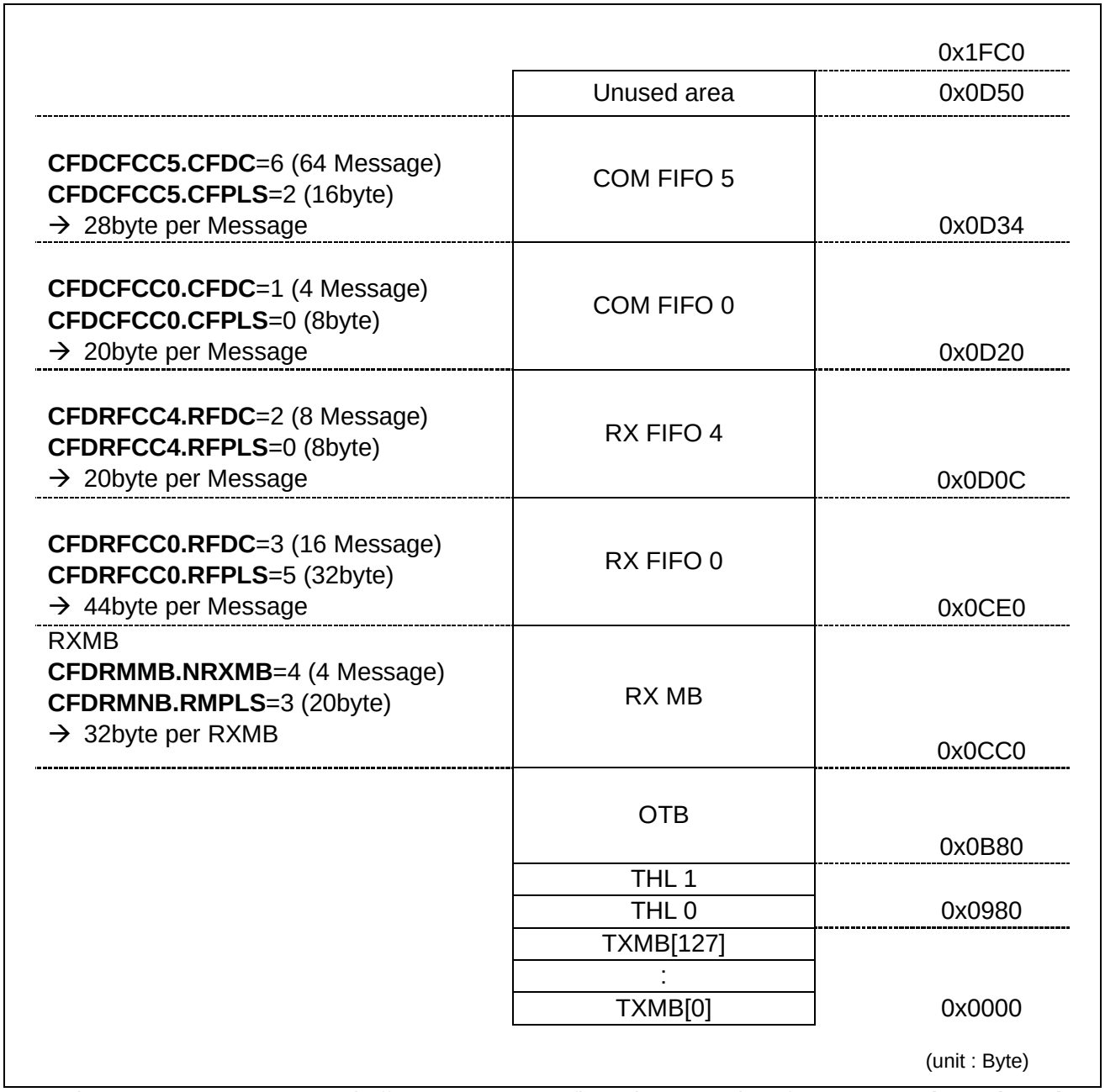

Figure 32.x2: RX MB + FIFO buffers RAM area configuration examples of a CANFD **2 channel version**

32.x.2 OTB Area

The OTB area starts immediately after the area allocated for THL Buffers. The OTB is a special purpose buffer used by the CANFD. This section of RAM area can be accessed only by the CPU in RAM Test mode. The average number of buffers for each channel is 2. Each Buffer needs 80 Bytes. Hence, the total number of Bytes allocated for the OTB is ((n+1)*2)*80 Bytes.