We would like to inform you of the following correction of the ambiguous explanation in the hardware manual about transmit and receive operation flows of Serial Sound Interface included in the above-mentioned applicable product.
(1) Transmission Using Direct Memory Access Controller (to "Enable transmit operation")

[Target Figure]

SH7201 Group: Figure 18.20 Transmission Using DMA Controller
SH7203 Group: Figure 18.20 Transmission Using DMA Controller
SH7205 Group: Figure 19.20 Transmission Using DMA Controller
SH7261 Group: Figure 18.20 Transmission Using DMA Controller
SH7263 Group: Figure 18.20 Transmission Using DMA Controller
SH7265 Group: Figure 19.20 Transmission Using DMA Controller
SH7262 Group, SH7264 Group: Figure 18.20 Transmission Using Direct Memory Access Controller
SH7266 Group, SH7267 Group: Figure 19.20 Transmission Using Direct Memory Access Controller
SH7268 Group, SH7269 Group: Figure 21.23 Transmission Using Direct Memory Access Controller

[After correction]

Start
Release from reset,
set SSICR configuration bits.

Setup direct memory access controller,
Enable direct memory access controller.

Enable an error interrupt,
enable transmit interrupt (DMA request)*1,
enable transmit operation.

Define \((TRMD)^{1,2}\), \((EN)^{1,2}\), \((SCKD)^{1,2}\), \((SWD)^{1,2}\), \((MUEN)^{1,2}\), \((DEL)^{1,2}\), \((PDTA)^{1,2}\), \((SDA)^{1,2}\), \((SPDP)^{1,2}\), \((SWSP)^{1,2}\), \((SCKP)^{1,2}\), \((SWL)^{1,2}\), \((DWL)^{1,2}\), \((CHNL)^{1,2}\).

Note: *1 In case of SH7201 Group, SH7203 Group, SH7205 Group,
SH7261 Group, SH7263 Group and SH7265 Group.
*2 In case of SH7201 Group, SH7203 Group,
SH7261 Group and SH7263 Group.
(2) Transmission Using Interrupt-Driven Data Flow Control (to “Enable transmit operation”)

**[Target Figure]**

- SH7201 Group: Figure 18.21 Transmission Using Interrupt Data Flow Control
- SH7203 Group: Figure 18.21 Transmission Using Interrupt Data Flow Control
- SH7205 Group: Figure 19.21 Transmission Using Interrupt-Driven Data Flow Control
- SH7261 Group: Figure 18.21 Transmission Using Interrupt Data Flow Control
- SH7263 Group: Figure 18.21 Transmission Using Interrupt Data Flow Control
- SH7265 Group: Figure 19.21 Transmission Using Interrupt-Driven Data Flow Control
- SH7262 Group, SH7264 Group: Figure 18.21 Transmission Using Interrupt-Driven Data Flow Control
- SH7266 Group, SH7267 Group: Figure 19.21 Transmission Using Interrupt-Driven Data Flow Control
- SH7268 Group, SH7269 Group: Figure 21.24 Transmission Using Interrupt-Driven Data Flow Control

**[After correction]**

1. Enable an error interrupt, \( T_E^1 = 1 \) and \( T_U^1 = 1 \)
2. Start
3. Release from reset, set SSICR configuration bits.
4. Setup Interrupt controller.
5. Enable an error interrupt, enable transmit interrupt (DATA interrupt)\(^{1}\), enable transmit operation, \( T_E^1 = 1 \), \( T_U^1 = 1 \), \( T_I = 1 \) (DIEN = 1)\(^{2}\), TIE = 1

**Note:**

*1 In case of SH7201 Group, SH7203 Group, SH7205 Group, SH7261 Group, SH7263 Group and SH7265 Group.

*2 In case of SH7201 Group, SH7203 Group, SH7261 Group and SH7263 Group.
(3) Reception Using Direct Memory Access Controller (to "Enable receive operation")

[Target Figure]
SH7201 Group: Figure 18.22 Reception Using DMA Controller
SH7203 Group: Figure 18.22 Reception Using DMA Controller
SH7205 Group: Figure 19.22 Reception Using DMA Controller
SH7261 Group: Figure 18.22 Reception Using DMA Controller
SH7263 Group: Figure 18.22 Reception Using DMA Controller
SH7265 Group: Figure 19.22 Reception Using DMA Controller
SH7262 Group, SH7264 Group: Figure 18.22 Reception Using Direct Memory Access Controller
SH7266 Group, SH7267 Group: Figure 19.22 Reception Using Direct Memory Access Controller
SH7268 Group, SH7269 Group: Figure 21.25 Reception Using Direct Memory Access Controller

[After correction]

Start

Release from reset,
set SSICR configuration bits.

Setup direct memory access controller,
Enable direct memory access controller.

Enable an error interrupt,
enable receive interrupt (DMA request)*1,
enable receive operation.

Define (TRMD)*1 (EN)*1, SCKD,
SWSD, MU/EN, DEL, PDTA,
SDTA, SPD, SWSP, SCKP,
SWL, DWL, CHNL.*1

Note: *1 In case of SH7201 Group, SH7203 Group, SH7205 Group,
SH7261 Group, SH7263 Group and SH7265 Group.

*2 In case of SH7201 Group, SH7203 Group,
SH7261 Group and SH7263 Group.
(4) Reception Using Interrupt-Driven Data Flow Control (to "Enable receive operation")

[Target Figure]
SH7201 Group: Figure 18.23 Reception Using Interrupt Data Flow Control
SH7203 Group: Figure 18.23 Reception Using Interrupt Data Flow Control
SH7205 Group: Figure 19.23 Reception Using Interrupt-Driven Data Flow Control
SH7261 Group: Figure 18.23 Reception Using Interrupt Data Flow Control
SH7263 Group: Figure 18.23 Reception Using Interrupt Data Flow Control
SH7265 Group: Figure 19.23 Reception Using Interrupt-Driven Data Flow Control
SH7262 Group, SH7264 Group: Figure 18.23 Reception Using Interrupt-Driven Data Flow Control
SH7266 Group, SH7267 Group: Figure 19.23 Reception Using Interrupt-Driven Data Flow Control
SH7268 Group, SH7269 Group: Figure 21.26 Reception Using Interrupt-Driven Data Flow Control

[After correction]

```
Ren(EN)*1 = 1, RUIEN/UIEN*1 = 1, ROIEN/OIEN*1 = 1, RIE = 1 (DIEN = 1)*2
```

Start

- Release from reset, set SSICR configuration bits.
- Setup interrupt controller.
- Enable an error interrupt, enable receive interrupt (DATA interrupt)/1, enable receive operation.

Define (TRMD)*1, (EN)*1, SCKD, SWSD, MUEN, DEL, PDTA, SDTA, SPD, SWSP, SCKP, SWL, DWL, CHNL.

Note: *1 In case of SH7201 Group, SH7203 Group, SH7205 Group, SH7261 Group, SH7263 Group and SH7265 Group.
*2 In case of SH7201 Group, SH7203 Group, SH7261 Group and SH7263 Group.
### Applicable Products and Reference Documents

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