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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0097A/E	Rev.	1.00
Title	Correction on AC and temperature sensor characteristics		Information Category	Technical Notification		
Applicable Product	RZ/T2M Group	Lot No. All	Reference Document	RZ/T2M Group Datasheet Rev.1.00 (R01DS0383EJ0100) RZ/T2M Group User's Manual: Hardware Rev.1.00 (R01UH0916EJ0100)		

There were errors in the contents of electrical characteristics on RZ/T2M Datasheet and User's Manual Hardware Rev.1.00, which should be corrected as follows:

1. AC Characteristics: Bus Timing

Several values of the bus timing were corrected as follows (Highlighted as red color):

[Before the changes]

Table 45(or 2).21 Bus Timing (1 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (CKIO), 30 pF (others), Tjmin = -40°C

Parameter		Symbol	CKIO = 1/t_{CKcyc} (注 1) (Max 66MHz) Min	Max	Unit
Address delay time 1	SDRAM*2	t_{AD1}	2	10.5	ns
	Other than the above		0	10	ns
Address delay time 2		t_{AD2}	1/2t_{CKcyc}	1/2t_{CKcyc} + 10	ns
Address setup time		t_{AS}	0	—	ns
Chip enable setup time		t_{CS}	0	—	ns
Address hold time		t_{AH}	0	—	ns
BS delay time		t_{BSD}	—	10.5	ns
CSn# delay time 1	SDRAM*2	t_{CSD1}	2	10.5	ns
	Other than the above		0	10	ns
Read/write delay time 1	SDRAM*2	t_{RWD1}	2	10.5	ns
	Other than the above		0	10	ns
Read strobe delay time		t_{RSD}	1/2t_{CKcyc}	1/2t_{CKcyc} + 10	ns
Read data setup time 1*3	High-drive output	t_{RDS1}	1/2t_{CKcyc} + 4	—	ns
	Normal output		1/2t_{CKcyc} + 7	—	ns
Read data setup time 2*3	High-drive output	t_{RDS2}	6.6	—	ns
Read data setup time 3*3	High-drive output	t_{RDS3}	1/2t_{CKcyc} + 4	—	ns
	Normal output		1/2t_{CKcyc} + 7	—	ns
Read data hold time 1		t_{RDH1}	0	—	ns
Read data hold time 2		t_{RDH2}	2	—	ns
Read data hold time 3		t_{RDH3}	0	—	ns
Write enable delay time 1		t_{WED1}	1/2t_{CKcyc}	1/2t_{CKcyc} + 10	ns
Write enable delay time 2		t_{WED2}	—	10	ns
Write data delay time 1		t_{WDD1}	—	10	ns

[After the changes]

Table 45(or 2).21 Bus Timing (1 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (CKIO), 30 pF (others), Tjmin = -40°C

Parameter		Symbol	CKIO = $1/t_{CKcyc}$ (注 1) (Max 66MHz) Min	Max	Unit
Address delay time 1	SDRAM*2	t_{AD1}	2	11	ns
	Other than the above		0	10	ns
Address delay time 2		t_{AD2}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns
Address setup time		t_{AS}	0	—	ns
Chip enable setup time		t_{CS}	0	—	ns
Address hold time		t_{AH}	0	—	ns
BS delay time		t_{BSD}	—	11	ns
CSn# delay time 1	SDRAM*2	t_{CSD1}	2	11	ns
	Other than the above		0	10	ns
Read/write delay time 1	SDRAM*2	t_{RWD1}	2	11	ns
	Other than the above		0	10	ns
Read strobe delay time		t_{RSD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns
Read data setup time 1*3	High-drive output	t_{RDS1}	$1/2t_{CKcyc}$ + 4	—	ns
	Normal output		$1/2t_{CKcyc}$ + 7	—	ns
Read data setup time 2*3	High-drive output	t_{RDS2}	6.6	—	ns
Read data setup time 3*3	High-drive output	t_{RDS3}	$1/2t_{CKcyc}$ + 4	—	ns
	Normal output		$1/2t_{CKcyc}$ + 7	—	ns
Read data hold time 1		t_{RDH1}	0	—	ns
Read data hold time 2		t_{RDH2}	2.5	—	ns
Read data hold time 3		t_{RDH3}	0	—	ns
Write enable delay time 1		t_{WED1}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns
Write enable delay time 2		t_{WED2}	—	11	ns
Write data delay time 1		t_{WDD1}	—	11	ns

[Before the changes]

Table 45(or 2).21 Bus Timing (2 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (CKIO), 30 pF (others), Tjmin = -40°C

Parameter		Symbol	CKIO = $1/t_{CKcyc}$ (注 1) (Max 66MHz) Min	Max	Unit
Write data delay time 2		t_{WDD2}	—	10.5	ns
Write data hold time 1		t_{WDH1}	1	—	ns
Write data hold time 2		t_{WDH2}	2	—	ns
Write data hold time 4		t_{WDH4}	0	—	ns
WAIT# setup time*3	High-drive output	t_{WTS}	$1/2t_{CKcyc}$ + 4.5	—	ns
	Normal output		$1/2t_{CKcyc}$ + 8	—	ns
WAIT# hold time		t_{WTH}	$1/2t_{CKcyc}$ + 3.5	—	ns
RAS# delay time 1		t_{RASD1}	2	10.5	ns
CAS# delay time 1		t_{CASD1}	2	10.5	ns
DQM delay time 1		t_{DQMD1}	2	10.5	ns
CKE delay time 1		t_{CKED1}	2	10.5	ns
AH# delay time		t_{AHD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns
Multiplex address delay time		t_{MAD}	—	10	ns
Multiplex address hold time		t_{MAH}	1	—	ns
Address setup time to AH#		t_{AVVH}	$1/2t_{CKcyc}$ - 2	—	ns
DACK/TEND delay time		t_{DACD}	See section 45.5.4. DMAC Timing		ns

[After the changes]

Table 45(or 2).21 Bus Timing (2 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (CKIO), 30 pF (others), Tjmin = -40°C

Parameter		Symbol	CKIO = $1/t_{CKcyc}$ (注 1) (Max 66MHz) Min	Max	Unit
Write data delay time 2		t_{WDD2}	—	11	ns
Write data hold time 1		t_{WDH1}	1	—	ns
Write data hold time 2		t_{WDH2}	2	—	ns
Write data hold time 4		t_{WDH4}	0	—	ns
WAIT# setup time*3	High-drive output	t_{WTS}	$1/2t_{CKcyc}$ + 4.5	—	ns
	Normal output		$1/2t_{CKcyc}$ + 8	—	ns
WAIT# hold time		t_{WTH}	$1/2t_{CKcyc}$ + 3.5	—	ns
RAS# delay time 1		t_{RASD1}	2	11	ns
CAS# delay time 1		t_{CASD1}	2	11	ns
DQM delay time 1		t_{DQMD1}	2	11	ns
CKE delay time 1		t_{CKED1}	2	11	ns
AH# delay time		t_{AHD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns
Multiplex address delay time		t_{MAD}	—	10	ns
Multiplex address hold time		t_{MAH}	1	—	ns
Address setup time to AH#		t_{AVVH}	$1/2t_{CKcyc}$ - 2	—	ns
DACK/TEND delay time		t_{DACD}	See section 45.5.4. DMAC Timing		ns

[Before the changes]

Table 45(or 2).22 Bus Timing (2 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 12 pF (CKIO), 12 pF (others), Tjmin = -20°C

Parameter		Symbol	CKIO = 1/t_{CKcyc} (注 1) (Max 100MHz) Min	Max	Unit
Read/write delay time 1	SDRAM*2	t_{RWD1}	1.3	8	
	Other than the above		0	8	
Read strobe delay time		t_{RSD}	1/2t_{CKcyc}	1/2t_{CKcyc} + 8	
Read data setup time 1*3	High-drive output	t_{RDS1}	1/2t_{CKcyc} + 4.5	—	ns
	Normal output		1/2t_{CKcyc} + 7	—	ns
Read data setup time 2*3	High-drive output	t_{RDS2}	6.6	—	ns
Read data setup time 3*3	High-drive output	t_{RDS3}	1/2t_{CKcyc} + 4.5	—	ns
	Normal output		1/2t_{CKcyc} + 7	—	ns
Read data hold time 1		t_{RDH1}	0	—	ns
Read data hold time 2		t_{RDH2}	2.5	—	ns
Read data hold time 3		t_{RDH3}	0	—	ns
Write enable delay time 1		t_{WED1}	1/2t_{CKcyc}	1/2t_{CKcyc} + 8	ns
Write enable delay time 2		t_{WED2}	—	9	ns
Write data delay time 1		t_{WDD1}	—	8	ns
Write data delay time 2		t_{WDD2}	—	10.5	ns
Write data hold time 1		t_{WDH1}	1	—	ns
Write data hold time 2		t_{WDH2}	2	—	ns
Write data hold time 4		t_{WDH4}	0	—	ns
WAIT# setup time*3	High-drive output	t_{WTS}	1/2t_{CKcyc} + 4.5	—	ns
	Normal output		1/2t_{CKcyc} + 8	—	ns
WAIT# hold time		t_{WTH}	1/2t_{CKcyc} + 3.5	—	ns
RAS# delay time 1		t_{RASD1}	2	10.5	ns
CAS# delay time 1		t_{CASD1}	2	10.5	ns
DQM delay time 1		t_{DQMD1}	2	10.5	ns
CKE delay time 1		t_{CKED1}	2	10.5	ns
AH# delay time		t_{AHD}	1/2t_{CKcyc}	1/2t_{CKcyc} + 10	ns
Multiplex address delay time		t_{MAD}	—	10	ns
Multiplex address hold time		t_{MAH}	1	—	ns
Address setup time to AH#		t_{AVVH}	1/2t_{CKcyc} - 2	—	ns
DACK/TEND delay time		t_{DACD}	See section 45.5.4. DMAC Timing		ns

[After the changes]

Table 45(or 2).22 Bus Timing (2 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 12 pF (CKIO), 12 pF (others), Tjmin = -20°C

Parameter		Symbol	CKIO = 1/t_{CKcyc} (注 1) (Max 100MHz) Min	Max	Unit
Read/write delay time 1	SDRAM*2	t_{RWD1}	1.3	8	
	Other than the above		0	8	
Read strobe delay time		t_{RSD}	1/2t_{CKcyc}	1/2t_{CKcyc} + 8	
Read data setup time 1*3	High-drive output	t_{RDS1}	1/2t_{CKcyc} + 4.5	—	ns
	Normal output		1/2t_{CKcyc} + 7	—	ns
Read data setup time 2*3	High-drive output	t_{RDS2}	3.5	—	ns
Read data setup time 3*3	High-drive output	t_{RDS3}	1/2t_{CKcyc} + 4.5	—	ns
	Normal output		1/2t_{CKcyc} + 7	—	ns
Read data hold time 1		t_{RDH1}	0	—	ns
Read data hold time 2		t_{RDH2}	2.5	—	ns
Read data hold time 3		t_{RDH3}	0	—	ns
Write enable delay time 1		t_{WED1}	1/2t_{CKcyc}	1/2t_{CKcyc} + 8	ns
Write enable delay time 2		t_{WED2}	—	9	ns
Write data delay time 1		t_{WDD1}	—	8	ns
Write data delay time 2		t_{WDD2}	—	10.5	ns
Write data hold time 1		t_{WDH1}	1	—	ns
Write data hold time 2		t_{WDH2}	2	—	ns
Write data hold time 4		t_{WDH4}	0	—	ns
WAIT# setup time*3	High-drive output	t_{WTS}	1/2t_{CKcyc} + 4.5	—	ns
	Normal output		1/2t_{CKcyc} + 8	—	ns
WAIT# hold time		t_{WTH}	1/2t_{CKcyc} + 3.5	—	ns
RAS# delay time 1		t_{RASD1}	2	10.5	ns
CAS# delay time 1		t_{CASD1}	2	10.5	ns
DQM delay time 1		t_{DQMD1}	2	10.5	ns
CKE delay time 1		t_{CKED1}	2	10.5	ns
AH# delay time		t_{AHD}	1/2t_{CKcyc}	1/2t_{CKcyc} + 10	ns
Multiplex address delay time		t_{MAD}	—	10	ns
Multiplex address hold time		t_{MAH}	1	—	ns
Address setup time to AH#		t_{AVVH}	1/2t_{CKcyc} - 2	—	ns
DACK/TEND delay time		t_{DACD}	See section 45.5.4. DMAC Timing		ns

2. Temperature Sensor Characteristics

Value of the temperature slope was corrected as follows (Highlighted as red color):

[Before the changes]

Table 45(or 2).46 Temperature sensor characteristics

Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	*1
Temperature slope	—	0.625	—	°C/LSB	—
Output code (at 25°C)	—	1545 (decimal)	—	—	TSUSAD register

Note 1. 2-point calibration (Tj = 25℃ and Tj = 85℃) and 8 times averaging. For details of 2-point calibration, …

[After the changes]

Table 45(or 2).46 Temperature sensor characteristics

Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	*1
Temperature slope	—	0.0625	—	°C/LSB	—
Output code (at 25°C)	—	1545 (decimal)	—	—	TSUSAD register

Note 1. 2-point calibration (Tj = 25℃ and Tj = 85℃) and 8 times averaging. For details of 2-point calibration, …