Date: Feb. 5, 2024

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0105A/E	Rev.	1.00
Title	Correction for 12-Bit A/D Converter(ADC12) and Timing of recovery from low power modes in RA2 group User's Manual		Information Category	Technical Notification		
Applicable Product	RA Family RA2L1/RA2E1/RA2E2/RA2E3 Group	Lot No. All lots	Reference Document	-Renesas RA2L1 Group User's Manual: Hardware R01UH0853EJ0140 Rev.1.40 -Renesas RA2E1 Group User's Manual: Hardware R01UH0852EJ0140 Rev.1.40 -Renesas RA2E2 Group User's Manual: Hardware R01UH0919EJ0130 Rev.1.30 -Renesas RA2E3 Group User's Manual: Hardware R01UH0992EJ0110 Rev.1.10		

Correction of errata regarding relationship between DBLANS bit settings and Double trigger enable channels in the 12-Bit A/D Converter(ADC12).

And correction of errata in the Timing of recovery from low power modes(2) and (3) in the Wakeup Time section of the Electrical Characteristics.

The details are shown from the next page.

Group:RA2L1

30. 12-Bit A/D Converter(ADC12)

Correct errata of DBLANS[4:0] values in Table 30.18 Relationship between DBLANS bit Settings and Double-trigger Enabled Channels(2 of 2).

Before

Table 30.18 Relationship between DBLANS bit Settings and Double-trigger Enabled Channels (2 of 2)

DBLANS[4:0]	Duplication channel
0x09	AN009
0x0A	AN010
0x0B	AN011
0x0C	AN012
0x0D	AN013
0x0E	AN014
0x11	AN017
0x13	AN018
0x14	AN019
0x15	AN020

After

Table 30.18 Relationship between DBLANS bit Settings and Double-trigger Enabled Channels (2 of 2)

DBLANS[4:0]	Duplication channel
0x09	AN009
0x0A	AN010
0x0B	AN011
0x0C	AN012
0x0D	AN013
0x0E	AN014
0x11	AN017
0x12	AN018
0x13	AN019
0x14	AN020

41. Electrical Characteristics

(1) Correct errata on Table41.23 Timing of recovery from low power modes (2).

The details are shown below.

- Border position of symbol t_{SBYMO}.
- Oscillator frequency when Vcc = 1.6V to 1.8V in "External clock input to main clock oscillator" and recovery time for Typ and Max.
- Remove *4 from "System clock source is HOCO" and add *4 to the voltage range description.

Before

Table 41.23 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	
			System clock source is main clock oscillator (20 MHz)*3 VCC = 1.6 V to 1.8 V		—	11.7	13		
		System clock source is HOCO*4	VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	5.2	6.5	µs	Figure 41.10
			VCC = 1.6 V to 1.8 V	t_{SBYMO}	—	13.2	15		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V		—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 24 MHz.

After

Table 41.23 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	
			System clock source is main clock oscillator (4 MHz)*3 VCC = 1.6 V to 1.8 V		—	8.5	9.1		
		System clock source is HOCO	VCC = 1.8 V to 5.5 V*4	t_{SBYHO}	—	5.2	6.5	µs	Figure 41.10
			VCC = 1.6 V to 1.8 V		—	13.2	15		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 24 MHz.

(2) Correct errata on Table 41.24, Timing of recovery from low power modes (3), frequency of "System clock source is MOCO".

Before

Table 41.24 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (2 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 41.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (2 MHz)*3	t_{SBYEX}	—	14.5	16	µs	
		System clock source is MOCO (2 MHz)		t_{SBYMO}	—	12	15	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.

After

Table 41.24 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (2 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 41.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (2 MHz)*3	t_{SBYEX}	—	14.5	16	µs	
		System clock source is MOCO (8 MHz)		t_{SBYMO}	—	12	15	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.

Group:RA2E1

29. 12-Bit A/D Converter(ADC12)

Correct errata of DBLANS[4:0] values in Table 29.18 Relationship between DBLANS bit Settings and Double-trigger Enabled Channels(2 of 2).

Before

Table 29.18 Relationship between DBLANS bit Settings and Double-trigger Enabled Channels (2 of 2)

DBLANS[4:0]	Duplication channel
0x09	AN009
0x0A	AN010
0x11	AN017
0x13	AN018
0x14	AN019
0x15	AN020
0x16	AN021
0x17	AN022

After

Table 29.18 Relationship between DBLANS bit Settings and Double-trigger Enabled Channels (2 of 2)

DBLANS[4:0]	Duplication channel
0x09	AN009
0x0A	AN010
0x11	AN017
0x12	AN018
0x13	AN019
0x14	AN020
0x15	AN021
0x16	AN022

39. Electrical Characteristics

(1) Correct errata on Table 39.23 Timing of recovery from low power modes (2).

The details are shown below.

- Border position of symbol t_{SBYMO}.
- Oscillator frequency when Vcc = 1.6V to 1.8V in "External clock input to main clock oscillator" and recovery time for Typ and Max.
- Remove *4 from "System clock source is HOCO" and add *4 to the voltage range description.

Before

Table 39.23 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	
			System clock source is main clock oscillator (20 MHz)*3 VCC = 1.6 V to 1.8 V		—	11.7	13		
		System clock source is HOCO*4	VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	7.7	9.4	µs	Figure 39.10
			VCC = 1.6 V to 1.8 V	t_{SBYMO}	—	15.7	17.9		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V		—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 24 MHz.

After

Table 39.23 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	
			System clock source is main clock oscillator (4 MHz)*3 VCC = 1.6 V to 1.8 V		—	8.5	9.1		
		System clock source is HOCO	VCC = 1.8 V to 5.5 V*4	t_{SBYHO}	—	7.7	9.4	µs	Figure 39.10
			VCC = 1.6 V to 1.8 V		—	15.7	17.9		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 24 MHz.

(2) Correct errata on Table 39.24, Timing of recovery from low power modes (3), frequency of "System clock source is MOCO".

Before

Table 39.24 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (2 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 39.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (2 MHz)*3	t_{SBYEX}	—	14.5	16	µs	
		System clock source is MOCO (2 MHz)		t_{SBYMO}	—	12	15	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.

After

Table 39.24 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (2 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 39.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (2 MHz)*3	t_{SBYEX}	—	14.5	16	µs	
		System clock source is MOCO (8 MHz)		t_{SBYMO}	—	12	15	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.

Group:RA2E2

28. 12-Bit A/D Converter(ADC12)

Correct errata of DBLANS[4:0] values in Table 28.16 Relationship between DBLANS bit Settings and Double-trigger Enabled Channels.

Before

Table 28.16 Relationship between DBLANS bit Settings and Double-trigger Enabled Channels

DBLANS[4:0]	Duplication channel
0x05	AN005
0x06	AN006
0x09	AN009
0x0A	AN010
0x14	AN019
0x15	AN020
0x16	AN021
0x17	AN022

After

Table 28.16 Relationship between DBLANS bit Settings and Double-trigger Enabled Channels

DBLANS[4:0]	Duplication channel
0x05	AN005
0x06	AN006
0x09	AN009
0x0A	AN010
0x13	AN019
0x14	AN020
0x15	AN021
0x16	AN022

36. Electrical Characteristics

(1) Correct errata on Table 36.23 Timing of recovery from low power modes (2).

The details are shown below.

- Border position of symbol t_{SBYMO}.
- Remove *2 from "System clock source is HOCO" and add *2 to the voltage range description.

Before

Table 36.23 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	System clock source is HOCO*2	VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	7.7	9.4	µs	Figure 36.8
			VCC = 1.6 V to 1.8 V		—	15.7	17.9		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The system clock is 24 MHz.

After

Table 36.23 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	System clock source is HOCO	VCC = 1.8 V to 5.5 V*2	t_{SBYHO}	—	7.7	9.4	µs	Figure 36.8
			VCC = 1.6 V to 1.8 V		—	15.7	17.9		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The system clock is 24 MHz.

(2) Correct errata on Table 36.24, Timing of recovery from low power modes (3), frequency of "System clock source is MOCO".

Before

Table 36.24 Timing of recovery from low power modes (3)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	System clock source is MOCO (2 MHz)	t_{SBYMO}	—	12	15	µs	Figure 36.8

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

After

Table 36.24 Timing of recovery from low power modes (3)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	System clock source is MOCO (8 MHz)	t_{SBYMO}	—	12	15	µs	Figure 36.8

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Group:RA2E3

29. 12-Bit A/D Converter(ADC12)

Correct errata of DBLANS[4:0] values in Table 29.16 Relationship between DBLANS bit settings and double-trigger enabled channels.

Before

Table 29.16 Relationship between DBLANS bit settings and double-trigger enabled channels

DBLANS[4:0]	Duplication channel
0x00	AN000
0x01	AN001
0x02	AN002
0x05	AN005
0x06	AN006
0x07	AN007
0x08	AN008
0x09	AN009
0x0A	AN010
0x14	AN019
0x15	AN020
0x16	AN021
0x17	AN022

After

Table 29.16 Relationship between DBLANS bit settings and double-trigger enabled channels

DBLANS[4:0]	Duplication channel
0x00	AN000
0x01	AN001
0x02	AN002
0x05	AN005
0x06	AN006
0x07	AN007
0x08	AN008
0x09	AN009
0x0A	AN010
0x13	AN019
0x14	AN020
0x15	AN021
0x16	AN022

35. Electrical Characteristics

(1) Correct errata on Table 35.22 Timing of recovery from low power modes (2).

The details are shown below.

- Border position of symbol t_{SBYMO}.
- Oscillator frequency when Vcc = 1.6V to 1.8V in "External clock input to main clock oscillator" and recovery time for Typ and Max.
- Remove *4 from "System clock source is HOCO" and add *4 to the voltage range description.

Before

Table 35.22 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	
			System clock source is main clock oscillator (20 MHz)*3 VCC = 1.6 V to 1.8 V		—	11.7	13		
		System clock source is HOCO*4	VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	7.7	9.4	µs	Figure 35.10
			VCC = 1.6 V to 1.8 V		—	15.7	17.9		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 24 MHz.

After

Table 35.22 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	
			System clock source is main clock oscillator (4 MHz)*3 VCC = 1.6 V to 1.8 V		—	8.5	9.1		
		System clock source is HOCO	VCC = 1.8 V to 5.5 V*4	t_{SBYHO}	—	7.7	9.4	µs	Figure 35.10
			VCC = 1.6 V to 1.8 V		—	15.7	17.9		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 24 MHz.

(2) Correct errata on Table 35.23, Timing of recovery from low power modes (3), frequency of "System clock source is MOCO".

Before

Table 35.23 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (2 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 35.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (2 MHz)*3	t_{SBYEX}	—	14.5	16	µs	
		System clock source is MOCO (2 MHz)		t_{SBYMO}	—	12	15	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.

After

Table 35.23 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (2 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 35.10
		External clock input to main clock oscillator	System clock source is main clock oscillator (2 MHz)*3	t_{SBYEX}	—	14.5	16	µs	
		System clock source is MOCO (8 MHz)		t_{SBYMO}	—	12	15	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.