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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A008A/E	Rev.	1.00
Title	Correcting wrong description of Delta Sigma Interface(DSMIF) specification in RZ/T1 Group User's Manual Hardware.		Information Category	Technical Notification		
Applicable Product	RZ/T1 Group	Lot No. All lots	Reference Document	RZ/T1 Group User's Manual Hardware Rev1.0 R01UH0483EJ0100 Rev.1.00		

Several wrong description of Delta Sigma Interface (DSMIF) specification in the RZ/T1 Group User's Manual Hardware Rev1.0. have been found.

This document describes corrections for the wrong description.

1. Summary

DSMIF Status register and Error Control Module(ECM) always report errors, if you make control program for DSMIF in RZ/T1 referring to User's Manual Hardware Rev1.0(Fig 41.9).

Additionally, ECM for DSMIF UNIT1 always reports errors because of wrong description of both register address of DSMIF and ECM Error source number in the User's Manual.

The detail is described in the following section 2 and 3.

These wrong description will be corrected in the revised edition of the RZ/T1 Group User's Manual Hardware.

2. Details of a correction

table 1.1 A list of errata(1)

page	Objects	Before correction	After correction
p.179	XYZ overcurrent abnormality detection lower limit setting register	Address : A007 2088h	Address:A007 2098h
p.179	XYZ overcurrent abnormality detection upper limit setting register	Address : A007 208Ch	Address : A007 209Ch
p.2263	The chart of the register	b8 —	b8 ERXI
p.2263	The chart of the register	b0 ERXI	b0 —
P.2263	XYZ Status Register (XYZSTA) Bit : b0	Symbol : ERXI Bit Name : Channel 3 (X) Overcurrent Abnormality Detection Status Description : This indicates the detection ~ Clearing condition: Writing 1 to this bit after it has been set to 1.	Symbol : - Bit Name : Reserved Description : The read value is undefined. The write value should be 0.

table 1.2 A list of errata(2)

page	Objects	Before correction	After correction
p.2263	XYZ Status Register (XYZSTA) Bit : b8	Symbol : - Bit Name : Reserved Description : These bits are read as 0. The write value should be 0.	Symbol : ERXI Bit Name : Channel 3 (X) Overcurrent Abnormality Detection Status Description : This bit indicates the detection of an overcurrent abnormality on channel 3 (X). 0: Overcurrent abnormality has not been found. 1: Overcurrent abnormality has been found. Setting condition: Overcurrent abnormality being detected from the values of data on current in the X2DATA register. Clearing condition: Writing 1 to this bit after it has been set to 1.
p.2263	XYZ Status Register (XYZSTA) bit : b3 to b1	These bits are read as 0. The write value should be 0.	The read value is undefined. The write value should be 0.
p.2264	XYZ Overcurrent Abnormality Detection Lower Limit Setting Register (XYZIUNCMP)	Address : A007 2088h	Address : A007 2098h
p.2265	XYZ Overcurrent Abnormality Detection Upper Limit Setting Register (XYZIOVCMP)	Address : A007 208Ch	Address : A007 209Ch
p.2278	Figure 41.9	Figure 41.9 in the Users Manual.	Figure 1.1 in this report.

table 1.3 A list of errata(3)

page	Objects	Before correction	After correction
p.2280	41.5.1 Initial Settings for Error Sources after Release from the Module-Stop State	(1) Clear the error status register of the DSMIF.*1 (2) Clear the error state of the ECM DSMIF error numbers (no. 26 to 29 and 31). (3) Enable the ECM DSMIF error numbers (no. 26 to 29 and 31). (4) Start the DSMIF in accord with the setting procedures. (5) If a short-circuit abnormality detection error occurs, read the UVWSTA and XYZSTA registers to check if the error occurred in one of channels 0 to 3 (U, V, W, and X).*2 Note 1. Performing step (1) after step (2) does not create any problem.	(1)Mask an error output signal due to ECM Error Mask Register 0(no.26 to 28,30 and 31) The value of the bit28 should be 1. (2)Enable Operation. (3)Wait for filtering time. (4)Clear the error status register of the DSMIF.*1 (5)Clear the error state of the ECM DSMIF error numbers due to ECM Error Source Status Clear Trigger Register 0(no.26 to 28,30 and 31) (6) Enable the ECM DSMIF error numbers (no.26 to 28,30 and 31). (7)Unmask an error output signal due to ECM error Mask Register 0(no.26 to 28,30 and 31) (8) If a short-circuit abnormality detection error occurs, read the UVWSTA and XYZSTA registers to check if the error occurred in one of channels 0 to 3 (U, V, W, and X).*2 Note 1. Performing step (4) after step (5) does not create any problem.
p.2283	Table 42.2 ECM Error Input (Error Source Number 29)	Module : ΔΣ interface Function : X overcurrent abnormality detection error	Module : - Function : Reserved
p.2283	Table 42.2 ECM Error Input (Error Source Number 30)	Module : - Function : Reserved	Module : ΔΣ interface Function : X overcurrent abnormality detection error
p.2287	The chart of the register	b28 ECMmSSE028	b28 —
p.2287	The chart of the register	b29 —	b29 ECMmSSE029
p.2289	ECM Master/Checker Error Source Status Register 0 (ECMmESSTR0) bit : b28	Symbol : ECMmSE028 Bit Name : Error Source Status 29 Description : Indicates occurrence of an X ~ 1: Error occurred	Symbol : - Bit Name : Reserved Description : The read value is undefined.
p.2289	ECM Master/Checker Error Source Status Register 0 (ECMmESSTR0) bit : b29	Symbol : - Bit Name : Reserved Description : This bit is read as 0.	Symbol : ECMmSE029 Bit Name : Error Source Status 30 Description : Indicates occurrence of an X overcurrent abnormality detection error (error source 30). 0: Error not occurred 1: Error occurred
p.2293	The chart of the register	b28 ECMMIE028	b28 —

table 1.4 A list of errata(4)

page	Objects	Before correction	After correction
p.2293	The chart of the register	b29 —	b29 ECMMIE029
p.2295	ECM Maskable Interrupt Configuration Register 0 (ECMMICFG0) bit : b28	Symbol : ECMMIE028 Bit Name : ECM Maskable Interrupt Generation Control 29 Description : Enables or disables a maskable ~ 1: Interrupt generation enabled	Symbol : - Bit Name : Reserved Description : This bit is read as 0. The write value should be 0.
p.2295	ECM Maskable Interrupt Configuration Register 0 (ECMMICFG0) bit : b29	Symbol : - Bit Name : Reserved Description : This bit is read as 0. The write value should be 0.	Symbol : ECMMIE029 Bit Name : ECM Maskable Interrupt Generation Control 30 Description : Enables or disables a maskable interrupt due to occurrence of an X overcurrent abnormality detection error (error source 30). 0: Interrupt generation disabled 1: Interrupt generation enabled
p.2295	ECM Maskable Interrupt Configuration Register 0 (ECMMICFG0) bit : b30	Bit Name : ECM Maskable Interrupt Generation Control 30	Bit Name : ECM Maskable Interrupt Generation Control 31
p.2295	ECM Maskable Interrupt Configuration Register 0 (ECMMICFG0) bit : b31	Bit Name : ECM Maskable Interrupt Generation Control 31	Bit Name : ECM Maskable Interrupt Generation Control 32
p.2298	The chart of the register	b28 ECMNMIE028	b28 —
p.2298	The chart of the register	b29 —	b29 ECMNMIE029
p.2300	ECM Non-maskable Interrupt Configuration Register 0 (ECMNMICFG0) bit : b28	Symbol : ECMNMIE028 Bit Name : ECM Non-maskable Interrupt Generation Control 29 Description : Enables or disables a non-maskable ~ 1: Interrupt generation enabled	Symbol : - Bit Name : Reserved Description : This bit is read as 0. The write value should be 0.
p.2300	ECM Non-maskable Interrupt Configuration Register 0 (ECMNMICFG0) bit : b29	Symbol : - Bit Name : Reserved Description : This bit is read as 0. The write value should be 0.	Symbol : ECMNMIE029 Bit Name : ECM Non-maskable Interrupt Generation Control 30 Description : Enables or disables a non-maskable interrupt due to occurrence of an X overcurrent abnormality detection error (error source 30). 0: Interrupt generation disabled 1: Interrupt generation enabled

table 1.5 A list of errata(5)

page	Objects	Before correction	After correction
p.2303	The chart of the register	b28 ECMIRE028	b28 —
p.2303	The chart of the register	b29 —	b29 ECMIRE029
p.2305	ECM Internal Reset Configuration Register 0 (ECMIRCFG0) bit : b28	Symbol : ECMIRE028 Bit Name : ECM Internal Reset Generation Control 29 Description : Enables or disables generation ~ 1: ECM reset generation enabled	Symbol : - Bit Name : Reserved Description : This bit is read as 0. The write value should be 0.
p.2305	ECM Internal Reset Configuration Register 0 (ECMIRCFG0) bit : b29	Symbol : - Bit Name : Reserved Description : Do not write other than 0.	Symbol : ECMIRE029 Bit Name : ECM Internal Reset Generation Control 30 Description : Enables or disables generation of an ECM reset due to occurrence of an X overcurrent abnormality detection error (error source 30). 0: ECM reset generation disabled 1: ECM reset generation enabled
p.2305	ECM Internal Reset Configuration Register 0 (ECMIRCFG0) bit : b31	Bit Name : ECM Internal Reset Generation Control	Bit Name : ECM Internal Reset Generation Control 32
p.2308	The chart of the register	b29 —	b29 ECMEMK029
p.2310	ECM Error Mask Register 0 (ECMEMK0) bit : b28	Description : Controls whether to mask ~ 1: Error signal output masked	Description : The write value should be 1.
p.2310	ECM Error Mask Register 0 (ECMEMK0) bit : b29	Symbol : - Bit Name : Reserved Description : Do not write other than 0.	Symbol : ECMEMK029 Bit Name : ECM Error Output Signal Mask Control 30 Description : Controls whether to mask an error output signal due to occurrence of an X overcurrent abnormality detection error (error source 30). 0: Error signal output not masked 1: Error signal output masked
p.2313	The chart of the register	b28 ECMCLSSE028	b28 —
p.2313	The chart of the register	b29 —	b29 ECMCLSSE029

table 1.6 A list of errata(6)

page	Objects	Before correction	After correction
p.2315	ECM Error Source Status Clear Trigger Register 0 (ECMESSTC0) bit : b28	Symbol : ECMCLSSE028 Bit Name : ECM Error Status Clear 29 Description : Clears the error status ~ 1: Corresponding error status cleared	Symbol : - Bit Name : Reserved Description : This bit is read as 0. The write value should be 0.
p.2315	ECM Error Source Status Clear Trigger Register 0 (ECMESSTC0) bit : b29	Symbol : - Bit Name : Reserved Description : Do not write other than 0.	Symbol : ECMCLSSE029 Bit Name : ECM Error Status Clear 30 Description : Clears the error status of X overcurrent abnormality detection error (error source 30) and the ECMmESSTR0.ECMmSSE029 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared
p.2318	ECM Protection Status Register (ECMPS) bit : b0	R/W : W	R/W : R
p.2318	ECM Protection Status Register (ECMPS) bit : b7 to b1	Description : The write value should be 0. R/W : W	Description : This bit is read as 0. R/W : R
p.2319	The chart of the register	b28 ECMPE028	b28 —
p.2319	The chart of the register	b29 —	b29 ECMPE029
p.2321	ECM Pseudo Error Trigger Register 0 (ECMPE0) bit : b28	Symbol : ECMPE028 Bit Name : ECM Pseudo Error Trigger 29 Description : Generates a pseudo X ~ 1: Generates corresponding pseudo error	Symbol : - Bit Name : Reserved Description : This bit is read as 0. The write value should be 0.
p.2321	ECM Pseudo Error Trigger Register 0 (ECMPE0) bit : b29	Symbol : - Bit Name : Reserved Description : Do not write other than 0.	Symbol : ECMPE029 Bit Name : ECM Pseudo Error Trigger 30 Description : Generates a pseudo X overcurrent abnormality detection error (error source 30). 0: Pseudo error not generated 1: Generates corresponding pseudo error
p.2326	The chart of the register	b28 ECMTE028	b28 —
p.2326	The chart of the register	b29 —	b29 ECMTE029

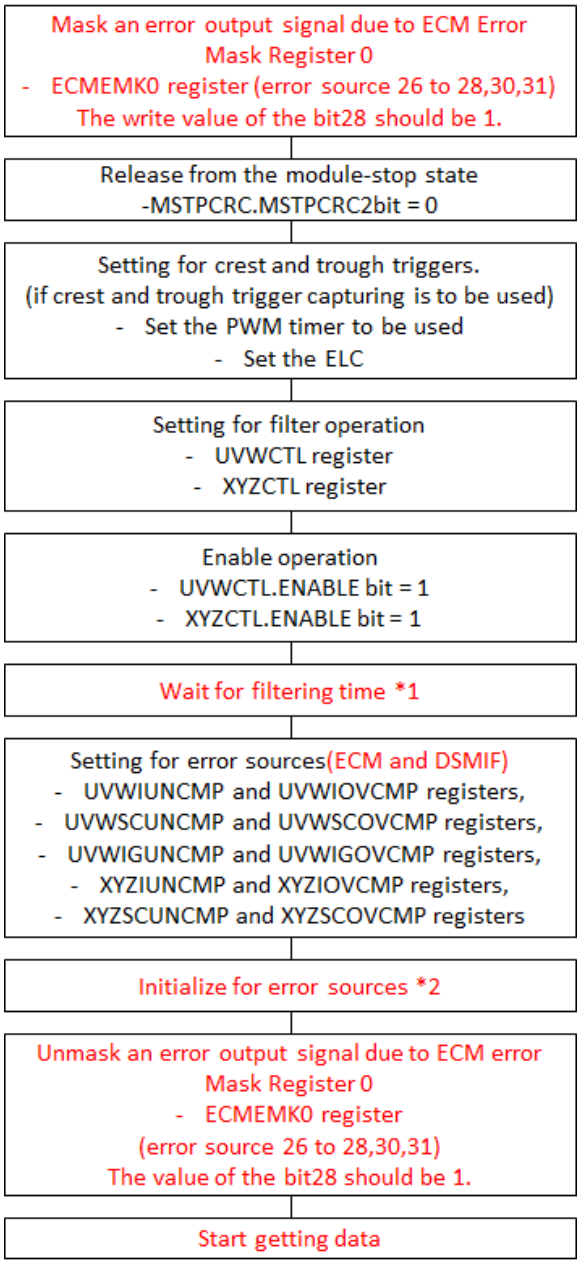
table 1.7 A list of errata(7)

page	Objects	Before correction	After correction
p.2328	ECM Delay Timer Configuration Register 0 (ECMDTMCFG0) bit : b28	Symbol : ECMTE028 Bit Name : ECM Delay Timer Start Control 29 Description : Enables delay timer ~ 1: Delay timer start enabled	Symbol : - Bit Name : Reserved Description : This bit is read as 0. The write value should be 0.
p.2328	ECM Delay Timer Configuration Register 0 (ECMDTMCFG0) bit : b29	Symbol : - Bit Name : Reserved Description : Do not write other than 0.	Symbol : ECMTE029 Bit Name : ECM Delay Timer Start Control 30 Description : Enables delay timer operation in response to an ECM maskable interrupt caused by an X overcurrent abnormality detection error (error source 30). 0: Delay timer start disabled 1: Delay timer start enabled
p.2332	The chart of the register	b28 ECMTE328	b28 —
p.2332	The chart of the register	b29 —	b29 ECMTE329
p.2334	ECM Delay Timer Configuration Register 3 (ECMDTMCFG3) bit : b28	Symbol : ECMTE328 Bit Name : ECM Delay Timer Start Control 29 Description : Enables delay timer operation ~ 1: Delay timer start enabled	Symbol : - Bit Name : Reserved Description : This bit is read as 0. The write value should be 0.
p.2334	ECM Delay Timer Configuration Register 3 (ECMDTMCFG3) bit : b29	Symbol : - Bit Name : Reserved Description : Do not write other than 0.	Symbol : ECMTE329 Bit Name : ECM Delay Timer Start Control 30 Description : Enables delay timer operation in response to an ECM non-maskable interrupt caused by an X overcurrent abnormality detection error (error source 30). 0: Delay timer start disabled 1: Delay timer start enabled

3. Detail of a correction for Fig.41.9 in the User's Manual

The revised points are described in red characters.

The description in black characters is unchanged, but please be noted the total sequence itself is changed.



Note 1 : Filtering time to wait :

Period of MCLK × Number of SINC stage[1-3]

＋ Period of decimation clock(max) × (6 ＋Number of SINC stage[1-3]) ＋ 5us

Period of decimation clock should be max value as setting register.

Note 2 : After release from the module-stop state, be sure to make initial settings for error sources in the error control module (ECM). For details, see section 41.5, Usage Notes.

Figure 1.1 Setting Procedure