To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A337A/E	Rev.	1.00
Title	Changes to Usage Notes on Clearing of Peripheral Module Interrupt Flag in the H8SX		Information Category	Technical Notification		
Applicable Product	H8SX/1650 Group, H8SX/1653 Group, and H8SX/1657 Group	Lot No. All lots	Reference Document	See below.		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the following changes to usage notes on clearing of peripheral module interrupt flag in the H8SX/1650 Group, H8SX/1653 Group, and H8SX 1657 Group Hardware Manuals.

1. Correction of Usage Notes on the Interrupt Controller

[Before change]

X.X Usage Notes

X.X.X Interrupts of Peripheral Modules

To clear an interrupt request flag by the CPU, the flag should be read from after clearing if the peripheral module clock is generated by dividing the system clock. This makes the request signal synchronized with the system clock. For details, see section xx.x.x, Notes on Clock Pulse Generator.

[After change]

X.X Usage Notes

X.X.X Interrupts of Peripheral Modules

To clear an interrupt request flag by the CPU, the flag must be read from after clearing within the interrupt processing routine even if the peripheral module clock is not generated by dividing the system clock. This makes the request signal synchronized with the system clock.

2. Modification in the Usage Notes on the Clock Pulse Generator

[Before change]

X.X.X Notes on Clock Pulse Generator

6. When Iϕ > Pϕ is specified by SCKCR, signals from the peripheral modules must be synchronized with the system clock. When CPU instructions are used to clear the interrupt source flag of a peripheral module, the flag must be read after being cleared to 0.

[After change]

The above description has been deleted.

3. Description Added to Register Bit of the Peripheral Modules

[Before change]

[Setting condition]

Omitted (No changes)

[Clearing condition]

- When writing 0 after reading XXX = 1

[After change]

[Setting condition]

Omitted (No changes)

[Clearing condition]

- When writing 0 after reading XXX = 1

  (When the CPU is used to clear an interrupt, the flag must be read after writing 0.)

Table 1 List of Target Products and Corresponding Modules

Target Products	Corresponding Modules
H8SX/1650 Group	ADC, SCI, TMR, TPU, and WDT
H8SX/1657 Group	ADC, SCI, TMR, TPU, and WDT
H8SX/1653 Group	ADC, IIC2, SCI, TMR, TPU, USB, and WDT

4. Target Products

Reference document: H8SX/1650 Group Hardware Manual (Rev. 2.00 REJ09B0029-0200Z)
H8SX/1653 Group Hardware Manual (Rev. 1.00 REJ09B0219-0100)
H8SX/1657 Group Hardware Manual (Rev. 1.00 REJ09B0106-0100Z)