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# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-RX*-A014A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Changes to Timing Specifications of the RIIC Module of RX630 Group | | Information Category | Technical Notification | | |
| Applicable Product | RX630 Group | Lot No.<br>All | Reference Document | RX630 Group User's Manual: Hardware Rev. 1.12 (R01UH0040EJ0112) | | |

This document describes changes to Table 45.18 “Timing of On-Chip Peripheral Modules (4)” and Table 45.19 “Timing of On-Chip Peripheral Modules (5)” in 45.4.5 “Timing of On-Chip Peripheral Modules” in Electrical Characteristics of RX630 Group User's Manual: Hardware Rev. 1.12.

1. Change of the symbol

   Changed the symbol from “(1/PCLK)” to “$t_{IICcyc}$” (RIIC)

   Changed the symbol from “(1/PCLK)” to “$t_{Pcyc}$” (Simple IIC)

   (hereinafter described as “tIICcyc” in 2 and 3).

2. Table 45.18 “Timing of On-Chip Peripheral Modules (4)”

   Changed the following specifications. The changes are underlined.

   2.1 RIIC (Standard-mode, SMBus) ICFER.FMPE=0

| Item | Symbol | | Before Change | After Change |
|---|---|---|---|---|
| SCL input cycle time | tSCL | min | 8(10) × (1/PCLK) + 1300 | 6(12) × tIICcyc + 1300 |
| SCL input high pulse width | tSCLH | min | 3(5) × (1/PCLK) + 300 | 3(6) × tIICcyc + 300 |
| SCL input low pulse width | tSCLL | min | 5 × (1/PCLK) + 1000 | 3(6) × tIICcyc + 300 |
| SCL, SDA input spike pulse removal time | tSP | max | 2 × (1/PCLK) | 1(4) × tIICcyc |
| SDA input bus free time | tBUF | min | 5 × (1/PCLK) + 1000 | 3(6) × tIICcyc + 300 |
| Start condition input hold time | tSTAH | min | 3(5) × (1/PCLK) + 300 | tIICcyc + 300 |
| Restart condition input setup time | tSTAS | min | 5 × (1/PCLK) + 1000 | 1000 |
| Stop condition input setup time | tSTOS | min | 3(5) × (1/PCLK) + 300 | 1000 |
| Data input setup time | tSDAS | min | 250 | tIICcyc + 50 |

2.2 RIIC (Fast-mode)

| Item | Symbol | | Before Change | After Change |
|---|---|---|---|---|
| SCL input cycle time | tSCL | min | 8(10) × (1/PCLK) + 600 | 6(12) × tIICcyc + 600 |
| SCL input high pulse width | tSCLH | min | 3(5) × (1/PCLK) + 300 | 3(6) × tIICcyc + 300 |
| SCL input low pulse width | tSCLL | min | 5 × (1/PCLK) + 300 | 3(6) × tIICcyc + 300 |
| SCL, SDA input spike pulse removal time | tSP | max | 2 × (1/PCLK) | 1(4) × tIICcyc |
| SDA input bus free time | tBUF | min | 5 × (1/PCLK) + 300 | 3(6) × tIICcyc + 300 |
| Start condition input hold time | tSTAH | min | 3(5) × (1/PCLK) + 300 | tIICcyc + 300 |
| Restart condition input setup time | tSTAS | min | 5 × (1/PCLK) + 300 | 300 |
| Stop condition input setup time | tSTOS | min | 3(5) × (1/PCLK) + 300 | 300 |
| Data input setup time | tSDAS | min | 100 | tIICcyc + 50 |

3. Table 45.19 “Timing of On-Chip Peripheral Modules (5)”

Changed the following specifications.

3.1 RIIC (Fast-mode+) ICFER.FMPE = 1

| Item | Symbol | | Before Change | After Change |
|---|---|---|---|---|
| SCL input cycle time | tSCL | min | 8(10) × (1/PCLK) + 240 | 6(12) × tIICcyc + 240 |
| SCL input high pulse width | tSCLH | min | 3(5) × (1/PCLK) + 120 | 3(6) × tIICcyc + 120 |
| SCL input low pulse width | tSCLL | min | 5 × (1/PCLK) + 120 | 3(6) × tIICcyc + 120 |
| SCL, SDA input spike pulse removal time | tSP | max | 4 × (1/PCLK) | 1(4) × tIICcyc |
| SDA input bus free time | tBUF | min | 5 × (1/PCLK) + 120 | 3(6) × tIICcyc + 120 |
| Start condition input hold time | tSTAH | min | 3(5) × (1/PCLK) + 120 | tIICcyc + 120 |
| Restart condition input setup time | tSTAS | min | 5 × (1/PCLK) + 120 | 120 |
| Stop condition input setup time | tSTOS | min | 3(5) × (1/PCLK) + 120 | 120 |
| Data input setup time | tSDAS | min | 50 | tIICcyc + 20 |

4. Revised versions of Tables 45.18 and 45.19

The following pages describe the revised versions of Tables 45.18 and 45.19. The changed values are shown in boldface in the tables.

Table 45.18 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a = T_{opr}$
High drive output is selected by the drive capacity control register.

| Item | | Symbol | Min.*1,*2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Standard-Mode, SMBus) ICFER.FMPE=0 | SCL input cycle time | $t_{SCL}$ | **6(12) × $t_{IICcyc}$** + 1300 | — | ns | Figure 45.37 |
| | SCL input high pulse width | $t_{SCLH}$ | 3**(6) × $t_{IICcyc}$** + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | **3(6) × $t_{IICcyc}$ + 300** | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | — | 1000 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | **1(4) × $t_{IICcyc}$** | ns | |
| | SDA input bus free time | $t_{BUF}$ | **3(6) × $t_{IICcyc}$ + 300** | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | **$t_{IICcyc}$** + 300 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | **1000** | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | **1000** | — | ns | |
| | Data input setup time | $t_{SDAS}$ | **$t_{IICcyc}$ + 50** | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |
| RIIC (Fast-mode) | SCL input cycle time | $t_{SCL}$ | **6(12) × $t_{IICcyc}$** + 600 | — | ns | |
| | SCL input high pulse width | $t_{SCLH}$ | 3**(6) × $t_{IICcyc}$** + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | **3(6) × $t_{IICcyc}$** + 300 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | **1(4) × $t_{IICcyc}$** | ns | |
| | SDA input bus free time | $t_{BUF}$ | **3(6) × $t_{IICcyc}$ + 300** | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | **$t_{IICcyc}$** + 300 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | **300** | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | **300** | — | ns | |
| | Data input setup time | $t_{SDAS}$ | **$t_{IICcyc}$ + 50** | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

tIICcyc: Cycle of the RIIC internal reference clock (IICϕ)

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. Cb is the total capacitance of the bus lines.

Table 45.19 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a = T_{opr}$
High drive output is selected by the drive capacity control register.

| Item | | Symbol | Min.*1,*2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Fast-mode+) ICFER.FMPE=1 | SCL input cycle time | $t_{SCL}$ | **6(12) × $t_{IICcyc}$** + 240 | — | ns | Figure 45.37 |
| | SCL input high pulse width | $t_{SCLH}$ | **3(6) × $t_{IICcyc}$** + 120 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | **3(6) × $t_{IICcyc}$** + 120 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | — | 120 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 120 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | **1(4) × $t_{IICcyc}$** | ns | |
| | SDA input bus free time | $t_{BUF}$ | **3(6) × $t_{IICcyc}$** + 120 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | **$t_{IICcyc}$** + 120 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | **120** | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | **120** | — | ns | |
| | Data input setup time | $t_{SDAS}$ | **$t_{IICcyc}$ + 20** | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 550 | pF | |
| Simple IIC (Standard-mode) | SDA input rise time | $t_{Sr}$ | — | 1000 | ns | |
| | SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × **$t_{Pcyc}$** | ns | |
| | Data input setup time | $t_{SDAS}$ | 250 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |
| Simple IIC (Fast-mode) | SCL, SDA input rise time | $t_{Sr}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × **$t_{Pcyc}$** | ns | |
| | Data input setup time | $t_{SDAS}$ | 100 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

tIICcyc: Cycle of the RIIC internal reference clock (IIC□), tPcyc: Cycle of the PCLK

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. Cb indicates the total capacity of the bus line.