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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A055A/E	Rev.	1.00
Title	Changes to Descriptions and Addition of Note on A/D Conversion Characteristics in the RX210 Group		Information Category	Technical Notification		
Applicable Product	RX210 Group	Lot No. All	Reference Document	RX210 Group User's Manual: Hardware Rev.1.30 (R01UH0037EJ0130)		

This document describes changes to descriptions and addition of a note on A/D conversion characteristics in RX210 Group User's Manual: Hardware Rev.1.30.

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Descriptions about the PCLKD frequency in Conditions and Note 3 in Table 42.61 A/D Conversion Characteristics (1) are moved to the first row of the table as a specification. A note is added as Note 4.

Before change

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, 2.7 V ≤ VREFH0 = (AVCC0 - 0.9 V) to AVCC0[*4],
VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKD = 1 to 50 MHz, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	—	12	Bit	
Conversion time[*1] (Operation at fPCLKD = 50 MHz)[*3]	Permissible signal source impedance (Max.) = 0.5 kΩ	1.0 (0.4)[*2]	—	—	μs	Sampling in 20 states
	Permissible signal source impedance (Max.) = 1 kΩ	1.1 (0.5)[*2]	—	—		Sampling in 25 states
	Permissible signal source impedance (Max.) = 5 kΩ	1.5 (0.9)[*2]	—	—		Sampling in 45 states
Omitted						
Absolute accuracy		—	± 1.25	± 5.0	LSB	High-precision channel
		—	± 1.25	± 8.0	LSB	Normal-precision channel
DNL differential nonlinearity error		—	± 1.0	—	LSB	
INL integral nonlinearity error		—	± 1.0	± 3.0	LSB	

Note 3. The lower-limit frequency of PCLKD is 1 MHz.

Note 4. When using the temperature sensor, use it when AVCC0 = VREFH0.

After change

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 ≥ 2.7 V, AVCC0 - 0.9 V ≤ VREFH0 ≤ AVCC0[*3],
VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		1	—	50	MHz	
Resolution		—	—	12	Bit	
Conversion time[*1] (Operation at fPCLKD = 50 MHz)[*3]	Permissible signal source impedance (Max.) = 0.5 kΩ	1.0 (0.4)[*2]	—	—	μs	Sampling in 20 states
	Permissible signal source impedance (Max.) = 1 kΩ	1.1 (0.5)[*2]	—	—		Sampling in 25 states
	Permissible signal source impedance (Max.) = 5 kΩ	1.5 (0.9)[*2]	—	—		Sampling in 45 states
Omitted						
Absolute accuracy		—	± 1.25	± 5.0	LSB	High-precision channel[*4]
		—	± 1.25	± 8.0	LSB	Normal-precision channel
DNL differential nonlinearity error		—	± 1.0	—	LSB	[*4]
INL integral nonlinearity error		—	± 1.0	± 3.0	LSB	[*4]

Note 3. When using the temperature sensor, use it when AVCC0 = VREFH0.

Note 4. When using the sample-and-hold circuit, 0.25 ≤ analog input voltage ≤ AVCC - 0.25 V.

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Descriptions about the PCLKD frequency in Conditions and Note 3 in Table 42.64 A/D Conversion Characteristics (2) are moved to the first row of the table as a specification. The maximum value of the PCLKD frequency is corrected.

Before change

Conditions: VCC = AVCC0 = 1.8 to 3.6 V, VREFH0 = 1.8 to 2.7 = (AVCC0 . 0.9 V) to AVCC0*4,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKD = 1 to 32 MHz, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at fPCLKD = 25 MHz)*3	Permissible signal source impedance (Max.) = 1 kΩ	2.0 (0.8)*2	—	—	µs	Sampling in 20 states
	Permissible signal source impedance (Max.) = 5 kΩ	2.2 (1.0)*2	—	—		Sampling in 25 states
Omitted						

Note 3. The lower-limit frequency of PCLKD is 1 MHz.

Note 4. When using the temperature sensor, use it when AVCC0 = VREFH0.

After change

Conditions: VCC = AVCC0 = 1.8 to 3.6 V, 1.8 V ≤ VREFH0 ≤ 2.7 V, AVCC0 - 0.9 V ≤ VREFH0 ≤ AVCC0*3,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		1	—	25	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at fPCLKD = 25 MHz)*3	Permissible signal source impedance (Max.) = 1 kΩ	2.0 (0.8)*2	—	—	µs	Sampling in 20 states
	Permissible signal source impedance (Max.) = 5 kΩ	2.2 (1.0)*2	—	—		Sampling in 25 states
Omitted						

Note 3. When using the temperature sensor, use it when AVCC0 = VREFH0.

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Descriptions about the PCLKD frequency in Conditions and Note 3 in Table 42.65 A/D Conversion Characteristics (3) are moved to the first row of the table as a specification. The maximum value of the PCLKD frequency is corrected.

Before change

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VREFH0 = AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, fPCLKD = 1 to 16 MHz, Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at fPCLKD = 12.5 MHz)*3	Permissible signal source impedance (Max.) = 1 kΩ	3.36 (0.96)*2	—	—	µs	Sampling in 12 states
	Permissible signal source impedance (Max.) = 5 kΩ	3.6 (1.2)*2	—	—		Sampling in 15 states
Omitted						

Note 3. The lower-limit frequency of PCLKD is 1 MHz.

After change

Conditions: VCC = AVCC0 = 1.62 to 1.8 V, VREFH0 = AVCC0,
VSS = AVSS0 = VREFL = VREFL0 = 0 V, Ta = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		1	—	12.5	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at fPCLKD = 12.5 MHz)	Permissible signal source impedance (Max.) = 1 kΩ	3.36 (0.96)*2	—	—	µs	Sampling in 12 states
	Permissible signal source impedance (Max.) = 5 kΩ	3.6 (1.2)*2	—	—		Sampling in 15 states
Omitted						