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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A063A/E	Rev.	1.00
Title	Change in the RX63N group and RX631 Group User's Manual concerning the sub-clock oscillator of the 64pin products of the RX631 group		Information Category	Technical Notification		
Applicable Product	RX631 Group (R5F5631PCDFM, R5F5631PDDFM, R5F5631NCDFM, R5F5631NDDFM, R5F5631MCDFM, R5F5631MDDFM)	Lot No.: All	Reference Document	RX63N Group, RX631 Group User's Manual: Hardware Rev. 1.60 (R01UH0041EJ0160)		

This technical update is inform you that some description about the sub-clock oscillator of 64pin products have been added to the User's Manual of the RX63N group and RX631 group, Hardware version Rev.1.60, as indicated below.

1. The following description about how to specify the initial value and sub-clock oscillator wait time select bit (SSTS[4:0] bits) of the 64pin products has been added the chapter of "11.2.8 Sub-Clock Oscillator Wait Control Register (SOSCWTCR)." The portion added is identified by underlining.

・Initial value of the sub-clock oscillator wait control register (SOSCWTCR)

Address(es): 0008 00A3h

	b7	b6	b5	b4	b3	b2	b1	b0	
	—	—	—	SSTS[4:0]					
Value after reset:	0	0	0	0	0	0	0	0	for products with 100 pins or more
	0	0	0	0	0	1	1	0	for the 64pin products

・How to specify the sub-clock oscillator wait time select bit (SSTS[4:0] bits) of the 64pin products

For the 64pin products, set the SSTS[4:0] bits so that the waiting time is at least as long as the sub-clock oscillator stabilization time (tSUBOSC).

Exampmle: When oscillation is at 32.768kHz and crystal resonator is to be used after 2s (=2000ms) of stabilization time

To satisfy the relation waiting time ≥tSUBOSC × fSUB = 2000[ms] × 32.768[kHz] = 65536[cycles], set the SSTS[4:0] bits to 01100b (65536 cycles).

2. The description about calculating the sub-clock oscillation stabilization wait time (tSUBOSCWT) of the 64pin products has been added to the section of "Table 50.12 Clock Timing (Sub-Clock Related)" as indicated below. The portion added is identified by underlining.

For the 64pin products, the number of cycles n selected by the value of the SOSCWTCR.SSTS[4:0] bits determines the sub-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{SUBOSCWT} = t_{SUBOSC} + \frac{n}{f_{SUB}}$$