RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A060A/E	Rev.	1.00
Title	Caution on using wait mode and stop mode		Information Category	Technical Notification		
Applicable Product	R8C/36T-A, R8C/38T-A	Lot No.	Reference Document	Latest user's Manual: applicable products	Hardware	e of

This caution below applies to wait mode and stop mode in the above mentioned Applicable Products.

1. Description

The Interrupt request bit(IR bit) of the Interrupt Control Register may not be set to "1"(Interrupt requested), when two or more peripheral function interrupts to be used for exiting wait mode/stop mode are generated simultaneously under the condition that there are two or more peripheral functions and their operations in wait mode/stop mode are enabled ^{Note 1}. In this case, the interrupt request flag will not be set to "1" and interrupt processing will not be executed even though another same interrupt source is generated.

Note 1. The peripheral functions, the interrupt request bit (the IR bit in the corresponding interrupt control register) of which is set to "1" (interrupt requested) in wait mode/stop mode.

2. Conditions

The problem described above occurs when all the following conditions are met.

(1) In Wait mode/Stop mode

(2) There are two or more peripheral functions and their operations in wait mode/stop mode are enabled.



3. Countermeasure

Execute the following countermeasure in your software.

- Setting the I flag of flag register to "0"(disable interrupts) before entering wait mode/stop mode.
- After exiting wait mode/stop mode, check the interrupt request flag of the peripheral function.
- If the peripheral function interrupt flag is set to "1", set the IR bit in the corresponding interrupt control register to "1".

• And then, setting the I flag of flag register to "1"(enable interrupts). In this way, the interrupts which have been generated can be processed properly.

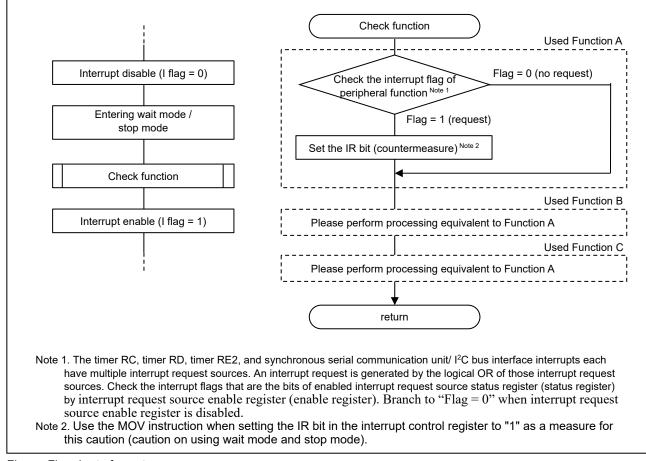


Figure. Flowchart of countermeasure

3.1 Caution on software measures

- To enter wait mode, disable the interrupts (set the I flag in the Flag register (FLG) to "0") and set the CM30 bit in the CM3 register to "1". Don't use the WAIT instruction.
- To enter stop mode, disable the interrupts (set the I flag in the Flag register (FLG) to "0") and set the CM10 bit in the CM1 register to "1".
- When an "interrupt-judging function" is called as a measure for this caution (caution on using wait mode and stop mode), the stack area are consumed.



3.2 Description of judgement bit

The following table shows the interrupt source, the interrupt flags of its peripheral functions and the interrupt request bit.

Interrupt Source	Interrupt flag of the peripheral functions	Interrupt request bit	References
INT4	INT4S bit in the INTSTS register Note 2	IR bit in the INT4IC register	3.3(1) ,3.3(13)
Timer RC_0	Each bit in the TRCSR_0 register Note 1	IR bit in the TRCIC_0 register	3.3(2) ,3.3(13)
Timer RE2	Each bit in the TREIFR register Note 1	IR bit in the TRE2IC register	3.3(3) ,3.3(13)
UART2 transmit/NACK2	U2TIF bit in the U2IR register Note 2	IR bit in the U2TIC register	3.3(4) ,3.3(13)
UART2 receive/ACK2	U2RIF bit in the U2IR register Note 2	IR bit in the U2RIC register	3.3(4) ,3.3(13)
Key input	KIIS bit in the KIS register Note 2	IR bit in the KUPIC register	3.3(5) ,3.3(13)
Synchronous serial communication unit/ I ² C	Each bit in the SISR_0 register Note 1	IR bit in the SSUIC_0/ IICIC_0 register	3.3(6) ,3.3(13)
bus interface			
UART0_0 transmit	U0TIF bit in the U0IR_0 register Note 2	IR bit in the U0TIC_0 register	3.3(7) ,3.3(13)
UART0_0 receive	U0RIF bit in the U0IR_0 register Note 2	IR bit in the U0RIC_0 register	3.3(7) ,3.3(13)
UART0_1 transmit	U0TIF bit in the U0IR_1 register Note 2	IR bit in the U0TIC_1 register	3.3(7) ,3.3(13)
UART0_1 receive	U0RIF bit in the U0IR_1 register Note 2	IR bit in the U0RIC_1 register	3.3(7) ,3.3(13)
INT2	INT2S bit in the INTSTS register Note 2	IR bit in the INT2IC register	3.3(1) ,3.3(13)
Timer RJ_0	LINIF bit in the LINIR_0 register Note 2	IR bit in the TRJIC_0 register	3.3(8) ,3.3(13)
Timer RB2_0	TRBIF bit in the TRBIR_0 register	IR bit in the TRB2IC_0 register	3.3(9) ,3.3(13)
INT1	INT1S bit in the INTSTS register Note 2	IR bit in the INT1IC register	3.3(1) ,3.3(13)
INT3	INT3S bit in the INTSTS register Note 2	IR bit in the INT3IC register	3.3(1) ,3.3(13)
INT0	INT0S bit in the INTSTS register Note 2	IR bit in the INT0IC register	3.3(1) ,3.3(13)
UART2 bus	U2BCNIF bit in the U2IR register Note 2	IR bit in the U2BCNIC register	3.3(4) ,3.3(13)
collision detection			
Voltage monitor 1 Note 3	VW1C2 bit in the VW1C register	IR bit in the VCMP1IC register	3.3(10) ,3.3(13)
Voltage monitor 2 Note 3	VW2C2 bit in the VW2C register	IR bit in the VCMP2IC register	3.3(11) ,3.3(13)
TSCU	SIF bit in the TSCUFR register	IR bit in the TSCUIC register	3.3(12) ,3.3(13)

Table. Interrupt flag of the peripheral functions

Note:

1. The bits of status register that the corresponding interrupt enable bits are set to 1.

2. Refer to "3.3 Register and flag used in a judgement" for the details on the applicable registers and bits.

3. The interrupt source is enabled only when the maskable interrupt is selected.



3.3 Register and flag used in judgement The red words (registers and bits) are not described in Hardware manual. In the case of not applicable, it is not necessary to change the software of these registers and bits. (1) INT Interrupt Status Register (INTSTS) Address: 00235h (INTSTS) Bit b7 b6 b5 b4 b3 b2 b1 b0 Symbol INT4S INT3S INT2S INT1S INT0S --After Reset 0 0 0 0 0 0 0 R/W Bit Symbol Bit Name Function INT0 interrupt request flag Note 1,2 **INTOS** R/W b0 INT1 interrupt request flag Note 1,2 b1 INT1S R/W 0: No interrupt requested INT2 interrupt request flag Note 1,2 b2 INT2S R/W 1: Interrupt requested INT3 interrupt request flag Note 1,2 INT3S R/W b3 b4 INT4S INT4 interrupt request flag Note 1,2 R/W b5-b7 R/W Reserved Set to 0. -Note 1. [Conditions for setting to 0] ·When the corresponding IR bit changes from 1 to 0 •When 0 is written to this bit after reading it as 1. [Conditions for setting to 1] ·When the corresponding interrupt request occurs Note 2. The results writing this bit are as follows. · If 1 is read, writing 0 to the same bit is to 0. ·If 0 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, it remains 1 even if 0 is written.) ·The bit remains unchanged if 1 is written to it. (2) Timer RC 0 Status Register (TRCSR 0) Address: 00145h (TRCSR 0) Bit b7 b6 b5 b4 b3 b2 b1 b0 OVF IMFD IMFC IMFB IMFA Symbol _ After Reset 1 1 1 0 0 0 0 0 Bit Name Function R/W Bit Symbol [Conditions for setting to 0] Input capture/ compare • When 0 is written to this bit after reading it as 1. b0 IMFA R/W match A flag · Set to 0 by the DTC acknowledge when the DTC is activated by an IMFi interrupt. Input capture/ compare [Condition for setting to 1] R/W b1 IMFB match B flag Input Capture Function When the value of the TRCCNT register is transferred to the TRCGRA register at the input edge of the TRCIOi Input capture/ compare R/W b2 IMFC pin. match C flag Output Compare Function/ PWM Mode/ PWM2 Mode Input capture/ compare When the values of registers TRCCNT and TRCGRi R/W b3 IMFD match D flag match. (i = A to D) b4-b6 Nothing is assigned. The write value must be 1. The read value is 1. _ _ [Conditions for setting to 0] • When 0 is written to this bit after reading it as 1. R/W b7 OVF Timer overflow flag [Condition for setting to 1] • When the TRCCNT register overflows from FFFFh to 0000h.



(3) Timer RE2	Interrupt Flag	Register	(TREIER)
	monupering	rtogiotor	(

Real-Time Clock Mode

Address: 0017Ah (TREIFR)

Address	s: 0017AN (I REIFR)								- 1
	Bit	b7	b6	b5	b4	b3	b2	b1	b0	
	Symbol	TADJSF	-	-	RSTADJ	ADJ30S	ALIE	RTCF	ALIF	
Aft	er Reset	0	0	0	0	0	0	0	0	
Bit	Symbol		Bit Na	me			Function		R/W] [
b0	AL IF	Alarm int	errupt flag		0. N	o interrupt red	nuested		R/W	11

BIt	Symbol	Bit Name	Function	R/W
b0	ALIF	Alarm interrupt flag	0: No interrupt requested	R/W
b1	RTCF	Real-time clock periodic interrupt flag	1: Interrupt requested	R/W
b2	ALIE	Alarm interrupt anable hit	0: Alarm interrupt disabled	R/W
DZ	ALIE	Alarm interrupt enable bit	1: Alarm interrupt enabled	r///
			When 1 is written to this bit, the value of the	
			TRESEC register changes as follows.	
			When TRESEC register value \leq 29:	
b3	ADJ30S	30-second adjustment bit	TRESEC←00	W
			When TRESEC register value \geq 30:	
			TRESEC←00、TREMIN←TREMIN+1	
			The read value is 0.	
			When 1 is written to this bit, the value of the	
b4	RSTADJ	Cocond counter react adjustment hit	TRESEC register is set to 00 and the initial	w
04	KSTADJ	Second counter reset adjustment bit	Counter is initialized.	vv
			The read value is 0.	
b5-b6	_	Nothing is assigned. The write value mus	t be 0. The read value is 0.	-
b7		Correction status flag	0: No correction	R/W
10	TADJSF Correction status flag		1: Being correction	FX/ VV

Address: 0017Bh (TREIER)

, luaroo	Bit	b7	b6	b5	b4	b3	b2	b1	b0
	Symbol	YRIE	MOIE	DYIE	HRIE	MNIE	SEIE	SEIE05	SEIE025
Af	ter Reset	0	0	0	0	0	0	0	0
Bit	Symbol		Bit Name			R/W			
b0	SEIE025		interrupt trigg onds enable	•	disable		-	.25 seconds .25 seconds	R/W
b1	SEIE05		interrupt trigg nds enable b		disable	interrupt trigg interrupt trigg	-		R/W
b2	SEIE		interrupt trigg enable bit	jered every	0: Periodic 1: Periodic	RVW			
b3	MNIE	Periodic minute e	interrupt trigg nable bit	jered every			-	ninute disable ninute enable	R/W
b4	HRIE	Periodic hour ena	interrupt trigg ble bit	jered every		interrupt trigg	•		R/W
b5	DYIE	Periodic day enat	interrupt trigg ble bit	jered every	0: Periodic	interrupt trigg	ered every d	lay disable	R/W
b6	MOIE	Periodic month er	interrupt trigg nable bit	jered every			-	nonth disable nonth enable	R/W
b7	YRIE	Periodic year ena	interrupt trigg ble bit	jered every	0: Periodic interrupt triggered every year disable 1: Periodic interrupt triggered every year enable				



	000D8h (U2IR)								
	Bit	57	b6	b5	b4		53	b2	b1	b
:	Symbol U2	2TIF	U2RIF	U2NAKIF	U2BC	NIF	-	-	-	_
After	Reset	0	0	0	0		0	0	0	C
Bit	Symbol			Bit Name			I	Fund	ction	
b0-b3	-	Rese	rved				Set to			
b4	U2BCNIF			ection interrupt		lag Note 1,2				
b5	U2NAKIF	NAC	K interrupt re	equest flag Note	1,2				requested	
b6	U2RIF	Rece	ive interrupt	request flag [№]	te 1,2	2	1: Inte	errupt requ	uested	
b7	U2TIF Conditions for s			errupt request	liag nete 1,	-				
[(Note 2. T	When 0 is wri Conditions for s When the cor he results writi If 1 is read, writer	tten to the setting to respond ing this b ting 0 to iting 0 to iting 0 to	his bit after r o 1] ing interrupt bit are as foll the same b o the same vritten.)	request occurs ows. it is to 0. bit does not ch	5	(If the bit	change	s from 0 t	o 1 after a 0	is rea
-	terrupt Status F 00237h (KIS)	-								
		b7	b6	b5	b4	b3		b2	b1	bC
		IIS	-	-	-	-		-	-	-
Απε	er Reset	0	0	0	0	0		0	0	0
Bit	Symbol		Bit	Name			F	unction		
b0-b6	-	Rese	rved			Set to 0.				
b7	KIIS	Kev i	nput interrur	ot request flag [™]	Note 1,2	0: No inter				
	Conditions for s					1: Interrup	reques	sted		
	•When 0 is wri Conditions for s	tten to the setting to	nis bit after r o 1]	anges from 1 to eading it as 1. request occurs						
Note 2. T	he results writi If 1 is read, wri	ng this b ting 0 to iting 0 tơ n if 0 is v	the same b o the same written.)	it is to 0. bit does not ch		(If the bit	change	s from 0 t	o 1 after a 0	is rea



(6) SI Status Register (SISR)

SSU Function:

Address: 000EAh (SISR_0)

Address:	000EAh (SIS	R_0)							
	Bit	b7	b6	b5	b4	b3	b2	b1	b0
	Symbol T	DRE	TEND	RDRF	NACKF	STOP	ORER_AL	AAS	CE_ADZ
Afte	er Reset	0	0	0	0	0	0	0	0
Bit	Symbol		Bit Na	me			Function		R/W
b0	CE_ADZ	Cor	nflict error flag		0: No co 1: Confli	nflict error ct error			R/W
b1	AAS	Res	served		Set to 0.				R/W
b2	ORER_AL	Ove	errun error flaç]	0: No ov 1: Overr	errun error un error			R/W
b3	STOP	Res	served		Set to 0.				R/W
b4	NACKF	Res	served		Set to 0.				R/W
b5	RDRF	Red	ceive data reg	ister full flag			RDR register e SIRDR regis	ter	R/W
b6	TEND	Tra	nsmit end flag	l	data is 1: The T	s transmitted	when the last		
b7	TDRE	Tra	nsmit data err	npty flag	SISDF	२ is transferred	erred from regis		R/W



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I ² C bus Fund	ction:										
Address:	000EAh	(SISR_	0)								
	Bit	b7	7	b6	b5	b4	b3	b2	b1		b0
	Symbol	TDF	RE	TEND	RDRF	NACKF	STOP	ORER_AL	AAS	CE	_ADZ
Afte	er Reset	0		0	0	0	0	0	0		0
Bit	Sym	bol		Bit Nam	ne		F	unction			R/W
b0	CE_A	ADZ		eral call add	ress	This flag is s detected.	set to 1 wher	n a general ca	ll address is		R/W
b1	AA	S	Slav flag	ve address re	ecognition	after the sta the SIMR2 r	This flag is set to 1 when the first frame immediately after the start condition matches bits SVA0 to SVA6 in the SIMR2 register in slave receive mode (slave address detection, general call address detection).				
b2	In I²C bus interface mode, this flag indicates that arbitration is lost in master mode. This flag is set to 1 when: • The internal SDA signal and SDA pin level do not match at the rising edge of the SCL signal in master transmit mode • The SDA pin is beld bigh at start condition detection							R/W			
b3	STO)P	Stop flag	condition de	etection	This flag is s after the frar		n a stop condit erred.	ion is detected	b	R/W
b4	NAC	KF	No a flag	acknowledge	detection	detected		n no ACKnowle after transmiss	C		R/W
b5	RDF	RF	Rec flag	eive data reg	jister full	This flag is s from registe		n receive data SIRDR.	is transferred		R/W
b6	TEN	۱D	Trar	nsmit end flaç	9	In I ² C bus interface mode, this flag is set to 1 at the rising edge of the 9th clock cycle of the SCL signal while the TDRE bit is 1. In clock synchronous mode, this flag is set to 1 when the last bit of the transmit frame is transmitted.					R/W
b7	TDF	RE	Trar	nsmit data en	npty flag	and the SI • The TRS b (transmit r • A start con retransmis	nsferred fror TDR registe bit in the SIC mode) idition is gen ssion)	n: n registers SIT r becomes em R1 register is s erated (includi is changed to	pty. set to 1 ing		R/W



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Bit Symbolb7 UOREb6 UOREb3 Cb2 Cb1 Cb0 CAfter Reset0000000BitSymbolBit NameFunctionRAb2-b1Nothing is assigned. The write value must be 0. The read value is 0b2UORIEUART0 receive interrupt enabled it1: Receive interrupt enabledRAb3UUTIEUART0 transmit interrupt enable bit0: Transmit interrupt enabledRAb4-Nothing is assigned. The write value must be 0. The read value is 0b6UORIFUART0 transmit interrupt request flag0: Not interrupt requestedRAb7UOTIFUART0 transmit interrupt request flag1: Interrupt requestedRAb7UOTIFUART0 transmit interrupt request flag1: Interrupt requestedRAb7UOTIFUART0 transmit interrupt request occursNote 1. [Conditions for setting to 1]	Symbol UOTIF UORIF - - UOTIE UORIE - - After Reset 0	Address.	00088h (U0IR_								
After Reset 0 <th< td=""><td>After Reset 0 <th< td=""><td></td><td></td><td></td><td></td><td></td><td>b4</td><td></td><td></td><td>b1</td><td>b0</td></th<></td></th<>	After Reset 0 <th< td=""><td></td><td></td><td></td><td></td><td></td><td>b4</td><td></td><td></td><td>b1</td><td>b0</td></th<>						b4			b1	b0
Bit Symbol Bit Name Function RA b0-b1 - Nothing is assigned. The write value must be 0. The read value is 0. - b2 UORIE UART0 receive interrupt enable bit 0: Receive interrupt disabled RA b3 UOTIE UART0 transmit interrupt enable bit 0: Transmit interrupt disabled RA b4-b5 - Nothing is assigned. The write value must be 0. The read value is 0. - b6 UORIF UART0 receive interrupt request flag ^{Nos 1.2} 0: No interrupt requested RA b7 UOTIF UART0 receive interrupt request flag ^{Nos 1.2} 1: Interrupt requested RA Note 1. [Conditions for setting to 0] •When the corresponding IR bit changes from 1 to 0 •When the corresponding interrupt request flag ^{Nos 1.2} 1: Interrupt requested RA VWhen 0 is writing this bit are as follows. •If 1 is read, writing 0 to the same bit to 0. •If 0 is read, writing 0 to the same bit to 0. •If 0 is read, writing 0 to the same bit so 0. •If 0 is read. VILIN Interrupt request flag ^{Nos 1.2} • • • • Symbol 57 b6 b5 b4 b3 b2 b1 b0	Bit Symbol Bit Name Function R// b0-b1 - Nothing is assigned. The write value must be 0. The read value is 0. - b2 UORIE UART0 receive interrupt enable bit 0: Receive interrupt disabled R/ b3 UOTIE UART0 transmit interrupt enable bit 0: Transmit interrupt disabled R/ b4-b5 - Nothing is assigned. The write value must be 0. The read value is 0. - b6 UORIF UART0 receive interrupt request flag ^{Nos 1.2} 0: No interrupt requested R/ b7 UOTIF UART0 receive interrupt request flag ^{Nos 1.2} 0: No interrupt requested R/ b7 UOTIF UART0 receive interrupt request flag ^{Nos 1.2} 0: No interrupt requested R/ b7 UOTIF UART0 responding interrupt request flag ^{Nos 1.2} 0: No interrupt requested R/ b7 UOTIF UART0 rease of lows. 1: To reasits writing this bit are as follows. 1: 1 · If 1 is read, writing 0 to the same bit to 0. · If 0 is read, writing 0 to the same bit to 0. · If 1 is read, writing 0 to the						-			-	-
b0-b1 - Nothing is assigned. The write value must be 0. The read value is 0. - b2 UQRIE UART0 receive interrupt enable bit 0: Receive interrupt enabled RA b3 UUTIE UART0 transmit interrupt enable bit 0: Transmit interrupt enabled RA b4-b5 - Nothing is assigned. The write value must be 0. The read value is 0. - b6 UORIF UART0 receive interrupt request flag ^{Note 1.2} 0: No interrupt requested RA b7 UORIF UART0 transmit interrupt request flag ^{Note 1.2} 0: No interrupt requested RA b7 UORIF UART0 transmit interrupt request flag ^{Note 1.2} 1: Interrupt requested RA Note 1. [Conditions for setting to 0] ···When 0 is written to this bit after reading it as 1. [Conditions for setting to 1] ···When 0 is written to this bit are as follows. · If 1 is read, writing 0 to the same bit to 0. ···If 0 is read, writing 0 to the same bit is to 0. ···If 1 is read, writing 0 to the same bit is to 0. · If 0 is read, writing 0 to the same bit is to 0. ···If 0 is read, writing 0 to the same bit is to 0. ···If 0 is read, writing 0 to the same bit is 0. · The bit remains unchanged if 1 is written to it. ····If 0 is read, writing 0 to the same bit is 0. ···	b0-b1 - Nothing is assigned. The write value must be 0. The read value is 0. - b2 U0RIE UART0 receive interrupt enable bit 0: Receive interrupt enabled R/ b3 U0TIE UART0 transmit interrupt enable bit 0: Transmit interrupt enabled R/ b4-b5 - Nothing is assigned. The write value must be 0. The read value is 0. R/ b4-b5 - Nothing is assigned. The write value must be 0. The read value is 0. R/ b7 UORIF UART0 receive interrupt request flag ^{Note 1.2} 0: No interrupt requested R/ b7 UORIF UART0 transmit interrupt request flag ^{Note 1.2} 0: No interrupt requested R/ b7 UORIF UART0 transmit interrupt request flag ^{Note 1.2} 1: Interrupt requested R/ Note 1. [Conditions for setting to 0] ···When 0 is written to this bit after reading it as 1. [Conditions for setting to 1] ···When 0 is written to this written to 0. ··· If 0 is read, writing 0 to the same bit to 0. ··· If 0 is read, writing 0 to the same bit is to 0. ··· If 0 is read, writing 0 to the same bit is to 0. ··· If 0 is read, writing 0 to the same bit as 0. ··· If 0 is read, writing 0 to the same bit is to 0. ··· · · · · · · · · · · · · · · · · ·	Afte	r Reset ()	0	0	0	0	0	0	0
b0-b1 - Nothing is assigned. The write value must be 0. The read value is 0. - b2 UORIE UART0 receive interrupt enable bit 0: Receive interrupt enabled RA b3 UOTIE UART0 transmit interrupt enable bit 0: Transmit interrupt enabled RA b4-b5 - Nothing is assigned. The write value must be 0. The read value is 0. - b6 UORIF UART0 receive interrupt request flag ^{Note 1.2} 0: No interrupt requested RA b7 UORIF UART0 receive interrupt request flag ^{Note 1.2} 0: No interrupt requested RA b7 UORIF UART0 receive interrupt request flag ^{Note 1.2} 0: No interrupt requested RA Note 1. [Conditions for setting to 0] ··When the corresponding interrupt request flag ^{Note 1.2} 1: Interrupt requested RA ··When the corresponding interrupt request loccurs Note 2. The results writing 0 to the same bit is to 0. ··H 0 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, remains 1 even if 0 is written.) ··The bit remains unchanged if 1 is written to it.	b0-b1 - Nothing is assigned. The write value must be 0. The read value is 0. - b2 U0RIE UART0 receive interrupt enable bit 0: Receive interrupt disabled R/ b3 U0TIE UART0 transmit interrupt enable bit 0: Transmit interrupt enabled R/ b4-b5 - Nothing is assigned. The write value must be 0. The read value is 0. - b6 U0RIF UART0 receive interrupt request flag ^{Note 1.2} 0: No interrupt requested R/ b7 U0TIF UART0 receive interrupt request flag ^{Note 1.2} 0: No interrupt requested R/ b7 U0TIF UART0 receive interrupt request flag ^{Note 1.2} 0: No interrupt requested R/ b7 U0TIF UART0 receive interrupt request flag ^{Note 1.2} 0: No interrupt requested R/ Note 1. [Conditions for setting to 0] - - 1: Interrupt requested R/ ·When the corresponding interrupt request locurs - - - - Note 1. [Conditions for setting to 1] - - - - - ·When the corresponding interrupt request locurs - - - - TR/	Bit	Symbol		Bit	Name			Functio	on	R/\
b2 UNRIE UART0 transmit interrupt enable bit 1: Receive interrupt enabled RN b3 U0TIE UART0 transmit interrupt enable bit 1: Transmit interrupt enabled RN b4-b5 - Nothing is assigned. The write value must be 0. The read value is 0. - b6 UORIF UART0 transmit interrupt request flag Note 1.2 0: No interrupt requested RN b7 UOTIF UART0 transmit interrupt request flag Note 1.2 0: No interrupt requested RN b7 UOTIF UART0 transmit interrupt request flag Note 1.2 0: No interrupt requested RN Note 1. [Conditions for setting to 0] ·When the corresponding interrupt request occurs Note 2. The results writing this bit are as follows. - Transmit interrupt request flag Note 1.2 0: Note 1.1 Note 1.1 - - - - - - - - - - - - - Transmit interrupt request flag Note 1.2 0: Note 1.1	b2 UNRLE UART0 transmit interrupt enable bit 1: Receive interrupt enabled P(7) b3 UOTIE UART0 transmit interrupt enable bit 0: Transmit interrupt enabled P(7) b4-b5 - Nothing is assigned. The write value must be 0. The read value is 0. - - b6 UORIF UART0 transmit interrupt request flag Net 12 0: Transmit interrupt requested P(7) b7 UOTIF UART0 transmit interrupt request flag Net 12 0: No interrupt requested P(7) Note 1. [Conditions for setting to 0] ··When the corresponding IR bit changes from 1 to 0 ··When the corresponding interrupt request flag Net 12 0: No interrupt requested P(7) . When 0 is written to this bit after reading it as 1. [Conditions for setting to 1] ··When the corresponding interrupt request occurs P(7) . When the corresponding interrupt request occurs Note 2. The results writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, remains 1 even f0 is written.) · The bit remains unchanged if 1 is written to it. Mdress: 0008Dh (LINIR_0) Bit b7 b6 b5 b4 b3 b2 b1 b0 Symbol - - - - - <t< td=""><td>b0-b1</td><td>-</td><td>Nothing is</td><td>assigned.</td><td>The write</td><td>e value must</td><td>be 0. The re</td><td>ad value is 0</td><td></td><td>-</td></t<>	b0-b1	-	Nothing is	assigned.	The write	e value must	be 0. The re	ad value is 0		-
b3 U0TIE UART0 transmit interrupt enable bit 1: Received interrupt disabled b4-b5 - Nothing is assigned. The write value must be 0. The read value is 0. - b6 UORIF UART0 transmit interrupt request flag Note 1.2 0: No interrupt requested RN b7 U0TIF UART0 transmit interrupt request flag Note 1.2 1: Interrupt requested RN Note 1. [Conditions for setting to 0] ···Vhen the corresponding interrupt request occurs 1: Interrupt requested RN Note 2. The results writing 0 to the same bit is to 0. ··If 0 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, remains 1 even if 0 is written.) ·The bit remains unchanged if 1 is written to it. mer RJ/ LIN Interrupt Request Register (LINIR) Address: 0008Dh (LINIR_0) Bit b7 b6 b5 b4 b3 b2 b1 b0 Symbol - - - - - - TRUE TRUE After Reset X X X X X X 0 0: No interrupt requested RN b0 LINIF Timer RJ/ LIN interrupt request flag Note 1.2 0: No interrupt	b3 U0TIE UART0 transmit interrupt enable bit 1: Receiver literal pit enabled b4-b5 - Nothing is assigned. The write value must be 0. The read value is 0. - b6 U0RIF UART0 transmit interrupt request flag ^{Note 12} 0: No interrupt requested R/ b7 U0TIF UART0 transmit interrupt request flag ^{Note 12} 0: No interrupt requested R/ Note 1. [Conditions for setting to 0] ··When the corresponding interrupt request flag ^{Note 12} 0: No interrupt requested R/ ·When 0 is written to this bit after reading it as 1. [Conditions for setting 0 to the same bit is to 0. ··If 0 is read, writing 0 to the same bit is to 0. ·If 0 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, remains 1 even if 0 is written.) ·The bit remains unchanged if 1 is written to it. Moterrupt request Register (LINIR) Address: 0008Dh (LINIR_0) Bit b5 b4 b3 b2 b1 b0 Symbol - - - - - Transmit interrupt requested R/ b0 LINIF Time RJ/ LIN interrupt request flag ^{Note 12} 0: No interrupt requested R/ b1: b7 - - - -	h2	UORIE	UART0 re	ceive inter	runt enat	ole bit				R/
b3 001ic 0Art0 transmit interrupt enable bit 1: Transmit interrupt enabled RN b4-b5 - Nothing is assigned. The write value must be 0. The read value is 0. - b6 UORIF UART0 transmit interrupt request flag ^{Note 1,2} 0: No interrupt requested RN b7 UOTIF UART0 transmit interrupt request flag ^{Note 1,2} 0: No interrupt requested RN Note 1. [Conditions for setting to 0] ·When the corresponding interrupt request flag ^{Note 1,2} 0: No interrupt requested RN Note 2. The results writing this bit are as follows. ·If 1 is read, writing 0 to the same bit so 0. ·If 1 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, remains 1 even if 0 is written.) ·The request Register (LINIR) Address: 0008Dh (LINIR_0) Bit b7 b6 b5 b4 b3 b2 b1 b0 Symbol - - - - - TRJIF After Reset X X X X X X 0 Bit Symbol Eit Name Function RN b1-b7 - - - -	b3 001ic 0/k10 transmit interrupt enable bit 1: Transmit interrupt enabled k7 b4-b5 - Nothing is assigned. The write value must be 0. The read value is 0. - b6 UORIF UART0 receive interrupt request flag Note 1.2 0: No interrupt requested R7 b7 UOTIF UART0 transmit interrupt request flag Note 1.2 1: Interrupt requested R7 Note 1. [Conditions for setting to 0] ·//when the corresponding IR bit changes from 1 to 0 ·//when the corresponding interrupt request as 1. [Conditions for setting to 1] ·//when the corresponding interrupt request occurs Note 2. The results writing this bit are as follows. ·// f1 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, remains 1 even if 0 is written.) ·// The bit remains unchanged if 1 is written to it. mer RJ/LIN Interrupt Request Register (LINIR) Address: 0008Dh (LINIR_0) b b b b b b b b b b b c r.	52	001112	0,		rapt on ac					
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b6 UORIF UART0 receive interrupt request flag Note 1.2 0: No interrupt requested R/ b7 UOTIF UART0 transmit interrupt request flag Note 1.2 0: No interrupt requested R/ Note 1. [Conditions for setting to 0] •When the corresponding IR bit changes from 1 to 0 •When the corresponding interrupt request occurs Note 2. The results writing this bit are as follows. •If 1 is read, writing 0 to the same bit is to 0. •If 0 is read, writing 0 to the same bit is to 0. ·If 0 is read, writing 0 to the same bit is to 0. •If 0 is read, writing 0 to the same bit is to 0. •If 0 is read, writing 0 to the same bit is to 0. ·If 0 is read, writing 0 to the same bit is to 0. •If 0 is read, writing 0 to the same bit is to 0. •If 0 is read, writing 0 to the same bit is to 0. ·If R/ Example Farmains 1 even if 0 is written.) •The bit remains unchanged if 1 is written to it. Maderss: 0008Dh (LINIR_0) Bit b7 b6 b5 b4 b3 b2 b1 b0 Symbol - - - - - TRJIF After Reset X X X X X 0 Note 1. [Conditions for setting to 0] • •<	b6 UORIF UART0 receive interrupt request flag Note 1.2 0: No interrupt requested R/ b7 UOTIF UART0 transmit interrupt request flag Note 1.2 0: No interrupt requested R/ Note 1. [Conditions for setting to 0] •When the corresponding IR bit changes from 1 to 0 •When the corresponding interrupt request occurs Note 2. The results writing this bit are as follows. •If 1 is read, writing 0 to the same bit is to 0. •If 0 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, remains 1 even if 0 is written.) •The bit remains unchanged if 1 is written to it. Moders: 0008Dh (LINIR_0) Bit b7 b6 b5 b4 b3 b2 b1 b0 Symbol - - - - TR/IF After Reset X X X X 0 R/ b1-b7 Note 1. [Conditions for setting to 0] Bit Name Function R/ Mater RJ/LIN Interrupt Request Register (LINIR) Address: 0008Dh (LINIR_0) Bit Name Interrupt requested R/ b1 b7 b6 b5 b4	h4-h5		Nothing is	assigned	The write	e value must				
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mer RJ/ LIN Interrupt Request Register (LINIR) Address: 0008Dh (LINIR_0) Bit b7 b6 b5 b4 b3 b2 b1 b0 Symbol TRJIF After Reset X X X X X X X X 0 Bit Symbol Bit Name Function R/1 b0 LINIF Timer RJ/ LIN interrupt request flag Note 1.2 0: No interrupt requested b1-b7 - Nothing is assigned. The write value must be 0. The read value is 0 Note 1. [Conditions for setting to 0] · When the corresponding IR bit changes from 1 to 0 · When 0 is written to this bit after reading it as 1. [Conditions for setting to 1] · When the corresponding interrupt request occurs Note 2. The read, writing 0 to the same bit is to 0. · If 0 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, remains 1 even if 0 is written.)	mer RJ/ LIN Interrupt Request Register (LINIR) Address: 0008Dh (LINIR_0) Bit b7 b6 b5 b4 b3 b2 b1 b0 Symbol TRJIF After Reset X X X X X X X X 0 Bit Symbol Bit Name Function R/ b0 LINIF Timer RJ/ LIN interrupt request flag Note 1.2 0: No interrupt requested 1: Interrupt requested R/ b1-b7 - Nothing is assigned. The write value must be 0. The read value is 0 Note 1. [Conditions for setting to 0] · When the corresponding IR bit changes from 1 to 0 · When 0 is written to this bit after reading it as 1. [Conditions for setting to 1] · When the corresponding interrupt request occurs Note 2. The read, writing 0 to the same bit is to 0. · If 0 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, remains 1 even if 0 is written.)										
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• If 0 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, remains 1 even if 0 is written.)	•If 0 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, remains 1 even if 0 is written.)	Bit b0 b1-b7 Note 1. [(Symbol LINIF - Conditions for s •When the corr •When 0 is writ Conditions for s •When the corr	Timer RJ/ Nothing is etting to 0] esponding IF ten to this bir etting to 1] esponding in	Bit N LIN interru assigned. R bit chang t after read	Name upt reque: The write ges from f ding it as quest occ	X st flag ^{Note 1,2} e value must 1 to 0 1.	0: No inter 1: Interrup	X Functio rupt requested t requested	n ed	0
remains 1 even if 0 is written.)	remains 1 even if 0 is written.)	Bit b0 b1-b7 Note 1. [([(Note 2. T	Symbol LINIF - Conditions for s ·When the corr ·When 0 is writ Conditions for s ·When the corr 'he results writir	Timer RJ/ Nothing is etting to 0] esponding IF ten to this bit etting to 1] esponding in ng this bit are	Bit N LIN interru assigned. R bit chang t after read aterrupt red as follows	Name upt reques The write ges from f ding it as quest occ s.	X st flag ^{Note 1,2} e value must 1 to 0 1.	0: No inter 1: Interrup	X Functio rupt requested t requested	n ed	0
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		Bit b0 b1-b7 Note 1. [(Note 2. T	Symbol LINIF - Conditions for s •When the corr •When 0 is writ Conditions for s •When the corr The results writir If 1 is read, writ If 0 is read, writ remains 1 even	Timer RJ/ Nothing is esponding IF ten to this bit etting to 1] esponding ir ng this bit are ing 0 to the s ting 0 to the if 0 is written	Bit N LIN interru assigned. R bit chang t after read aterrupt red as follows same bit is same bit is n.)	Vame upt reque The write ges from ding it as quest occ s. to 0. does not	X st flag ^{Note 1,2} e value must 1 to 0 1. urs	0: No inter 1: Interrup be 0. The re	X Functio rupt requested t requested ad value is 0	n ed	0 R/ R/ -
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		Bit b0 b1-b7 Note 1. [(Note 2. T	Symbol LINIF - Conditions for s •When the corr •When 0 is writ Conditions for s •When the corr The results writir If 1 is read, writ If 0 is read, writ remains 1 even	Timer RJ/ Nothing is esponding IF ten to this bit etting to 1] esponding ir ng this bit are ing 0 to the s ting 0 to the if 0 is written	Bit N LIN interru assigned. R bit chang t after read aterrupt red as follows same bit is same bit is n.)	Vame upt reque The write ges from ding it as quest occ s. to 0. does not	X st flag ^{Note 1,2} e value must 1 to 0 1. urs	0: No inter 1: Interrup be 0. The re	X Functio rupt requested t requested ad value is 0	n ed	0 R/\ R/\ -
		Bit b0 b1-b7 Note 1. [(Note 2. T	Symbol LINIF - Conditions for s •When the corr •When 0 is writ Conditions for s •When the corr The results writir If 1 is read, writ If 0 is read, writ remains 1 even	Timer RJ/ Nothing is esponding IF ten to this bit etting to 1] esponding ir ng this bit are ing 0 to the s ting 0 to the if 0 is written	Bit N LIN interru assigned. R bit chang t after read aterrupt red as follows same bit is same bit is n.)	Vame upt reque The write ges from ding it as quest occ s. to 0. does not	X st flag ^{Note 1,2} e value must 1 to 0 1. urs	0: No inter 1: Interrup be 0. The re	X Functio rupt requested t requested ad value is 0	n ed	0 R/ R/ -
		Bit b0 b1-b7 Note 1. [(Note 2. T	Symbol LINIF - Conditions for s •When the corr •When 0 is writ Conditions for s •When the corr The results writir If 1 is read, writ If 0 is read, writ remains 1 even	Timer RJ/ Nothing is esponding IF ten to this bit etting to 1] esponding ir ng this bit are ing 0 to the s ting 0 to the if 0 is written	Bit N LIN interru assigned. R bit chang t after read aterrupt red as follows same bit is same bit is n.)	Vame upt reque The write ges from ding it as quest occ s. to 0. does not	X st flag ^{Note 1,2} e value must 1 to 0 1. urs	0: No inter 1: Interrup be 0. The re	X Functio rupt requested t requested ad value is 0	n ed	0 R/\ R/\ -
		Bit b0 b1-b7 Note 1. [(Note 2. T	Symbol LINIF - Conditions for s •When the corr •When 0 is writ Conditions for s •When the corr The results writir If 1 is read, writ If 0 is read, writ remains 1 even	Timer RJ/ Nothing is esponding IF ten to this bit etting to 1] esponding ir ng this bit are ing 0 to the s ting 0 to the if 0 is written	Bit N LIN interru assigned. R bit chang t after read aterrupt red as follows same bit is same bit is n.)	Vame upt reque The write ges from ding it as quest occ s. to 0. does not	X st flag ^{Note 1,2} e value must 1 to 0 1. urs	0: No inter 1: Interrup be 0. The re	X Functio rupt requested t requested ad value is 0	n ed	0 R/\ R/\ -
		Bit b0 b1-b7 Note 1. [(Note 2. T	Symbol LINIF - Conditions for s •When the corr •When 0 is writ Conditions for s •When the corr The results writir If 1 is read, writ If 0 is read, writ remains 1 even	Timer RJ/ Nothing is esponding IF ten to this bit etting to 1] esponding ir ng this bit are ing 0 to the s ting 0 to the if 0 is written	Bit N LIN interru assigned. R bit chang t after read aterrupt red as follows same bit is same bit is n.)	Vame upt reque The write ges from ding it as quest occ s. to 0. does not	X st flag ^{Note 1,2} e value must 1 to 0 1. urs	0: No inter 1: Interrup be 0. The re	X Functio rupt requested t requested ad value is 0	n ed	0 R/\ R/\ -



RENESAS TECHNICAL UPDATE TN-R8C-A060A/E

(9) Timer F	RB2 Interrup	t Reque	st Reg	ister (TRBI	R)					
Addre	ess: 00137h	(TRBIR	_0)							
	Bit	b7	· .	b6	b5	b4	b3	b2	b1	b0
	Symbol	TRB	BIE	TRBIF	-	-	-	-	-	-
	After Reset	0		0	0	0	0	0	0	0
Bit	t Syn	nbol		E	Bit Name			Functior	า	R/W
b0-b	- 55		Nothi	ng is assig	ned. The writ	te value musi	t be 0. The re	ad value is 0		-
b6	b6 TRBIF Timer RB2 interrupt request flag 0: No interrupt requested 1: Interrupt requested								R/W	
b7	b7 TRBIE Timer RB2 interrupt enable bit 0: Interrupt disabled R 1: Interrupt enabled 1: Interrupt enabled 1: Interrupt enabled								R/W	
	ge Monitor 1 ess: 00039h Bit)	Register (' b6	VW1C) b5	b4	b3	b2	b1	b0
	Symbol	VW1	C7	-	VW1F1	VW1F0	VW1C3	VW1C2	VW1C1	VW1C0
	After Reset	1		0	0	0	1	0	1	0
Bit	t Sym	nbol			Bit Name			Functio	n	R/W
b0	VW ⁻	1C0	Volta	ge monitor	1 interrupt er	nable bit	0: Disabled 1: Enabled			R/W
b1	VW	1C1	Volta selec	-	1 digital filter	mode	(digital fi 1: Digital fi	Iter enabled r Iter circuit en Iter disabled I Iter circuit dis	abled) mode	R/W
b2	2 VW	1C2	Volta	ge change	detection flag	g		d by passing	through Vdet	.1 R/W
b3	S VW	1C3	Volta	ge detectio	n 1 signal mo	onitor flag	0: VCC < \ 1: VCC ≥ \ circuit di	/det1 or volta	ge detection	1 R
b4	- VW	1F0	0	- 1:	1 4 - :4 -			O divided by O divided by∶		R/W
b5	5 VW	1F1	Sam	oling clock	Seieci DIIS			O divided by O divided by		R/W
b6	; -		Rese	rved			Set to 0.			R/W
b7	, vw	1C7	Volta condi	-	1 interrupt g	eneration		ches Vdet1	or above or below	R/W



(11) \	√oltage Mo	nitor 2 C	ircuit C	ontrol	Register (V	W2C)					
	Address:	0003Ah	(VW2C)							
		Bit	b7	7	b6	b5	b4	b3	b2	b1	b0
		Symbol	VW2	2C7	-	VW2F1	VW2F0	VW2C3	VW2C2	VW2C1	VW2C0
	Afte	r Reset	1		0	0	0	1	0	1	0
	Bit	Sym	bol			Bit Name			Functio	n	R/W
	b0	VW2	2C0	Volta	age monitor	2 interrupt en	able bit	0: Disabled 1: Enabled			R/W
	b1	VW2	2C1		age monitor ct bit	2 digital filter	mode	0: Digital fil (digital fil 1: Digital fil (digital fil	R/W		
	b2	VW2	C2	Volta	age change	detection flag	I	0: Not dete 1: Detected		through Vdet	2 R/W
	b3	VW2	2C3	Volta	age detectio	n 2 signal mo	nitor flag	0: VCC < V 1: VCC ≥ V circuit dis	det2 or volta	ge detection	2 R
	b4	VW2	2F0	0) divided by) divided by :		R/W
	b5	VW2	2F1	Sam	pling clock s	Select dits		10b: fLOCO 11b: fLOCO	R/W		
	b6	-		Res	erved			Set to 0.			R/W
	b7	VW2	2C7	Voltage monitor 2 interrupt generation condition select bit				0: VCC rea 1: VCC rea	R/W		



Audress.	06B12h (TS) Bit	50гк) b7	hG	h <i>E</i>	h1	b 2	b 0	h1	b0
			b6	b5	b4	b3	b2	b1	
	,	SIF	-	-	-	-	MVF	OVFER	DTS
Aner	Reset	0	0	0	0	0	0	0	0
Bit	Symbol		В	lit Name			Function	1	
			Data transfer status flag			[Conditions for	or setting to ()]	
						When data	transfer to R	AM is complete	ed.
						When 1 is written to the TSCUINT bit in the TSCUCR0 register. Note1			1
b0	DTSR	Da							
						[Condition for setting to 1]			
						•When data 1 is captured to the buffer.			
						When the primary counter overflows.			
					[Conditions for setting to 0]				
						When 1 is written to the TSCUINT bit in			I
b1	OVFER	0	Overflow error flag				R0 register. [⊾]		
ы		0,				• When 0 is written by program.			
						[Condition for setting to 1]			
						When the primary counter overflows.			
b2	b2 MVF TSCU operation flag		0: Touch sensor control unit is stopped						
						1: Touch sensor control unit is in operation			on
b6- b3	-	No	Nothing is assigned. The write value mu			ust be 0. The re	ead value is ().	
	7 SIF					[Sources for	• •		
b7					When 1 is written to the TSCUINT bit in			l –	
					the TSCUCR0 register. Note1				
		SIF TSCU interrupt request flag	request flag		• When 0 is written after read. Note2				
				[Sources for setting to 1]					
					When a measurement of the touch sensor			sor	

Note 1. This flag is not set to 0 only by setting the TSCUSTRT bit in the TSCUCR0 register to 0 (measurement stops) Note 2. The results writing this bit are as follows.

 \cdot If 1 is read, writing 0 to the same bit is to 0.

·If 0 is read, writing 0 to the same bit does not change it. (If the bit changes from 0 to 1 after a 0 is read, it remains 1 even if 0 is written.)

·The bit remains unchanged if 1 is written to it.

(13) Interrupt Control Register

Address: 00041H (FMRDYIC), 00046H (INT4IC), 00047H (TRCIC_0), 0004AH (TRE2IC), 0004BH (U2TIC), 0004CH (U2RIC), 0004DH (KUPIC), 0004EH (ADIC), 0004FH (SSUIC_0/ IICIC_0), 00051H (U0TIC_0), 00052H (U0RIC_0), 00053H (U0TIC_1), 00054H (U0RIC_1), 00055H (INT2IC), 00056H (TRJIC_0), 00058H (TRB2IC_0), 00059H (INT1IC), 0005AH (INT3IC), 0005DH (INT0IC), 0005EH (U2BCNIC), 0006BH (TRGIC), 00072H (VCMP1IC), 00073H (VCMP2IC), 00075H (TSCUIC)

	0006BH (TRGIC), 00072H (VCMPTIC), 00073H (VCMP2IC), 00075H (TSCUIC)									
	Bit	b7	b6	b5	b4		b3	b2	b1	b0
Ś	Symbol		-	-	-		IR	ILVL2	ILVL1	ILVL0
Afte	After Reset		0	0	0		0	0	0	0
Bit	Bit Symbol Bit N			lame				Function		R/W
b0	ILVL0							nto un unt dio ole	R/W	
b1	ILVL1	Interr	Interrupt priority level select bits					iterrupt disabled) el 1 to Level 7		R/W
b2	ILVL2					0011	D-IIID. Lev		1	R/W
b3	IR	Interr	Interrupt request bit				o interrupt r terrupt requ	•		R/W Note
b4-b7	b4-b7 - Nothing is assigned. The write value must be 0. The read value is 0.					-				

Note. Only 0 can be written to the IR bit. (Do not write 1 to this bit.) However, a case to use as this measure is excluded. In this case, use the MOV instruction when setting the IR bit in the interrupt control register to "1" as a measure for "caution on using wait mode and stop mode".



3.4 Example of software measures (using wait mode)

Examples of the software measures when using wait mode are shown below.

Example)

Interrupts to exit wait mode: Timer RE2 interrupt (ILVL=1), Periodic interrupt triggered every second enable bit (SEIE=1)

INT0 interrupt (ILVL=6)

The peripheral functions the operations of which are enabled in wait mode: INT1 interrupt (ILVL=0)

	Entering wait mode	Descriptions
BCLR	1, FMR0	CPU rewrite mode disabled
BSET	0, PRCR	Writing to CM3 register enabled
FCLR	I	Interrupt disabled
BSET	0, CM3	Enter wait mode
NOP		
BCLR	0, PRCR	Writing to CM3 register disabled (Protection enabled)
JSR	CHECK_ICU	The check function is called
FSET	I	Interrupt enabled
NOP		NOP instruction

	Check function	Descriptions
CHECK_ICU:		
BTST	1, TREIFR	Judge the RTCF bit
JNC	CHK_ICU001	Branch to the label when RTCF bit is 0
MOV.B	#009H, TRE2IC	Set the IR bit (Countermeasure)
CHK_ICU001:		
BTST	0, INTSTS	Judge the INT0S bit
JNC	CHK_ICU002	Branch to the label when INT0S bit is 0
MOV.B	#00EH, INTOIC	Set the IR bit (Countermeasure)
CHK_ICU002:		
BTST	1, INTSTS	Judge the INT1S bit
JNC	CHK_ICU003	Branch to the label when INT1S bit is 0
MOV.B	#008H, INT1IC	Set the IR bit (Countermeasure)
CHK_ICU003:		
RTS		Return to subroutine



3.5 Example of software measures (using stop mode)

Examples of the software measures when using stop mode are shown below.

Example)

Interrupts to exit wait mode: INT1 interrupt (ILVL=7), INT0 interrupt (ILVL=5)

	Entering stop mode	Descriptions
BCLR	1, FMR0	CPU rewrite mode disabled
BSET	0, PRCR	Writing to CM1 register enabled
FCLR	1	Interrupt disabled
BSET	0, CM1	Enter stop mode (CM10=1)
JMP.B	LABEL_001	Branches to the label
LABEL_001:		
NOP		
BCLR	0, PRCR	Writing to CM1 register disabled (Protection enabled)
JSR	CHECK_ICU	The check function is called
FSET	I	Interrupt enabled
NOP		NOP instruction

	Check function	Descriptions
CHECK_ICU:		
BTST	1, INTSTS	Judge the INT1S bit
JNC	CHK_ICU001	Branch to the label when INT1S bit is 0
MOV.B	#00FH, INT1IC	Set the IR bit (Countermeasure)
CHK_ICU001:		
BTST	0, INTSTS	Judge the INT0S bit
JNC	CHK_ICU002	Branch to the label when INT0S bit is 0
MOV.B	#00DH, INTOIC	Set the IR bit (Countermeasure)
CHK_ICU002:		
RTS		Return to subroutine

