To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	25 May 2000	No.	TN-H8*-171A/E
THEME	Attention on use Timer F		
CLASSIFICATION	☐ Spec. change ■ Limitation on ■ Supplement of Documents		
PRODUCT NAME	H8/3887 series, H8/3847 series, H8/3867 series, H8/3827 series, H8/3847R series, H8/3827R series, H8/3802 series	Lot No. etc. All Lot	
REFERENCE DOCUMENTS	H8/3887 series, H8/3847 series Hardware Manual Rev. 2.0 H8/3867 series, H8/3827 series Hardware Manual Rev. 3.0 H8/3847R series, H8/3827R series, H8/3802 series Hardware Manual Rev. 1.0	Effective Date Eternal From	

We appreciate your selection of Hitachi microcomputers.
We inform you of additional information for Hitachi single chip microcomputer H8/3887/47/67/27/47R/27R series, H8/3802 series Hardware Manual.

<Additional contents>

9.4 Timer F ---(For H8/3887/47 series, in section 9.4 on P 197. For H8/3867/27 series, in section 9.4 on P 194. For H8/3827R series, in section 9.4 on P 193. For H8/3847R series, in section 9.4 on P203. For H8/3802 series, in section 9.3 on P 174)

9.4.5 Application Notes ---(For H8/3887/47 series, in section 9.4.5 on P 214.
For H8/3867/27 series, in section 9.4.5 on P 212.
For H8/3827R series, in section 9.4.5 on P 210.
For H8/3847R series, in section 9.4.5 on P 220.
For H8/3802 series, in section 9.3.5 on P192)

(3) Clear timer FH, timer FL interrupt request flags (IRRTFH, IRRTFL), timer overflow flags H, L (OVFH, OVFL) and compare match flags H, L (CMFH, CMFL)

When ϕ w/4 is selected as the internal clock, “Interrupt factor generation signal” will be operated with ϕ w and the signal will be outputted with ϕ w width.
And, “Overflow signal” and “Compare match signal” are controlled with 2 cycles of ϕ w signals.
Those signals are outputted with 2 cycles width of ϕ w. (Figure1)
In active (high-speed, medium-speed) mode, even if you cleared interrupt request flag during the term of validity of “Interrupt factor generation signal” , same interrupt request flag is set. (Figure 1-1).
And, you cannot be cleared timer overflow flag and compare match flag during the term of validity of “Overflow signal” and “Compare match signal”.

For interrupt request flag is set right after interrupt request is cleared, interrupt process to one time timer FH, timer FL interrupt might be repeated. (Figure1-2)
Therefore, to definitely clear interrupt request flag in active (high-speed, medium-speed) mode, clear should be processed after the time that calculated with below (1) formula. And, to definitely clear timer overflow flag and compare match flag, clear should be processed after read timer control status register F(TCSRF) after the time that calculated with below (1) formula.
For ST of (1) formula, please substitute the longest number of execution states in used instruction.
(10 states of RTE instruction when MULXU, DIVXU instruction is not used, 14 states when MULXU, DIVXU instruction is used)
In subactive mode, there are no limitation for interrupt request flag, timer overflow flag, and compare match flag clear.

The term of validity of “Interrupt factor generation signal”
=1 cycle of ϕ w + waiting time for completion of executing instruction + interrupt time synchronized with ϕ
$=1/\phi$ w $+ST\times(1/\phi)+(2/\phi)$ (second)·····(1)

ST: Executing number of execution states

Method 1 is recommended to operate for time efficiency.

(Method1)
1.Prohibit interrupt in interrupt handling routine (set IENFH, IENFL to "0").
2.After program process returned normal handling, clear interrupt request flags (IRRTFH, IRRTFL) after more than time that calculated with (1) formula.
3.After read timer control status register F (TCSRF), clear timer overflow flags (OVFH, OVFL) and compare match flags (CMFH, CMFL).
4.Operate interrupt permission (set IENFH, IENFL to “1”).

(Method2)
1.Set interrupt handling routine time to more than time that calculated with (1) formula.
2.Clear interrupt request flags (IRRTFH, IRRTFL) at the end of interrupt handling routine.
3.After read timer control status register F (TCSRF), clear timer overflow flags (OVFH, OVFL) and compare match flags (CMFH, CMFL).

All above attentions are also applied in 16bit mode and 8bit mode.

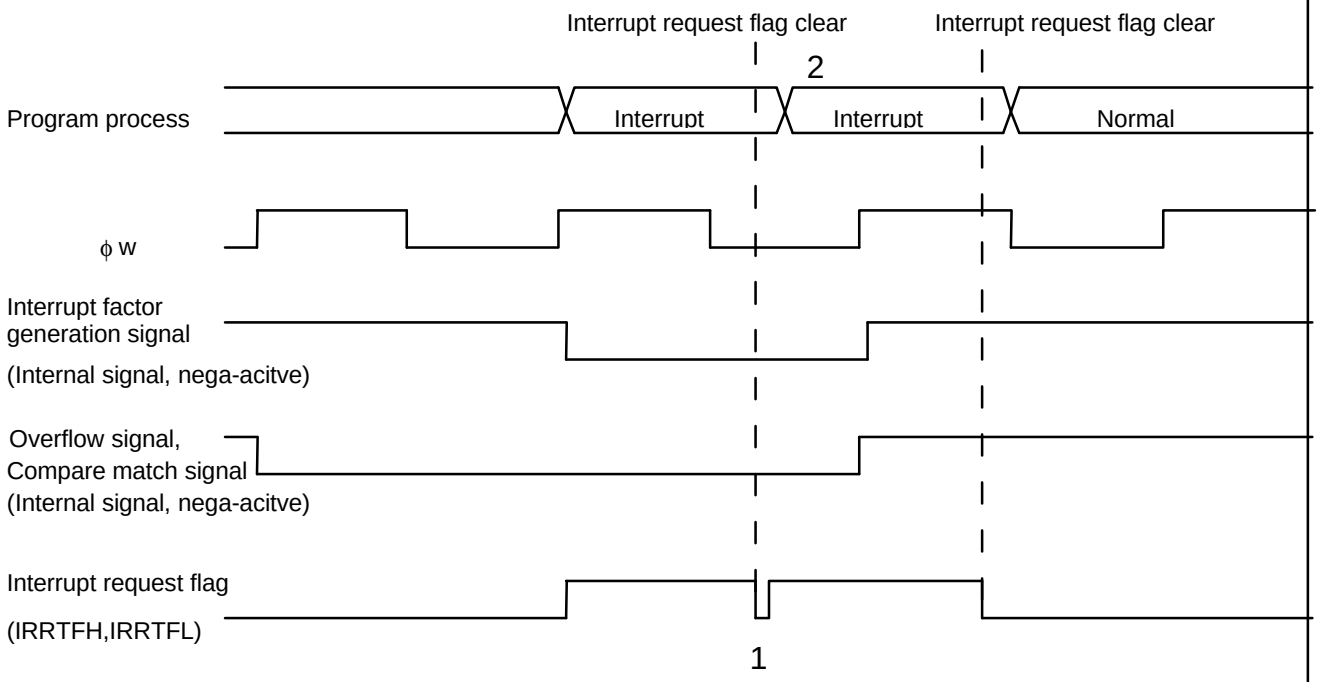

Figure 1 Clear interrupt request flag when interrupt factor generation signal is valid

(4) Timer counter (TCF) read/write

When ϕ w/4 is selected as the internal clock in active(high-speed, medium-speed) mode, write on TCF is impossible. And, when read TCF, as the system clock and internal clock are mutually asynchronous, TCF synchronizes with synchronization circuit.

This results in a maximum TCF read value error of ±1.

When read/write TCF in active(high-speed, medium-speed) mode is needed, please select internal clock except for ϕ w/4 before read/write.

In subactive mode, even ϕ w/4 is selected as the internal clock, normal read/write TCF is possible.

HITACHI SEMICONDUCTOR TECHNICAL

DATE	14 September 2000	No.	TN-H8*-186A/E
THEME	DC characteristics of the port 9		
CLASSIFICATION	■ Spec. change ■ Supplement of Documents	☐ Limitation on Use	
PRODUCT NAME	HD6473802,HD6433802,HD6433801,HD6433800	Lot No.etc.	All lots
REFERENCE DOCUMENTS	H8/3802 Series Hardware Manual (ADE-602-203)	Effective Date From	Eternal Now

The DC characteristics of the port 9 are changed in Hitachi single chip microcomputer H8/3802 series hardware manual. We want it understood and approved.

Section 14 Electrical Characteristics

14.2 H8/3802 Series Electrical Characteristics

14.2.2 DC Characteristics

Table 14.2 DC Characteristics • • • (P312)

(Incorrect)

			Values					
Item	**Symbol**	**Applicable Pins**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**	**Notes**
Output low voltage	V_{OL}	$P9_0$ to $P9_2$	—	—	0.5	_	I_{OL}=25mA	_
		$P9_3$ to $P9_5$	—	—	0.5	_	I_{OL}=10mA	

(Correct)

			Values					
Item	**Symbol**	**Applicable Pins**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**	**Notes**
Output low voltage	V_{OL}	$P9_0$ to $P9_2$	—	—	0.5	V	V_{CC}=2.2 to 5.5V I_{OL}=25mA I_{OL}=15mA	*5
		$P9_3$ to $P9_5$	—	—	0.5	V	I_{OL}=10mA	

HITACHI SEMICONDUCTOR TECHNICAL

DATE	14 September 2000	No.	TN-H8*-187A/E
THEME	Error Correction of H8/3802 Series Hardware Manual		
CLASSIFICATION	☐ Spec. change ☐ Limitation on Use ■ Supplement of Documents		
PRODUCT NAME	HD6473802,HD6433802,HD6433801,HD6433800	Lot No.etc.	All lots
REFERENCE DOCUMENTS	H8/3802 Series Hardware Manual (ADE-602-203)	Effective Date From	Eternal Now

The error corrections in Hitachi single chip microcomputer H8/3802 series hardware manual are given below. We want it understood and approved.

Section 3 Exception Handling
3.3 Interrupts
3.3.2 Interrupt Control Registers
Table 3.3 Interrupt Control Registers ·····(P61)

(Incorrect)

Name	Abbrev.	R/W	Initial Value	Address
IRQ edge select register	IEGR	R/W	H'FC	H'FFF2
Interrupt enable register 1	IENR1	R/W	H'58	H'FFF3
Interrupt enable register 2	IENR2	R/W	H'32	H'FFF4
Interrupt request register 1	IRR1	R/W*	H'78	H'FFF6
Interrupt request register 2	IRR2	R/W*	H'32	H'FFF7
Wakeup interrupt request register	IWPR	R/W*	H'00	H'FFF9
Wakeup edge select register	WEGR	R/W	H'00	H'FF90

(Correct)

Name	Abbrev.	R/W	Initial Value	Address
IRQ edge select register	IEGR	R/W	—	H'FFF2
Interrupt enable register 1	IENR1	R/W	—	H'FFF3
Interrupt enable register 2	IENR2	R/W	—	H'FFF4
Interrupt request register 1	IRR1	R/W*	—	H'FFF6
Interrupt request register 2	IRR2	R/W*	—	H'FFF7
Wakeup interrupt request register	IWPR	R/W*	H'00	H'FFF9
Wakeup edge select register	WEGR	R/W	H'00	H'FF90

Section 3 Exception Handling
3.3 Interrupts
3.3.2 Interrupt Control Registers
1. IRQ edge select register (IEGR) ·····(P61)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IEG1	IEG0
Initial value	1	1	1	1	1	1	0	0
Read/Write	—	—	—	—	—	—	R/W	R/W

IEGR is an 8-bit read/write register used to designate whether pins $\overline{IRQ_1}$ and $\overline{IRQ_0}$ are set to rising edge sensing or falling edge sensing.

Bits 7 to 2: Reserved bits

Bits 7 to 2 are reserved; they are always read as 1 and cannot be modified.

(Correct)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IEG1	IEG0
Initial value	1	1	1	—	—	—	0	0
Read/Write	—	—	—	—	—	—	R/W	R/W

IEGR is an 8-bit read/write register used to designate whether pins $\overline{IRQ_1}$ and $\overline{IRQ_0}$ are set to rising edge sensing or falling edge sensing.

Bits 7 to 5: Reserved bits

Bits 7 to 5 are reserved; they are always read as 1 and cannot be modified.

Bits 4 to 2: Reserved bits

Bits 4 to 2 are reserved bits.

Section 3 Exception Handling
3.3 Interrupts
3.3.2 Interrupt Control Registers
2. Interrupt enable register 1 (IENR1) ·····(P62 to P63)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	IENTA	—	IENWP	—	—	IENEC2	IEN1	IEN0
Initial value	0	1	0	1	1	0	0	0
Read/Write	R/W	—	R/W	—	—	R/W	R/W	R/W

Bit 6: Reserved bit

Bit 6 is reserved; it is always read as 1 and cannot be modified.

Bits 4 and 3: Reserved bits

Bits 4 and 3 are reserved; they are always read as 1 and cannot be modified.

(Correct)

Bit	7	6	5	4	3	2	1	0
	IENTA	—	IENWP	—	—	IENEC2	IEN1	IEN0
Initial value	0	—	0	—	—	0	0	0
Read/Write	R/W	—	R/W	—	—	R/W	R/W	R/W

Bit 6: Reserved bit

Bit 6 is reserved bit.

Bits 4 and 3: Reserved bits

Bits 4 and 3 are reserved bits.

Section 3 Exception Handling
3.3 Interrupts
3.3.2 Interrupt Control Registers
3. Interrupt enable register 2 (IENR2) ·····(P63 to P64)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	IENDT	IENAD	—	—	IENTFH	IENTFL	—	IENEC
Initial value	0	0	1	1	0	0	1	0
Read/Write	R/W	R/W	—	—	R/W	R/W	—	R/W

Bits 5 and 4: Reserved bits

Bits 5 and 4 are reserved bits; they are always read as 1 and cannot be modified.

Bit 1: Reserved bit

Bit 1 is reserved; it is always read as 1 and cannot be modified.

(Correct)

Bit	7	6	5	4	3	2	1	0
	IENDT	IENAD	—	—	IENTFH	IENTFL	—	IENEC
Initial value	0	0	—	—	0	0	—	0
Read/Write	R/W	R/W	W	W	R/W	R/W	W	R/W

Bits 5 and 4: Reserved bits

Bits 5 and 4 are reserved; only a write of 0 is possible.

Bit 1: Reserved bit

Bit 1 is reserved; only a write of 0 is possible.

Section 3 Exception Handling
3.3 Interrupts
3.3.2 Interrupt Control Registers
4. Interrupt request register 1 (IRR1) ·····(P65)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	IRRTA	—	—	—	—	IRREC2	IRRI1	IRRI0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W*	—	—	—	—	R/W*	R/W*	R/W*

Bits 6 to 3: Reserved bits

Bits 6 to 3 are reserved; they are always read as 1 and cannot be modified.

(Correct)

Bit	7	6	5	4	3	2	1	0
	IRRTA	—	—	—	—	IRREC2	IRRI1	IRRI0
Initial value	0	—	1	—	—	0	0	0
Read/Write	R/W*	—	—	—	—	R/W*	R/W*	R/W*

Bits 6 and 4,3: Reserved bits

Bits 6 and 4,3 are reserved bits.

Bit 5: Reserved bit

Bit 5 is reserved; it is always read as 1 and cannot be modified.

Section 3 Exception Handling
3.3 Interrupts
3.3.2 Interrupt Control Registers
5. Interrupt request register 2 (IRR2) ·····(P67, P68)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	IRRDT	IRRAD	—	—	IRRTFH	IRRTFL	—	IRREC
Initial value	0	0	1	1	0	0	1	0
Read/Write	R/W*	R/W*	—	—	R/W*	R/W*	—	R/W*

Bits 5 and 4: Reserved bits

Bits 5 and 4 are reserved; they are always read as 1 and cannot be modified.

Bit 1: Reserved bit

Bit 1 is reserved; it is always read as 1 and cannot be modified.

(Correct)

Bit	7	6	5	4	3	2	1	0
	IRRDT	IRRAD	—	—	IRRTFH	IRRTFL	—	IRREC
Initial value	0	0	—	—	0	0	—	0
Read/Write	R/W*	R/W*	W	W	R/W*	R/W*	W	R/W*

Bits 5 and 4: Reserved bits

Bits 5 and 4 are reserved; only a write of 0 is possible.

Bit 1: Reserved bit

Bit 1 is reserved; only a write of 0 is possible.

Section 8 I/O Ports
8.2 Port 3
8.2.2 Register Configuration and Description
Table 8.2 Port 3 Registers ·····(P129)

(Incorrect)

Name	Abbrev.	R/W	Initial Value	Address
Port data register 3	PDR3	R/W	H'01	H'FFD6
Port control register 3	PCR3	W	H'01	H'FFE6
Port pull-up control register 3	PUCR3	R/W	H'01	H'FFE1
Port mode register 3	PMR3	R/W	H'39	H'FFCA

(Correct)

Name	Abbrev.	R/W	Initial Value	Address
Port data register 3	PDR3	R/W	—	H'FFD6
Port control register 3	PCR3	W	—	H'FFE6
Port pull-up control register 3	PUCR3	R/W	—	H'FFE1
Port mode register 3	PMR3	R/W	—	H'FFCA

Section 8 I/O Ports
8.2 Port 3
8.2.2 Register Configuration and Description
1. Port data register 3 (PDR3) ·····(P130)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	P37	P36	P35	P34	P33	P32	P31	—
Initial value	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

PDR3 is an 8-bit register that stores data for port 3 pins P37 to P31. If port 3 is read while PCR3 bits are set to 1, the values stored in PDR3 are read, regardless of the actual pin states. If port 3 is read while PCR3 bits are cleared to 0, the pin states are read.
Upon reset, PDR3 is initialized to H'01.

(Correct)

Bit	7	6	5	4	3	2	1	0
	P37	P36	P35	P34	P33	P32	P31	—
Initial value	0	0	0	0	0	0	0	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

PDR3 is an 8-bit register that stores data for port 3 pins P37 to P31. If port 3 is read while PCR3 bits are set to 1, the values stored in PDR3 are read, regardless of the actual pin states. If port 3 is read while PCR3 bits are cleared to 0, the pin states are read.

Section 8 I/O Ports
8.2 Port 3
8.2.2 Register Configuration and Description
2. Port control register 3 (PCR3) ·····(P130)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	PCR37	PCR36	PCR35	PCR34	PCR33	PCR32	PCR31	—
Initial value	0	0	0	0	0	0	0	1
Read/Write	W	W	W	W	W	W	W	—

PCR3 is an 8-bit register for controlling whether each of the port 3 pins P37 to P31 functions as an input pin or output pin. Setting a PCR3 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR3 and in PDR3 are valid only when the corresponding pin is designated in PMR3 as a general I/O pin.

Upon reset, PCR3 is initialized to H'01.

PCR3 is a write-only register, which is always read as all 1s.

(Correct)

Bit	7	6	5	4	3	2	1	0
	PCR37	PCR36	PCR35	PCR34	PCR33	PCR32	PCR31	—
Initial value	0	0	0	0	0	0	0	—
Read/Write	W	W	W	W	W	W	W	W

PCR3 is an 8-bit register for controlling whether each of the port 3 pins P37 to P31 functions as an input pin or output pin. Setting a PCR3 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR3 and in PDR3 are valid only when the corresponding pin is designated in PMR3 as a general I/O pin.

PCR3 is a write-only register, and the bits 7 to 1 are read as all 1s.

Bit 0 is reserved; only a write of 0 is possible.

Section 8 I/O Ports
8.2 Port 3
8.2.2 Register Configuration and Description
3, Port pull-up control register 3 (PUCR3) ·····(P130)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	PUCR37	PUCR36	PUCR35	PUCR34	PUCR33	PUCR32	PUCR31	—
Initial value	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

PUCR3 controls whether the MOS pull-up of the port 3 pins P37 to P31 is on or off. When a PCR3 bit is cleared to 0, setting the corresponding PUCR3 bit to 1 turns on the MOS pull-up for the corresponding pin, while clearing the bit to 0 turns off the MOS pull-up.

Upon reset, PUCR3 is initialized to H'01.

(Correct)

Bit	7	6	5	4	3	2	1	0
	PUCR37	PUCR36	PUCR35	PUCR34	PUCR33	PUCR32	PUCR31	—
Initial value	0	0	0	0	0	0	0	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W

PUCR3 controls whether the MOS pull-up of the port 3 pins P37 to P31 is on or off. When a PCR3 bit is cleared to 0, setting the corresponding PUCR3 bit to 1 turns on the MOS pull-up for the corresponding pin, while clearing the bit to 0 turns off the MOS pull-up.

Bit 0 is reserved; only a write of 0 is possible.

Section 8 I/O Ports
8.2 Port 3
8.2.2 Register Configuration and Description
4. Port mode register 3 (PMR3) ·····(P131, P132)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	AEVL	AEVH	—	—	—	TMOFH	TMOFL	—
Initial value	0	0	1	1	1	0	0	1
Read/Write	R/W	R/W	—	—	—	R/W	R/W	—

PMR3 is an 8-bit read/write register, controlling the selection of pin functions for port 3 pins.

Upon reset, PMR3 is initialized to H'39.

Bits 5 to 3: Reserved bits

These bits are reserved; they are always read as 1 and cannot be modified.

Bit 0: Reserved bit

This bit is reserved; it is always read as 1 and cannot be modified.

(Correct)

Bit	7	6	5	4	3	2	1	0
	AEVL	AEVH	—	—	—	TMOFH	TMOFL	—
Initial value	0	0	—	—	—	0	0	—
Read/Write	R/W	R/W	W	W	W	R/W	R/W	W

PMR3 is an 8-bit read/write register, controlling the selection of pin functions for port 3 pins.

Bits 5 to 3: Reserved bits

These bits are reserved; only a write of 0 is possible.

Bit 0: Reserved bit

This bit is reserved; only a write of 0 is possible.

Section 8 I/O Ports
8.3 Port 4
8.3.2 Register Configuration and Description
Table 8.5 Port 4 Registers ·····(P135)

(Incorrect)

Name	Abbrev.	R/W	Initial Value	Address
Port data register 4	PDR4	R/W	H'F8	H'FFD7
Port control register 4	PCR4	W	H'F8	H'FFE7
Port mode register 2	PMR2	R/W	H'DE	H'FFC9

(Correct)

Name	Abbrev.	R/W	Initial Value	Address
Port data register 4	PDR4	R/W	H'F8	H'FFD7
Port control register 4	PCR4	W	H'F8	H'FFE7
Port mode register 2	PMR2	R/W	—	H'FFC9

Section 8 I/O Ports
8.3 Port 4
8.3.2 Register Configuration and Description
3. Port mode register 2 (PMR2) ·····(P136)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	—	—	POF1	—	—	—	—	IRQ0
Initial value	1	1	0	1	1	1	1	0
Read/Write	—	—	R/W	—	—	—	—	R/W

PMR2 is an 8-bit read/write register controlling the selection of the P43/IRQ0 pin function and the PMOS on/off state for the P35/SO1 pin. Upon reset, PMR2 is initialized to H'DE.

Bits 7, 6, and 4 to 1: Reserved bits

Bits 7, 6, and 4 to 1 are reserved; they are always read as 1 and cannot be modified.

(Correct)

Bit	7	6	5	4	3	2	1	0
	—	—	POF1	—	—	—	—	IRQ0
Initial value	1	1	0	1	1	—	—	0
Read/Write	—	—	R/W	—	—	W	W	R/W

PMR2 is an 8-bit read/write register controlling the selection of the P43/IRQ0 pin function and the PMOS on/off state for the P35 pin.

Bits 7, 6, and 4, 3: Reserved bits

Bits 7, 6, and 4, 3 are reserved; they are always read as 1 and cannot be modified.

Bits 2, 1: Reserved bits

These bits are reserved; only a write of 0 is possible.

Section 8 I/O Ports
8.7 Port 8
8.7.2 Register Configuration and Description
Table 8.17 Port 8 Registers ·····(P151)

(Incorrect)

Name	Abbrev.	R/W	Initial Value	Address
Port data register 8	PDR8	R/W	H'FE	H'FFDB
Port control register 8	PCR8	W	H'FE	H'FFEB

(Correct)

Name	Abbrev.	R/W	Initial Value	Address
Port data register 8	PDR8	R/W	—	H'FFDB
Port control register 8	PCR8	W	—	H'FFEB

Section 8 I/O Ports
8.7 Port 8
8.7.2 Register Configuration and Description
1. Port data register 8 (PDR8) ·····(P152)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	P80
Initial value	1	1	1	1	1	1	1	0
Read/Write	—	—	—	—	—	—	—	R/W

PDR8 is an 8-bit register that stores data for port 8 pin P80. If port 8 is read while PCR8 bits are set to 1, the values stored in PDR8 are read, regardless of the actual pin states. If port 8 is read while PCR8 bits are cleared to 0, the pin states are read.

Upon reset, PDR8 is initialized to H'FE.

(Correct)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	P80
Initial value	—	—	—	—	—	—	—	0
Read/Write	—	—	—	—	—	—	—	R/W

PDR8 is an 8-bit register that stores data for port 8 pin P80. If port 8 is read while PCR8 bits are set to 1, the values stored in PDR8 are read, regardless of the actual pin states. If port 8 is read while PCR8 bits are cleared to 0, the pin states are read.

Section 8 I/O Ports
8.7 Port 8
8.7.2 Register Configuration and Description
2. Port control register 8 (PCR8) ·····(P152)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PCR80
Initial value	1	1	1	1	1	1	1	0
Read/Write	—	—	—	—	—	—	—	W

PCR8 is an 8-bit register for controlling whether the port 8 pin P80 functions as an input or output pin. Setting a PCR8 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. PCR8 and PDR8 settings are valid when the corresponding pins are designated for general-purpose input/output by bits SGS3 to SGS0 in LPCR.

Upon reset, PCR8 is initialized to H'FE.

PCR8 is a write-only register, which is always read as all 1s.

(Correct)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PCR80
Initial value	—	—	—	—	—	—	—	0
Read/Write	W	W	W	W	W	W	W	W

PCR8 is an 8-bit register for controlling whether the port 8 pin P80 functions as an input or output pin. Setting a PCR8 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. PCR8 and PDR8 settings are valid when the corresponding pins are designated for general-purpose input/output by bits SGS3 to SGS0 in LPCR.

PCR8 is a write-only register, and the bit 0 is read as 1.

Bits 7 to 1 are reserved; only a write of 0 is possible.

Section 8 I/O Ports
8.8 Port 9
8.8.2 Register Configuration and Description
Table 8.20 Port 9 Registers ·····(P154)

(Incorrect)

Name	Abbrev.	R/W	Initial Value	Address
Port data register 9	PDR9	R/W	H'FF	H'FFDC
Port mode register 9	PMR9	R/W	H'F4	H'FFEC

(Correct)

Name	Abbrev.	R/W	Initial Value	Address
Port data register 9	PDR9	R/W	H'FF	H'FFDC
Port mode register 9	PMR9	R/W	—	H'FFEC

Section 8 I/O Ports
8.8 Port 9
8.8.2 Register Configuration and Description
2. Port mode register 9 (PMR9) ·····(P155)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PIOFF	—	PWM2	PWM1
Initial value	1	1	1	1	0	1	0	0
Read/Write	—	—	—	—	R/W	—	R/W	R/W

PMR9 is an 8-bit read/write register controlling the selection of the P90 and P91 pin functions.

(Correct)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PIOFF	—	PWM2	PWM1
Initial value	1	1	1	1	0	—	0	0
Read/Write	—	—	—	—	R/W	W	R/W	R/W

PMR9 is an 8-bit read/write register controlling the selection of the $P9_0$ and $P9_2$ pin functions.

Bit 2: Reserved bit

This bit is reserved; only a write of 0 is possible.

Section 8 I/O Ports
8.11 Input/Output Data Inversion Function
8.11.2 Register Configuration and Description
Table 8.28 Register Configuration ·····(P164, P165)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	—	—	SPC32	—	SCINV3	SCINV2	—	—
Initial value	1	1	0	1	0	0	1	1
Read/Write	—	—	R/W	—	R/W	R/W	—	—

SPCR is an 8-bit readable/writable register that performs RXD_{32} and TXD_{32} pin input/output data inversion switching. SPCR is initialized to H'D3 by a reset.

Bit 4: Reserved bit

Bit 4 is reserved; this is always read as 1 and cannot be modified.

Bits 1 and 0: Reserved bits

Bits 1 and 0 are reserved; they are always read as 1 and cannot be modified.

(Correct)

Bit	7	6	5	4	3	2	1	0
	—	—	SPC32	—	SCINV3	SCINV2	—	—
Initial value	1	1	0	—	0	0	—	—
Read/Write	—	—	R/W	W	R/W	R/W	W	W

SPCR is an 8-bit readable/writable register that performs RXD_{32} and TXD_{32} pin input/output data inversion switching.

Bit 4: Reserved bit

Bit 4 is reserved; only a write of 0 is possible.

Bits 1 and 0: Reserved bits

Bits 1 and 0 are reserved; only a write of 0 is possible.

Section 9 Timers
9.2 Timer A
9.2.1 Overview
3. Register configuration
Table 9.2 Timer A Registers ·····(P170)

(Incorrect)

Name	Abbrev.	R/W	Initial Value	Address
Timer mode register A	TMA	R/W	H'F0	H'FFB0
Timer counter A	TCA	R	H'00	H'FFB1
Clock stop register 1	CKSTPR1	R/W	H'FF	H'FFFA

(Correct)

Name	Abbrev.	R/W	Initial Value	Address
Timer mode register A	TMA	R/W	—	H'FFB0
Timer counter A	TCA	R	H'00	H'FFB1
Clock stop register 1	CKSTPR1	R/W	H'FF	H'FFFA

Section 9 Timers
9.2 Timer A
9.2.2 Register Descriptions
1. Timer mode register A (TMA) ·····(P170)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	TMA3	TMA2	TMA1	TMA0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

TMA is an 8-bit read/write register for selecting the prescaler, and input clock.

Upon reset, TMA is initialized to H'F0.

Bits 7 to 4: Reserved bits

Bits 7 to 4 are reserved; they are always read as 1 and cannot be modified.

(Correct)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	TMA3	TMA2	TMA1	TMA0
Initial value	—	—	—	1	0	0	0	0
Read/Write	W	W	W	—	R/W	R/W	R/W	R/W

TMA is an 8-bit read/write register for selecting the prescaler, and input clock.

Bits 7 to 5: Reserved bits

Bits 7 to 5 are reserved; only a write of 0 is possible.

Bit 4: Reserved bit

Bit 4 is reserved; this is always read as 1 and cannot be modified.

Section 10 Serial Communication Interface
10.1 Overview
10.1.4 Register configuration
Table 10.2 Registers ·····(P214)

(Incorrect)

Name	Abbrev.	R/W	Initial Value	Address
Serial mode register	SMR	R/W	H'00	H'FFA8
Bit rate register	BRR	R/W	H'FF	H'FFA9
Serial control register 3	SCR3	R/W	H'00	H'FFAA
Transmit data register	TDR	R/W	H'FF	H'FFAB
Serial status register	SSR	R/W	H'84	H'FFAC
Receive data register	RDR	R	H'00	H'FFAD
Transmit shift register	TSR	Protected	—	—
Receive shift register	RSR	Protected	—	—
Bit rate counter	BRC	Protected	—	—
Clock stop register 1	CKSTPR1	R/W	H'FF	H'FFFA
Serial port control register	SPCR	R/W	H'C0	H'FF91

(Correct)

Name	Abbrev.	R/W	Initial Value	Address
Serial mode register	SMR	R/W	H'00	H'FFA8
Bit rate register	BRR	R/W	H'FF	H'FFA9
Serial control register 3	SCR3	R/W	H'00	H'FFAA
Transmit data register	TDR	R/W	H'FF	H'FFAB
Serial status register	SSR	R/W	H'84	H'FFAC
Receive data register	RDR	R	H'00	H'FFAD
Transmit shift register	TSR	Protected	—	—
Receive shift register	RSR	Protected	—	—
Bit rate counter	BRC	Protected	—	—
Clock stop register 1	CKSTPR1	R/W	H'FF	H'FFFA
Serial port control register	SPCR	R/W	—	H'FF91

Section 10 Serial Communication Interface
10.1 Overview
10.1.4 Register configuration
Table 10.2 Registers ·····(P235)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	—	—	SPC32	—	SCINV3	SCINV2	—	—
Initial value	1	1	0	1	0	0	1	1
Read/Write	—	—	R/W	—	R/W	R/W	—	—

SPCR is an 8-bit readable/writable register that performs RXD32 and TXD32 pin input/output data inversion switching. SPCR is initialized to H'D3 by a reset.

Bits 7, 6, 4, 1, and 0: Reserved bits

Bits 7 and 6 are reserved; they are always read as 1 and cannot be modified.

(Correct)

Bit	7	6	5	4	3	2	1	0
	—	—	SPC32	—	SCINV3	SCINV2	—	—
Initial value	1	1	0	—	0	0	—	—
Read/Write	—	—	R/W	W	R/W	R/W	W	W

SPCR is an 8-bit readable/writable register that performs RXD_{32} and TXD_{32} pin input/output data inversion switching.

Bits 7 and 6: Reserved bits

Bits 7 and 6 are reserved; they are always read as 1 and cannot be modified.

Bits 4, 1, and 0: Reserved bits

Bits 4, 1, and 0 are reserved; only a write of 0 is possible.

Section 12 A/D Converter
12.2 Register Descriptions
12.2.2 A/D Mode Register (AMR) ·····(P280, P281)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	CKS	—	—	—	CH3	CH2	CH1	CH0
Initial value	0	0	1	1	0	0	0	0
Read/Write	R/W	—	—	—	R/W	R/W	R/W	R/W

AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins.
Upon reset, AMR is initialized to H'30.

Bit 6: Reserved bit

Bit 6 is a readable/writeable reserved bit, but should not be modified as this may cause erroneous operation.

(Correct)

Bit	7	6	5	4	3	2	1	0
	CKS	—	—	—	CH3	CH2	CH1	CH0
Initial value	0	0	1	1	0	0	0	0
Read/Write	R/W	R/W	—	—	R/W	R/W	R/W	R/W

AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins.
Upon reset, AMR is initialized to H'30.

Bit 6: Reserved bit

This bit is reserved; do not set this bit to 1.

Section 13 LCD Controller/Driver
13.2 Register Descriptions
13.2.1 LCD Port Control Register (LPCR) ·····(P292)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	DTS1	DTS0	CMX	—	SGS3	SGS2	SGS1	SGS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	—	R/W	R/W	R/W	R/W

Bit 4: Reserved bit

Bit 4 is a readable/writable reserved bit. It is initialized to 0 by a reset.

(Correct)

Bit	7	6	5	4	3	2	1	0
	DTS1	DTS0	CMX	—	SGS3	SGS2	SGS1	SGS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 4: Reserved bit

This bit is reserved; do not set this bit to 1.

Section 13 LCD Controller/Driver
13.2 Register Descriptions
13.2.3 LCD Control Register 2 (LCR2) ..... (P296)

(Incorrect)

Bit	7	6	5	4	3	2	1	0
	LCDAB	—	—	—	—	—	—	—
Initial value	0	1	1	0	0	0	0	0
Read/Write	R/W	—	—	—	—	—	—	—

Bits 4 to 0: Reserved bits

Bits 4 to 0 are reserved; they can be read and written, and are initialized to 0 upon reset.

(Correct)

Bit	7	6	5	4	3	2	1	0
	LCDAB	—	—	—	—	—	—	—
Initial value	0	1	1	0	0	0	0	0
Read/Write	R/W	—	—	R/W	R/W	R/W	R/W	R/W

Bits 4 to 0: Reserved bits

Bit 4 to 0 is reserved; do not set these bits to 1.

Appendix B Internal I/O Registers
B.2 Functions
SPCR ·····(P348)

(Incorrect)

SPCR-Serial Port Control Register H'91 SCI

Bit	7	6	5	4	3	2	1	0
	—	—	SPC32	—	SCINV3	SCINV2	—	—
Initial value	1	1	0	1	0	0	1	1
Read/Write	—	—	R/W	—	R/W	R/W	—	—

(Correct)

SPCR-Serial Port Control Register H'91 SCI

Bit	7	6	5	4	3	2	1	0
	—	—	SPC32	—	SCINV3	SCINV2	—	—
Initial value	1	1	0	—	0	0	—	—
Read/Write	—	—	R/W	W	R/W	R/W	W	W

Appendix B Internal I/O Registers
B.2 Functions
TMA ·····(P358)

(Incorrect)

TMA-Timer mode register A H'B0 Timer A

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	TMA3	TMA2	TMA1	TMA0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

(Correct)

TMA-Timer mode register A H'B0 Timer A

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	TMA3	TMA2	TMA1	TMA0
Initial value	—	—	—	1	0	0	0	0
Read/Write	W	W	W	—	R/W	R/W	R/W	R/W

Appendix B Internal I/O Registers
B.2 Functions
LPCR ·····(P363)

(Incorrect)

LPCR-LCD port control register H'C0 LCD controller/driver

Bit	7	6	5	4	3	2	1	0
	DTS1	DTS0	CMX	—	SGS3	SGS2	SGS1	SGS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	—	R/W	R/W	R/W	R/W

(Correct)

LPCR-LCD port control register H'C0 LCD controller/driver

Bit	7	6	5	4	3	2	1	0
	DTS1	DTS0	CMX	—	SGS3	SGS2	SGS1	SGS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Appendix B Internal I/O Registers
B.2 Functions
LCR2 ·····(P365)

(Incorrect)

LCR2-LCD control register 2 H'C2 LCD

Bit	7	6	5	4	3	2	1	0
	LCDAB	—	—	—	—	—	—	—
Initial value	0	1	1	0	0	0	0	0
Read/Write	R/W	—	—	—	—	—	—	—

(Correct)

LCR2-LCD control register 2 H'C2 LCD controller/driver

Bit	7	6	5	4	3	2	1	0
	LCDAB	—	—	—	—	—	—	—
Initial value	0	1	1	0	0	0	0	0
Read/Write	R/W	—	—	R/W	R/W	R/W	R/W	R/W

Appendix B Internal I/O Registers
B.2 Functions
AMR ·····(P366)

(Incorrect)

AMR-A/D mode register H'C6 A/D converter

Bit	7	6	5	4	3	2	1	0
	CKS	—	—	—	CH3	CH2	CH1	CH0
Initial value	0	0	1	1	0	0	0	0
Read/Write	R/W	—	—	—	R/W	R/W	R/W	R/W

(Correct)

AMR-A/D mode register H'C6 A/D converter

Bit	7	6	5	4	3	2	1	0
	CKS	—	—	—	CH3	CH2	CH1	CH0
Initial value	0	0	1	1	0	0	0	0
Read/Write	R/W	R/W	—	—	R/W	R/W	R/W	R/W

Appendix B Internal I/O Registers
B.2 Functions
PMR2 ·····(P368)

(Incorrect)

PMR2-Port Mode Register 2 H'C9 I/O port

Bit	7	6	5	4	3	2	1	0
	—	—	POF1	—	—	—	—	IRQ0
Initial value	1	1	0	1	1	1	1	0
Read/Write	—	—	R/W	—	—	—	—	R/W

(Correct)

PMR2-Port Mode Register 2 H'C9 I/O port

Bit	7	6	5	4	3	2	1	0
	—	—	POF1	—	—	—	—	IRQ0
Initial value	1	1	0	1	1	—	—	0
Read/Write	—	—	R/W	—	—	W	W	R/W

Appendix B Internal I/O Registers
B.2 Functions
PMR3 ·····(P369)

(Incorrect)

PMR3-Port Mode Register 3 H'CA I/O port

Bit	7	6	5	4	3	2	1	0
	AEVL	AEVH	—	—	—	TMOFH	TMOFL	—
Initial value	0	0	—	—	—	0	0	—
Read/Write	R/W	R/W	—	—	—	R/W	R/W	—

(Correct)

PMR3-Port Mode Register 3 H'CA I/O port

Bit	7	6	5	4	3	2	1	0
	AEVL	AEVH	—	—	—	TMOFH	TMOFL	—
Initial value	0	0	—	—	—	0	0	—
Read/Write	R/W	R/W	W	W	W	R/W	R/W	W

Appendix B Internal I/O Registers
B.2 Functions
PDR3 ·····(P372)

(Incorrect)

PDR3-Port data register 3 H'D6 I/O ports

Bit	7	6	5	4	3	2	1	0
	P37	P36	P35	P34	P33	P32	P31	—
Initial value	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

(Correct)

PDR3-Port data register 3 H'D6 I/O port

Bit	7	6	5	4	3	2	1	0
	P37	P36	P35	P34	P33	P32	P31	—
Initial value	0	0	0	0	0	0	0	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

Appendix B Internal I/O Registers
B.2 Functions
PDR8 ·····(P373)

(Incorrect)

PDR8-Port data register 8 H'DB I/O ports

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	P80
Initial value	1	1	1	1	1	1	1	0
Read/Write	—	—	—	—	—	—	—	R/W

(Correct)

PDR8-Port data register 8 H'DB I/O port

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	P80
Initial value	—	—	—	—	—	—	—	0
Read/Write	—	—	—	—	—	—	—	R/W

Appendix B Internal I/O Registers
B.2 Functions
PUCR3 ·····(P374)

(Incorrect)

PUCR3-Port pull-up control register 3 H'E1 I/O ports

Bit	7	6	5	4	3	2	1	0
	PUCR37	PUCR36	PUCR35	PUCR34	PUCR33	PUCR32	PUCR31	—
Initial value	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

(Correct)

PUCR3-Port pull-up control register 3 H'E1 I/O port

Bit	7	6	5	4	3	2	1	0
	PUCR37	PUCR36	PUCR35	PUCR34	PUCR33	PUCR32	PUCR31	—
Initial value	0	0	0	0	0	0	0	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W

Appendix B Internal I/O Registers
B.2 Functions
PCR3 ·····(P375)

(Incorrect)

PCR3-Port control register 3 H'E6 I/O ports

Bit	7	6	5	4	3	2	1	0
	PCR37	PCR36	PCR35	PCR34	PCR33	PCR32	PCR31	—
Initial value	0	0	0	0	0	0	0	1
Read/Write	W	W	W	W	W	W	W	—

(Correct)

PCR3-Port control register 3 H'E6 I/O port

Bit	7	6	5	4	3	2	1	0
	PCR37	PCR36	PCR35	PCR34	PCR33	PCR32	PCR31	—
Initial value	0	0	0	0	0	0	0	—
Read/Write	W	W	W	W	W	W	W	W

Appendix B Internal I/O Registers
B.2 Functions
PCR8 ·····(P377)

(Incorrect)

PCR8-Port control register 8 H'EB I/O ports

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PCR80
Initial value	1	1	1	1	1	1	1	0
Read/Write	—	—	—	—	—	—	—	W

(Correct)

PCR8-Port control register 8 H'EB I/O port

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PCR80
Initial value	—	—	—	—	—	—	—	0
Read/Write	W	W	W	W	W	W	W	W

Appendix B Internal I/O Registers
B.2 Functions
PMR9 ·····(P377)

(Incorrect)

PMR9-Port mode register 9 H'EC I/O ports

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PIOFF	—	PWM2	PWM1
Initial value	1	1	1	1	0	1	0	0
Read/Write	—	—	—	—	R/W	—	R/W	R/W

(Correct)

PMR9-Port mode register 9 H'EC I/O port

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PIOFF	—	PWM2	PWM1
Initial value	1	1	1	1	0	—	0	0
Read/Write	—	—	—	—	R/W	W	R/W	R/W

Appendix B Internal I/O Registers
B.2 Functions
IEGR ·····(P381)

(Incorrect)

IEGR-IRQ edge select register H'F2 System control

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IEG1	IEG0
Initial value	0	1	1	1	1	1	0	0
Read/Write	—	—	—	—	—	—	R/W	R/W

(Correct)

IEGR-IRQ edge select register H'F2 System control

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IEG1	IEG0
Initial value	1	1	1	—	—	—	0	0
Read/Write	—	—	—	—	—	—	R/W	R/W

Appendix B Internal I/O Registers
B.2 Functions
IENR1 ·····(P382)

(Incorrect)

IENR1-Interrupt enable register 1 H'F3 System control

Bit	7	6	5	4	3	2	1	0
	IENTA	—	IENWP	—	—	IENEC2	IEN1	IEN0
Initial value	0	1	0	1	1	0	0	0
Read/Write	R/W	—	R/W	—	—	R/W	R/W	R/W

(Correct)

IENR1-Interrupt enable register 1 H'F3 System control

Bit	7	6	5	4	3	2	1	0
	IENTA	—	IENWP	—	—	IENEC2	IEN1	IEN0
Initial value	0	—	0	—	—	0	0	0
Read/Write	R/W	—	R/W	—	—	R/W	R/W	R/W

Appendix B Internal I/O Registers
B.2 Functions
IENR2 ·····(P383)

(Incorrect)

IENR2-Interrupt enable register 2 H'F4 System control

Bit	7	6	5	4	3	2	1	0
	IENDT	IENAD	—	—	IENTFH	IENTFL	—	IENEC
Initial value	0	0	1	1	0	0	1	0
Read/Write	R/(W)	R/(W)	—	—	R/(W)	R/(W)	—	R/(W)

(Correct)

IENR2-Interrupt enable register 2 H'F4 System control

Bit	7	6	5	4	3	2	1	0
	IENDT	IENAD	—	—	IENTFH	IENTFL	—	IENEC
Initial value	0	0	—	—	0	0	—	0
Read/Write	R/W	R/W	W	W	R/W	R/W	W	R/W

Appendix B Internal I/O Registers
B.2 Functions
IRR1 ·····(P384)

(Incorrect)

IRR1-Interrupt request register 1 H'F6 System control

Bit	7	6	5	4	3	2	1	0
	IRRTA	—	—	—	—	IRREC2	IRRI1	IRRI0
Initial value	0	1	1	1	1	0	0	0
Read/Write	R/W*	—	—	—	—	R/W*	R/W*	R/W*

(Correct)

IRR1-Interrupt request register 1 H'F6 System control

Bit	7	6	5	4	3	2	1	0
	IRRTA	—	—	—	—	IRREC2	IRRI1	IRRI0
Initial value	0	—	1	—	—	0	0	0
Read/Write	R/W*	—	—	—	—	R/W*	R/W*	R/W*

Appendix B Internal I/O Registers
B.2 Functions
IRR2 ·····(P385)

(Incorrect)

IRR2-Interrupt request register 2 H'F6 System control

Bit	7	6	5	4	3	2	1	0
	IRRDT	IRRAD	—	—	IRRTFH	IRRTFL	—	IRREC
Initial value	0	0	1	1	0	0	1	0
Read/Write	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*	—	R/(W)*

(Correct)

IRR2-Interrupt request register 2 H'F6 System control

Bit	7	6	5	4	3	2	1	0
	IRRDT	IRRAD	—	—	IRRTFH	IRRTFL	—	IRREC
Initial value	0	0	—	—	0	0	—	—
Read/Write	R/W*	R/W*	W	W	R/W*	R/W*	W	R/W*