RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan Renesas Electronics Corporation

Product Category	ſ	MPU/N	1CU									ument Io.	TN	I-SH7	'-A825	5A/E	Rev.	1.00
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Amendmer	nts																	
1. Page 2	294	of 1170	C															
11.4.1	Cor	nmon (Contro	l Reai	ster (C	MNCF	R) DPR	RTY bit										
							.,		-									
Origina	al:																	
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	•	
-	_	—	—	—	-	—	CKO STP	CKO DRV	_	_	_	—	—	—	-	DMSTP		
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	
	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3 END	2	1 HIZ	0 HIZ	1	
Initial value:		BSD	MAP		BLOCK		Y[1:0]						IAN		MEM	CNT		
	0 R	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R	0 R	0 R	0 R	1 R	0/1* R	0 R	0 R/W	0 R/W		
Ameno	ded:																	
Bit:	31	30	29	28	27	26	25 CKO	24 CKO	23	22	21	20	19	18	17	16	1	
L	_	—	—	-	-	—	STP	DRV	_	-	—	—	—	—	-	DMSTP		
	0 R	0 R	0 R	0 R	0 R	0 R	0 R/W	0 R/W	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R/W		
	15	14		12	11	10	9	8	7	6	5	4	3	2	1	0		
		BSD		[1:0]	BLOCK	10	3		<u> </u>				END		HIZ	HIZ	1	
	0	0	0	0	0	0	0	0	0	0	0	1	IAN 0/1*	0	0 MEM	CNT 0	J	
	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R/W	R/W		



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2.	Page	290	0I	1170

11.4.1 Common Control Register (CMNCR) DPRTY bit.

Original:

10, 9	DPRTY	00	R/W	DMA Burst Transfer Priority
	[1:0]			Specify the priority for a refresh request/bus mastership request during DMA burst transfer.
				00: Accepts a refresh request and bus mastership request during DMA burst transfer
				01: Accepts a refresh request but does not accept a bus mastership request during DMA burst transfer
				10: Accepts neither a refresh request nor a bus mastership request during DMA burst transfer
				11: Setting prohibited
A	and a de			
	ended:	00	P	Deserved
Ame 10, 9	ended:	00	R	Reserved These bits are always read as 0. The write value should
	ended:	00	R	
	ended:	00	R	These bits are always read as 0. The write value should
10, 9	-		R	These bits are always read as 0. The write value should
10, 9	ended:		R	These bits are always read as 0. The write value should
10, 9 3. Pag	-)	R	These bits are always read as 0. The write value should
10, 9 3. Pag 11.5	e 401 of 1170)	R	These bits are always read as 0. The write value should

Bits DPRTY[1:0] in CMNCR can select whether or not the bus request is received during DMAC burst transfer.

Amended:

The above description is deleted.

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11.4.6 Refresh Timer Control/Status Register (RTCSR) CMIE bit.

Original:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	_	—	_	_	_	_	—	—	—	—		—	—		—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	_	—	—	_	—	_	—	CMF	CMIE		CKS[2:0]		RRC[2:0]]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W



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Ame	naea:															
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	_	—	—	—	—
nitial value: R/W:	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	_	_	_	_	_	_	_	_	CMF			CKS[2:0			RRC[2:0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
6 0119	CN	11⊏	0		R/W	Cor	mare	Match	Interri	upt Ena	hla					
J	Civ		U		Γ\/ V V	Ena	ables o	or disat	oles a (CMF in et to 1	terrup	t reque	est whe	en the		
						0: E	Disable	s the (CMF in	terrupt	reque	est				
						1: E	Enables	s the C	CMF in	terrupt	reque	st				
															_	
	nded:															
6	_		0		R		served								_	
							ese bits ays be		lways	read as	s 0. Th	e write	e value	should	b	
11.4	.8 Ref	of 117(resh Ti		onstan	t Regis	ster (R	TCOR)								
11.4 Orig If the mair	.8 Ref inal: e CMII ntaineo	resh Ti E bit of d until t	the R	TCSR 1F bit i	t Regis is set t in RTC equests	to 1, ai SR is (n interr cleared	rupt is d to 0.	Clearir	ng the	CMF b	it in R	TCSR	affects	only i	nterru
11.4 Orig If the mair and	.8 Ref inal: e CMII ntainec does i	resh Ti E bit of d until t not affe	the R ⁻ the R ⁻ the CM	TCSR 1F bit i resh re	is set t in RTC	to 1, ai SR is (s. This	n interr clearec makes	rupt is d to 0. s it pos	Clearin sible to	ng the o	CMF b t the n	it in R ⁻ umber	TCSR of refr	affects esh rec	only i	nterru
11.4 Orig If the mair and refre	.8 Ref inal: e CMII ntainec does i	resh Ti E bit of d until t not affe interru	the R ⁻ the R ⁻ the CM	TCSR 1F bit i resh re	is set t in RTC equests	to 1, ai SR is (s. This	n interr clearec makes	rupt is d to 0. s it pos	Clearin sible to	ng the o	CMF b t the n	it in R ⁻ umber	TCSR of refr	affects esh rec	only i	nterru
11.4 Orig If the mair and refre	8 Ref inal: CMII tained does i sh by nded:	resh Ti E bit of d until t not affe interru	the R the R the CM ect refr pts, ar	TCSR IF bit i resh re	is set t in RTC equests	to 1, an SR is o . This the ref	n interr clearec makes fresh a	rupt is d to 0. s it pos nd inte	Clearir sible to erval tir	ng the o	CMF b t the n	it in R ⁻ umber	TCSR of refr	affects esh rec	only i	nterru
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11.4 Orig If the mair and refre	8 Ref inal: CMII tained does i sh by nded:	resh Ti E bit of d until t not affe interru	the R the R the CM ect refr pts, ar	TCSR IF bit i resh re	is set f in RTC equests specify	to 1, an SR is o . This the ref	n interr clearec makes fresh a	rupt is d to 0. s it pos nd inte	Clearir sible to erval tir	ng the o	CMF b t the n	it in R ⁻ umber	TCSR of refr	affects esh rec	only i	nterru
11.4 Orig If the mair and refre	8 Ref inal: CMII tained does i sh by nded:	resh Ti E bit of d until t not affe interru	the R the R the CM ect refr pts, ar	TCSR IF bit i resh re	is set f in RTC equests specify	to 1, an SR is o . This the ref	n interr clearec makes fresh a	rupt is d to 0. s it pos nd inte	Clearir sible to erval tir	ng the o	CMF b t the n	it in R ⁻ umber	TCSR of refr	affects esh rec	only i	nterru
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11.4 Orig If the mair and refre	8 Ref inal: CMII tained does i sh by nded:	resh Ti E bit of d until t not affe interru	the R the R the CM ect refr pts, ar	TCSR IF bit i resh re	is set f in RTC equests specify	to 1, an SR is o . This the ref	n interr clearec makes fresh a	rupt is d to 0. s it pos nd inte	Clearir sible to erval tir	ng the o	CMF b t the n	it in R ⁻ umber	TCSR of refr	affects esh rec	only i	nterru
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11.4 Orig If the mair and refre	8 Ref inal: CMII tained does i sh by nded:	resh Ti E bit of d until t not affe interru	the R the R the CM ect refr pts, ar	TCSR IF bit i resh re	is set f in RTC equests specify	to 1, an SR is o . This the ref	n interr clearec makes fresh a	rupt is d to 0. s it pos nd inte	Clearir sible to erval tir	ng the o	CMF b t the n	it in R ⁻ umber	TCSR of refr	affects esh rec	only i	nterru
11.4 Orig If the mair and refre	8 Ref inal: CMII tained does i sh by nded:	resh Ti E bit of d until t not affe interru	the R the R the CM ect refr pts, ar	TCSR IF bit i resh re	is set f in RTC equests specify	to 1, an SR is o . This the ref	n interr clearec makes fresh a	rupt is d to 0. s it pos nd inte	Clearir sible to erval tir	ng the o	CMF b t the n	it in R ⁻ umber	TCSR of refr	affects esh rec	only i	nterru
11.4 Orig If the mair and refre	8 Ref inal: CMII tained does i sh by nded:	resh Ti E bit of d until t not affe interru	the R the R the CM ect refr pts, ar	TCSR IF bit i resh re	is set f in RTC equests specify	to 1, an SR is o . This the ref	n interr clearec makes fresh a	rupt is d to 0. s it pos nd inte	Clearir sible to erval tir	ng the o	CMF b t the n	it in R ⁻ umber	TCSR of refr	affects esh rec	only i	nterru
11.4 Orig If the mair and refre	8 Ref inal: CMII tained does i sh by nded:	resh Ti E bit of d until t not affe interru	the R the R the CM ect refr pts, ar	TCSR IF bit i resh re	is set f in RTC equests specify	to 1, an SR is o . This the ref	n interr clearec makes fresh a	rupt is d to 0. s it pos nd inte	Clearir sible to erval tir	ng the o	CMF b t the n	it in R ⁻ umber	TCSR of refr	affects esh rec	only i	nterru

