To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A587A/E	Rev.	1.00
Title	Amendment of SH7720 Hardware manual(4)		Information Category	Technical Notification		
Applicable Product	HD6417720	Lot No.	Reference Document	SH7720 hardware manual Rev2.00 (REJ09B0033-0200)		
		All				

There are the amendments and additions of SH7720 Hardware manual Rev2.00.

Amendments and additions

1. Page 240 of 1382, Section 8

   "Table 8.2 Interrupt Sources and IPRA to IPRJ"

   Amendment

   Original:

Register	Bits 15 to 12	Bits 11 to 8	Bits 7 to 4	Bits 3 to 0
IPRD	USBF (USBF_SPD)	TMU (TMU_SUNI)	IRQ5	IRQ4

   Amended:

Register	Bits 15 to 12	Bits 11 to 8	Bits 7 to 4	Bits 3 to 0
IPRD	Reserved*	TMU (TMU_SUNI)	IRQ5	IRQ4

2. Page 243 of 1382, Section 8

   "8.3.4 Interrupt Request Register 0 (IRR0)"

   Amendment

   Original:

Bit	Bit Name	Initial Value	R/W	Description
7	USBF_SPDR	0	R/W	USBF_SPD Interrupt Request

   Amended:

Bit	Bit Name	Initial Value	R/W	Description
7	-	0	R/W	Reserved
				This bit is always read as 0.
				The write value should be 0.

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3. Page 260 of 1382,   Section 8

"Table 8.3 Interrupt Exception Handling Sources and Priority (IRQ Mode)"

Amendment

Original:

Interrupt	Source	Interrupt Code *1	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Unit
USBF	USBF_SPD	H'6E0*3	0 to 15 (0)	IPRD (15 to 12)	-

Amended:

Interrupt	Source	Interrupt Code *1	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Unit
-	-	-	-	-	-

4. Page 262 of 1382,   Section 8

"Table 8.4 Interrupt Exception Handling Sources and Priority (IRL Mode)"

Amendment

Original:

Interrupt	Source	Interrupt Code *1	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Unit
USBF	USBF_SPD	H'6E0*3	0 to 15 (0)	IPRD (15 to 12)	-

Amended:

Interrupt	Source	Interrupt Code *1	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Unit
-	-	-	-	-	-

5. Page 783 of 1382,   Section 25

"25.3.1 Interrupt Flag Register 0 (IFR0)"

Amendment

Original:

When each flag is set to 1 and an interrupt is enabled in the corresponding bit of IER0,an interrupt occurs

from the INT pin specified by the corresponding bit in ISR0.

Amended:

When each flag is set to 1 and an interrupt is enabled in the corresponding bit of IER0,

an interrupt request specified by the corresponding bit in ISR0 is issued.

6. Page 786 of 1382,   Section 25

  "25.3.2 Interrupt Flag Register 1 (IFR1)"

  Amendment

  Original:

  When each flag is set to 1 and an interrupt is enabled in the corresponding bit of IER1, an interrupt occurs

  from the INT pin specified by the corresponding bit in ISR1.

  Amended:

  When each flag is set to 1 and an interrupt is enabled in the corresponding bit of IER1,

  an interrupt request specified by the corresponding bit in ISR1 is issued.

7. Page 787 of 1382,   Section 25

  "25.3.3 Interrupt Flag Register 2 (IFR2)"

  Amendment

  Original:

  When each flag is set to 1 and an interrupt is enabled in the corresponding bit of IER2, an interrupt occurs

  from the INT pin specified by the corresponding bit in ISR2.

  Amended:

  When each flag is set to 1 and an interrupt is enabled in the corresponding bit of IER2,

  an interrupt request specified by the corresponding bit in ISR2 is issued.

8. Page 789 of 1382,   Section 25

  "25.3.4 Interrupt Flag Register 3 (IFR3)"

  Amendment

  Original:

  When each flag is set to 1 and an interrupt is enabled in the corresponding bit of IER3, an interrupt occurs

  from the INT pin specified by the corresponding bit in ISR3.

  Amended:

  When each flag is set to 1 and an interrupt is enabled in the corresponding bit of IER3,

  an interrupt request specified by the corresponding bit in ISR3 is issued.

9. Page 791 of 1382,   Section 25

  "25.3.5 Interrupt Flag Register 4 (IFR4)"

  Amendment

  Original:

  When each flag is set to 1 and an interrupt is enabled in the corresponding bit of IER4, an interrupt occurs

  from the INT pin specified by the corresponding bit in ISR4.

  Amended:

  When each flag is set to 1 and an interrupt is enabled in the corresponding bit of IER4,

  an interrupt request specified by the corresponding bit in ISR4 is issued.

10. Page 791 of 1382,   Section 25

  "25.3.6 Interrupt Select Register 0 (ISR0)"

  Amendment

  Original:

  ISR0 selects the INT pin to output the interrupt requests indicated in interrupt flag register 0.

  When the corresponding bit in ISR2 is cleared to 0, an interrupt request is issued from the INT0N pin.

  When the bit is set to 1, an interrupt request is issued from the INT1N pin. In the initial value,

  each of interrupt source of the interrupt flag register 0 is issued from the INT0N pin.

  Amended:

  ISR0 selects the interrupt requests of the interrupt controller (INTC) indicated in interrupt flag register 0.

  When the corresponding bit in ISR0 is cleared to 0, the USBFI0 interrupt request is selected.

  When the bit is set to 1, the USBFI1 interrupt request is selected. In the initial value,

  each of interrupt source of the interrupt flag register 0 selects the USBFI0 interrupt request.

11. Page 792 of 1382,   Section 25

  "25.3.7 Interrupt Select Register 1 (ISR1)"

  Amendment

  Original:

  ISR1 selects the INT pin to output the interrupt requests indicated in interrupt flag register 1.

  When the corresponding bit in ISR1 is cleared to 0, an interrupt request is issued from the INT0N pin.

  When the bit is set to 1, an interrupt request is issued from the INT1N pin. In the initial value,

  each of interrupt source of the interrupt flag register 1 is issued from the INT1N pin.

  Amended:

  ISR1 selects the interrupt requests of the interrupt controller (INTC) indicated in interrupt flag register 1.

  When the corresponding bit in ISR1 is cleared to 0, the USBFI0 interrupt request is selected.

  When the bit is set to 1, the USBFI1 interrupt request is selected. In the initial value,

  each of interrupt source of the interrupt flag register 1 selects the USBFI1 interrupt request.

12. Page 792 of 1382,   Section 25

"25.3.8 Interrupt Select Register 2 (ISR2)"

Amendment

Original:

ISR2 selects the INT pin to output the interrupt requests indicated in interrupt flag register 2.

When the corresponding bit in ISR2 is cleared to 0, an interrupt request is issued from the INT0N pin.

When the bit is set to 1, an interrupt request is issued from the INT1N pin. In the initial value,

each of interrupt source of the interrupt flag register 2 is issued from the INT1N pin.

Amended:

ISR2 selects the interrupt requests of the interrupt controller (INTC) indicated in interrupt flag register 2.

When the corresponding bit in ISR2 is cleared to 0, the USBFI0 interrupt request is selected.

When the bit is set to 1, the USBFI1 interrupt request is selected. In the initial value,

each of interrupt source of the interrupt flag register 2 selects the USBFI1 interrupt request.

13. Page 793 of 1382,   Section 25

"25.3.9 Interrupt Select Register 3 (ISR3)"

Amendment

Original:

ISR3 selects the INT pin to output the interrupt requests indicated in interrupt flag register 3.

When the corresponding bit in ISR3 is cleared to 0, an interrupt request is issued from the INT0N pin.

When the bit is set to 1, an interrupt request is issued from the INT1N pin. In the initial value,

each of interrupt source of the interrupt flag register 3 is issued from the INT0N pin.

Amended:

ISR3 selects the interrupt requests of the interrupt controller (INTC) indicated in interrupt flag register 3.

When the corresponding bit in ISR3 is cleared to 0, the USBFI0 interrupt request is selected.

When the bit is set to 1, the USBFI1 interrupt request is selected. In the initial value,

each of interrupt source of the interrupt flag register 3 selects the USBFI0 interrupt request.

14. Page 793 of 1382,   Section 25

"25.3.10 Interrupt Select Register 4 (ISR4)"

Amendment

Original:

ISR4 selects the INT pin to output the interrupt requests indicated in interrupt flag register 4.

When the corresponding bit in ISR4 is cleared to 0, an interrupt request is issued from the INT0N pin.

When the bit is set to 1, an interrupt request is issued from the INT1N pin. In the initial value,

each of interrupt source of the interrupt flag register 4 is issued from the INT0N pin.

Amended:

ISR4 selects the interrupt requests of the interrupt controller (INTC) indicated in interrupt flag register 4.

When the corresponding bit in ISR4 is cleared to 0, the USBFI0 interrupt request is selected.

When the bit is set to 1, the USBFI1 interrupt request is selected. In the initial value,

each of interrupt source of the interrupt flag register 4 selects the USBFI0 interrupt request.

15. Page 794 of 1382,   Section 25

"25.3.11 Interrupt Enable Register 0 (IER0)"

Amendment

Original:

When an interrupt flag is set to 1 while the corresponding bit of each interrupt is set to 1, the INTN pin set

in the interrupt select register 0 is asserted low and an interrupt request is issued.

Amended:

When an interrupt flag is set to 1 while the corresponding bit of each interrupt is set to 1,

an interrupt request set in the interrupt select register 0 is issued.

16. Page 794 of 1382,   Section 25

"25.3.12 Interrupt Enable Register 1 (IER1)"

Amendment

Original:

When an interrupt flag is set to 1 while the corresponding bit of each interrupt is set to 1, the INTN pin set

in the interrupt select register 1 is asserted low and an interrupt request is issued.

Amended:

When an interrupt flag is set to 1 while the corresponding bit of each interrupt is set to 1,

an interrupt request set in the interrupt select register 1 is issued.

17. Page 795 of 1382,   Section 25

"25.3.13 Interrupt Enable Register 2 (IER2)"

Amendment

Original:

When an interrupt flag is set to 1 while the corresponding bit of each interrupt is set to 1, the INTN pin set

in the interrupt select register 2 is asserted low and an interrupt request is issued.

Amended:

When an interrupt flag is set to 1 while the corresponding bit of each interrupt is set to 1,

an interrupt request in the interrupt select register 2 is issued.

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18. Page 795 of 1382,   Section 25

   "25.3.14 Interrupt Enable Register 3 (IER3)"

   Amendment

   Original:

   When an interrupt flag is set to 1 while the corresponding bit of each interrupt is set to 1, the INTN pin set

   in the interrupt select register 3 is asserted low and an interrupt request is issued.

   Amended:

   When an interrupt flag is set to 1 while the corresponding bit of each interrupt is set to 1,

   an interrupt request set in the interrupt select register 3 is issued.

19. Page 796 of 1382,   Section 25

   "25.3.15 Interrupt Enable Register 4 (IER4)"

   Amendment

   Original:

   When an interrupt flag is set to 1 while the corresponding bit of each interrupt is set to 1, the INTN pin set

   in the interrupt select register 4 is asserted low and an interrupt request is issued.

   Amended:

   When an interrupt flag is set to 1 while the corresponding bit of each interrupt is set to 1,

   an interrupt request set in the interrupt select register 4 is issued.

20. Page 825 of 1382,   Section 25

   "Figure 25.14 EP4 Isochronous-Out Transfer Operation (SOF is Normal)"

   Amendment

   Original: INTN

   Amended : Interrupt Request

21. Page 826 of 1382,   Section 25

   "Figure 25.15 EP4 Isochronous-Out Transfer Operation (SOF is Broken)"

   Amendment

   Original: INTN

   Amended : Interrupt Request

22. Page 828 of 1382,   Section 25

   "Figure 25.16 EP5 Isochronous-In Transfer Operation (SOF is Normal)"

   Amendment

   Original: INTN

   Amended : Interrupt Request

23. Page 829 of 1382,   Section 25

"Figure 25.17 EP5 Isochronous-In Transfer Operation (SOF in Broken)"

Amendment

Original: INTN

Amended : Interrupt Request

21. Page 1222 of 1382,   Section 37

"37.2 Register Bits"

Amendment

Original:

Register	Bit 31/	Bit 30/	Bit 29/	Bit 28/	Bit 27/	Bit 26/	Bit 25/	Bit 24/	
Abbreviation	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0	Module
IRR0	USBF_SPDR	TMU_SUNIR	IRQ5R	IRQ4R	IRQ3R	IRQ2R	IRQ1R	IRQ0R	INTC

Amended:

Register	Bit 31/	Bit 30/	Bit 29/	Bit 28/	Bit 27/	Bit 26/	Bit 25/	Bit 24/	
Abbreviation	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0	Module
IRR0	-	TMU_SUNIR	IRQ5R	IRQ4R	IRQ3R	IRQ2R	IRQ1R	IRQ0R	INTC

22. Page 1222 of 1382,   Section 37

"37.2 Register Bits"

Amendment

Original:

Register	Bit 31/	Bit 30/	Bit 29/	Bit 28/	Bit 27/	Bit 26/	Bit 25/	Bit 24/	
Abbreviation	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0	Module
IPRD	USBF (USBF_SPD)				TMU (TMU_SUNI)				INTC

Amended:

Register	Bit 31/	Bit 30/	Bit 29/	Bit 28/	Bit 27/	Bit 26/	Bit 25/	Bit 24/	
Abbreviation	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0	Module
IPRD	-				TMU (TMU_SUNI)				INTC