To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A572A/E	Rev.	1.00
Title	Amendment of SH7720 hardware manual (2)		Information Category	Technical Notification		
Applicable Product	HD6417720	Lot No. All	Reference Document	SH7720 hardware manual (REJ09B0033-0200 Rev2.00)		

There are the amendments and additions of SH7720 hardware manual Rev2.00.

Amendments and additions.

1. Page 10 of 1382, Section 1

Amendment

Original:

Pin No.	Pin Name	Pin No.	Pin Name
K17	SCIF0_TxD/PTT2	L17	SCIF0_RxD/PTT1

Amended:

Pin No.	Pin Name	Pin No.	Pin Name
K17	SCIF0_TxD/IrTx/PTT2	L17	SCIF0_RxD/IrRx/PTT1

2. Page 11 of 1382, Section 1

Amendment

Original:

Pin No.	Pin Name	Pin No.	Pin Name
K1	VccQ1	L1	VssQ1
L20	SCIF0_TxD/PTT2	L21	SCIF0_RxD/PTT1
U5	D15		

Amended:

Pin No.	Pin Name	Pin No.	Pin Name
K1	VssQ1	L1	VccQ1
L20	SCIF0_TxD/IrTx/PTT2	L21	SCIF0_RxD/IrRx/PTT1
U5	D5		

3. Page 17 of 1382, Section 1

Amendment

Original:

Pin No. (PLBG0256GA-A)	Pin No. (PLBG0256KA-A)	Pin Name	Function	I/O	I/O Buffer Power Supply
K17	L20	SCIF0_TxD/PTT2	Transmit data/general-purpose port	O/IO	VccQ

Amended:

Pin No. (PLBG0256GA-A)	Pin No. (PLBG0256KA-A)	Pin Name	Function	I/O	I/O Buffer Power Supply
K17	L20	SCIF0_TxD/IrTx/PTT2	Transmit data/transmit data/ general-purpose port	O/O/IO	VccQ

4. Page 18 of 1382, Section 1

Amendment

Original:

Pin No. (PLBG0256GA-A)	Pin No. (PLBG0256KA-A)	Pin Name	Function	I/O	I/O Buffer Power Supply
L17	L21	SCIF0_RxD/PTT1	Receive data/general-purpose port	I/IO	VccQ

Amended:

Pin No. (PLBG0256GA-A)	Pin No. (PLBG0256KA-A)	Pin Name	Function	I/O	I/O Buffer Power Supply
L17	L21	SCIF0_RxD/IrRx/PTT1	Receive data/receive data/ general-purpose port	I/I/IO	VccQ

5. Page 439 of 1382, Section 11

Amendment

Original:

9. USBH/USBF Clock Control Register: The USBH/USBF clock control register is assigned the source clock which generates the USBH/USBF and frequency division ration.

Amended:

9. USBH/USBF Clock Control Register: The USBH/USBF clock control register is assigned the source clock which generates the USBH/USBF.

6. Page 444 of 1382, Section 11

Amendment

Original:

Bit	Bit Name	Initial Value	R/W	Description
15	PLL2EN	0	R/W	PLL2 Enable PLL2EN specifies whether make the PLL circuit 2 ON in clock operating mode 7. When the PLL circuit 2 is necessary to output the USBH/USBF clock, PLL2EN makes the circuit ON. The PLL circuit 2 is ON in non-clock operating mode 7 regardless of the PLL2EN setting. 0: PLL circuit 2 is OFF 1: PLL circuit 2 is ON

Amended:

Bit	Bit Name	Initial Value	R/W	Description
15	PLL2EN	0	R/W	PLL2 Enable PLL2EN specifies whether make the PLL circuit 2 ON in clock operating mode 7. The PLL circuit 2 is ON in non-clock operating mode 7 regardless of the PLL2EN setting. 0: PLL circuit 2 is OFF 1: PLL circuit 2 is ON

7. Page 1022 of 1382, Section 31

Amendment

Original: The 40-MHz peripheral clock is needed, and bits CSEL3 to CSEL0 should be set to 0001 for a 20-Mbps transfer clock of the MMCIF.

Amended: The 33-MHz peripheral clock is needed, and bits CSEL3 to CSEL0 should be set to 0001 for a 16.5-Mbps transfer clock of the MMCIF.

8. Page 1114 of 1382, Section 34

Amendment

Original:

Port	Port Function (Related Module)	Other Function (Related Module)
T	PTT2 input/output (port)	SCIF0_TxD output (SCIF)
	PTT1 input/output (port)	SCIF0_RxD input (SCIF)

Amended:

Port	Port Function (Related Module)	Other Function (Related Module)
T	PTT2 input/output (port)	SCIF0_TxD output (SCIF) / IrTx output (IrDA)
	PTT1 input/output (port)	SCIF0_RxD input (SCIF) / IrRx input (IrDA)

9. Page 1177 of 1382, Section 35

Amendment

Original:

PTT2 (input/output) / SCIF0_TxD (output)

PTT1 (input/output) / SCIF0_RxD (input)

Amended:

PTT2 (input/output) / IrTx (Output) / SCIF0_TxD (output)

PTT1 (input/output) / IrRx (input) / SCIF0_RxD (input)

10. Page 1191 of 1382, Section 36

Amendment

Original:

Bit	Pin Name	I/O	Bit	Pin Name	I/O
224	A19/PTR1	Control	194	SCIF0_RxD/PTT1	IN
223	A20/PTR2	Control	193	SCIF0_TxD/PTT2	IN

Amended:

Bit	Pin Name	I/O	Bit	Pin Name	I/O
224	A19/PTR1	Control	194	SCIF0_RxD/IrRx/PTT1	IN
223	A20/PTR2	Control	193	SCIF0_TxD/IrTx/PTT2	IN

11. Page 1192 of 1382, Section 36

Amendment

Original:

Bit	Pin Name	I/O	Bit	Pin Name	I/O
176	USB1d_TXDPLS/AFE_SCLK/$\overline{\text{IOIS16}}$/ $\overline{\text{PCC\_IOIS16}}$/PTG4	IN	155	SCIF0_RxD/PTT1	OUT
175	USB1d_TXSE0/IRQ4/AFE_TXOUT/ $\overline{\text{PCC\_DRV}}$/PTG5	IN	154	SCIF0_TxD/PTT2	OUT

Amended:

Bit	Pin Name	I/O	Bit	Pin Name	I/O
176	USB1d_TXDPLS/AFE_SCLK/$\overline{\text{IOIS16}}$/ $\overline{\text{PCC\_IOIS16}}$/PTG4	IN	155	SCIF0_RxD/IrRx/PTT1	OUT
175	USB1d_TXSE0/IRQ4/AFE_TXOUT/ $\overline{\text{PCC\_DRV}}$/PTG5	IN	154	SCIF0_TxD/IrTx/PTT2	OUT

12. Page 1193 of 1382, Section 36

AmendmentOriginal:

Bit	Pin Name	I/O	Bit	Pin Name	I/O
137	USB1d_TXDPLS/AFE_SCLK/$\overline{\text{IOIS16}}$/$\overline{\text{PCC\_IOIS16}}$/PTG4	OUT	117	SCIF0_RxD/PTT1	Control
136	USB1d_TXSE0/IRQ4/AFE_TXOUT/$\overline{\text{PCC\_DRV}}$/PTG5	OUT	116	SCIF0_TxD/PTT2	Control

Amended:

Bit	Pin Name	I/O	Bit	Pin Name	I/O
137	USB1d_TXDPLS/AFE_SCLK/$\overline{\text{IOIS16}}$/$\overline{\text{PCC\_IOIS16}}$/PTG4	OUT	117	SCIF0_RxD/IrRx/PTT1	Control
136	USB1d_TXSE0/IRQ4/AFE_TXOUT/$\overline{\text{PCC\_DRV}}$/PTG5	OUT	116	SCIF0_TxD/IrTx/PTT2	Control

13. Page 1335 of 1382, Section 38

Amendment

Original:

Item	Symbol	Min.	Max.	Unit	Figure
UCLK external input clock frequency (48 MHz)	t_{FREQ}	47.9	48.1	MHz	38.66
Clock rise time	t_{R48}	—	2	ns	
Clock fall time	t_{F48}	—	2	ns	
Duty (t_{HIGH}/t_{LOW})	t_{DUTY}	90	110	%	

Amended:

Item	Symbol	Min.	Max.	Unit	Figure
EXTAL_USB clock frequency (48 MHz)	t_{FREQ}	47.9	48.1	MHz	38.66
Clock rise time	t_{R48}	—	6	ns	
Clock fall time	t_{F48}	—	6	ns	

14. Page 1351 of 1382, Appendix

Amendment

Original:

Category									
PLBG0256GA-A	PLBG0256KA-A	Pin Name	Power-On Reset	Manual Reset	Software Standby	Hardware Standby	Bus Release	I/O	Handling of Unused Pins
K17	L20	SCIF0_TxD/PTT2	V	Z/P	Z/K	Z/Z	O/P	O/IO	Open
L17	L21	SCIF0_RxD/PTT1	V	Z/P	Z/K	Z/Z	I/P	I/IO	Open

Amended:

Category									
PLBG0256GA-A	PLBG0256KA-A	Pin Name	Power-On Reset	Manual Reset	Software Standby	Hardware Standby	Bus Release	I/O	Handling of Unused Pins
K17	L20	SCIF0_TxD/IrTx/PTT2	V	Z/Z/P	Z/Z/K	Z/Z/Z	O/O/P	O/O/IO	Open
L17	L21	SCIF0_RxD/IrRx/PTT1	V	Z/Z/P	Z/Z/K	Z/Z/Z	I/I/P	I/I/IO	Open