To our customers,

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**Old Company Name in Catalogs and Other Documents**

On April 1\textsuperscript{st}, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: [http://www.renesas.com](http://www.renesas.com)

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April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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Issued by: Renesas Electronics Corporation ([http://www.renesas.com](http://www.renesas.com))

There are the amendments and additions of MultiMediaCard Interface of SH7720 hardware manual Rev2.00.

Amendments and additions.

1. Page 1024 of 1382, Section 31

Amendment

Original:

DMACR sets DMA request signal output. DMAEN enables/disables a DMA request signal. The DMA request signal is output by a value that has been set to bits SET2 to SET0.

Amended:

DMACR sets DMA request signal output. DMAEN enables/disables a DMA request signal. The DMA request signal is output by a value that has been set to bits SET2 to SET0.

Before executing a command (CMD18, CMD25) in the multiblock transfer, this register should be set.

Auto mode is not used in open-ended multi block transfer.
2. Page 1075 of 1382, Section 31

Amendment

Original:

Command sequence start

→ FIFO clear

→ Write transfer block size to TBCR

→ Execute CMD16

→ Does CMD16 end successfully?

   Yes

   → Write the number of transfer blocks to TBNCR

   → Execute CMD23

   → Does CMD23 end successfully?

      Yes

      → Execute CMD25 (CMDR to CMDSTRT)

      → Is CRCERI interrupt generated?

         Yes

         → Set DMAC

         → Set DMACR (MMCIF)

         → [1]

      → Is CRPI interrupt generated?

         Yes

         → Read response register

         → Is response status normal?

            Yes

            → Set DMAC

            → Set DMACR (MMCIF)

            → [1]

         → Is CTERI interrupt generated?

            Yes

            → Read response register

            → Is response status normal?

               Yes

               → [2]

      → No

         → Is CTERI interrupt generated?

            Yes

            → [1]

            → [2]

Amended:

Command sequence start

→ FIFO clear

→ Write transfer block size to TBCR

→ Execute CMD16

→ Does CMD16 end successfully?

   Yes

   → Write the number of transfer blocks to TBNCR

   → Execute CMD23

   → Does CMD23 end successfully?

      Yes

      → Execute CMD25 (CMDR to CMDSTRT)

      → Is CRCERI interrupt generated?

         Yes

         → Set DMAC

         → Set DMACR (MMCIF)

         → [1]

      → Is CRPI interrupt generated?

         Yes

         → Read response register

         → Is response status normal?

            Yes

            → Set DMAC

            → Set DMACR (MMCIF)

            → [1]

         → Is CTERI interrupt generated?

            Yes

            → [2]

      → No

         → Is CTERI interrupt generated?

            Yes

            → [1]

            → [2]