To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1st, 2010
Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Renesas Technology Corp.

Product Category	MPU/MCU		Document No.	TN-H8*-A415A/E	Rev.	1.00
Title	An amendment to the H8S/2472 Group, H8S/2463 Group, H8S/2462 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	H8S/2472, 2463, 2462 Group	Lot No. All Lots	Reference Document	H8S/2472 Group, H8S/2463 Group, H8S/2462 Group Hardware Manual Rev.2.00 REJ09B0403-0200		

We would like to inform you about the amendment to the H8S/2472 Group, H8S/2463 Group, H8S/2462 Group Hardware Manual

Section 3 MCU Operating Modes

3.3 Operating Mode Descriptions

3.3.1 MODE 2

[Error]

・Multiplex extended mode

When 8-bit bus is specified, port 1 functions as the port for address output and data input/output regardless of the setting of the data direction register (DDR). Ports 2 (P23 to P20) and 4 (P47 to P44) can be used as a general port.

When 16-bit bus is specified, ports 1, 2 (P23 to P20), and 4 (P47 to P44) function as the port for address output and data input/output regardless of the setting of the data direction register (DDR).

[Correct]

・Multiplex extended mode

When 8-bit bus is specified, **port 2 (P23 to P20), and 4 (P47 to P44)** functions as the port for address output and data input/output regardless of the setting of the data direction register (DDR). **Ports 1** can be used as a general port.

When 16-bit bus is specified, ports 1, 2 (P23 to P20), and 4 (P47 to P44) function as the port for address output and data input/output regardless of the setting of the data direction register (DDR).

Section 6.Bus Controller (BSC)

6.5 Bus Interface

6.5.1 Data Size and Data Alignment

[Error]

(1) 8-Bit Access Space

Figure 6.3 illustrates data alignment control for the 8-bit access space. With the 8-bit access space, the upper data bus (D15 to D8) is always used for accesses. The amount of data that can be accessed at one time is one byte: a word access is performed as two byte accesses, and a longword access, as four byte accesses.

The lower data bus (AD7 to AD0) is used in address-data multiplex extended mode.

[Correct]

(1) 8-Bit Access Space

Figure 6.3 illustrates data alignment control for the 8-bit access space. With the 8-bit access space, the upper data bus (D15 to D8) is always used for accesses. The amount of data that can be accessed at one time is one byte: a word access is performed as two byte accesses, and a longword access, as four byte accesses.

The upper data bus (AD15 to AD8) is used in address-data multiplex extended mode.

Section 6.Bus Controller (BSC)

6.5 Bus Interface

6.5.2 Valid Strobes

[Error]

Table 6.13 Data Buses Used and Valid Strobes

Area	Access Size	Read/ Write	Address	Valid Strobe	Upper Data Bus (D15 to D8/ AD15 to AD8)	Lower Data Bus (D7 to D0/ AD7 to AD0)
8-bit access space	Byte	Read	—	$\overline{RD}$	Valid	Ports or others
		Write	—	$\overline{HWR}$		
8-bit access space (in address-data multiplex extended mode)	Byte	Read	—	$\overline{RD}$	Ports or others	Valid
		Write	—	$\overline{HWR}$		
16-bit access space	Byte	Read	Even	$\overline{RD}$	Valid	Invalid
			Odd		Invalid	Valid
		Write	Even	$\overline{HWR}$	Valid	Undefined
			Odd	$\overline{LWR}$	Undefined	Valid
	Word	Read	—	$\overline{RD}$	Valid	Valid
		Write	—	$\overline{HWR}$, $\overline{LWR}$		

[Correct]

Table 6.13 Data Buses Used and Valid Strobes

Area	Access Size	Read/ Write	Address	Valid Strobe	Upper Data Bus (D15 to D8/ AD15 to AD8)	Lower Data Bus (D7 to D0/ AD7 to AD0)
8-bit access space	Byte	Read	—	$\overline{RD}$	Valid	Ports or others
		Write	—	$\overline{HWR}$		
8-bit access space (in address-data multiplex extended mode)	Byte	Read	—	$\overline{RD}$	**Valid**	**Ports or others**
		Write	—	$\overline{HWR}$		
16-bit access space	Byte	Read	Even	$\overline{RD}$	Valid	Invalid
			Odd		Invalid	Valid
		Write	Even	$\overline{HWR}$	Valid	Undefined
			Odd	$\overline{LWR}$	Undefined	Valid
	Word	Read	—	$\overline{RD}$	Valid	Valid
		Write	—	$\overline{HWR}$, $\overline{LWR}$		

Section 6.Bus Controller (BSC)

6.5 Bus Interface

6.5.5 Basic Operation Timing in Address-Data Multiplex Extended Mode

[Error]

(1) 8-Bit, 2-State Data Access Space

Figures 6.16 and 6.17 show the bus timing for an 8-bit, 2-state access space. When an 8-bit access space is accessed, the lower half (AD7 to AD0) of the data bus is used. Wait states cannot be inserted.

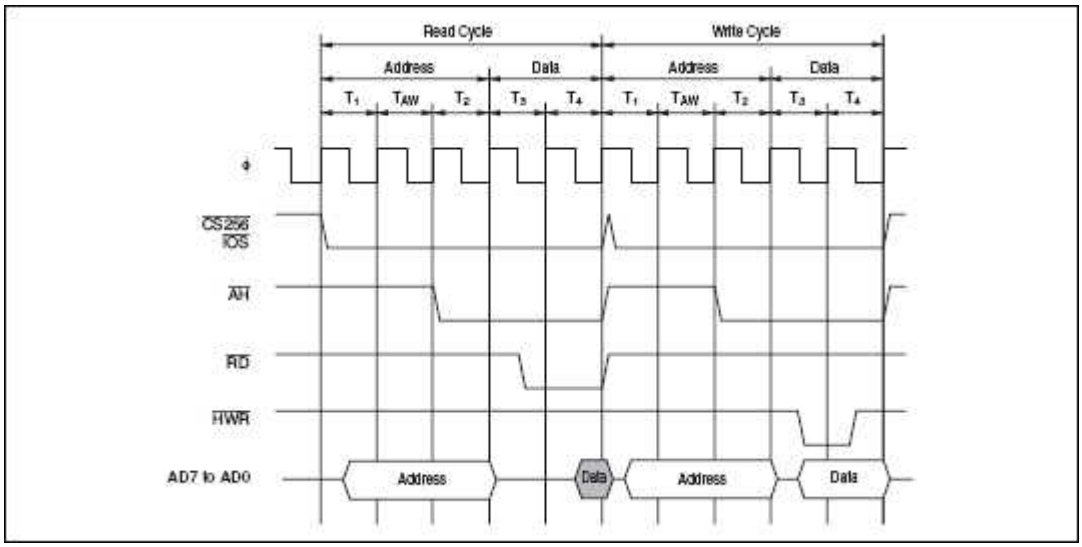

Figure 6.16 Bus Timing for 8-Bit, 2-State Access Space

[Correct]

(1) 8-Bit, 2-State Data Access Space

Figures 6.16 and 6.17 show the bus timing for an 8-bit, 2-state access space. When an 8-bit access space is accessed, **the upper half (AD15 to AD8)** of the data bus is used. Wait states cannot be inserted.

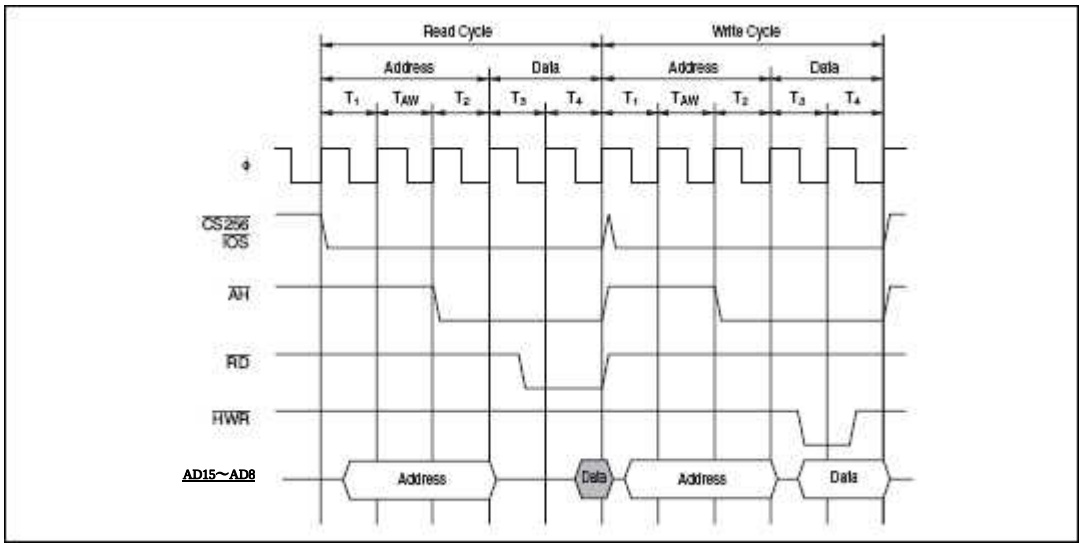

Figure 6.16 Bus Timing for 8-Bit, 2-State Access Space

Section 6.Bus Controller (BSC)

6.5 Bus Interface

6.5.5 Basic Operation Timing in Address-Data Multiplex Extended Mode

[Error]

(1) 8-Bit, 2-State Data Access Space

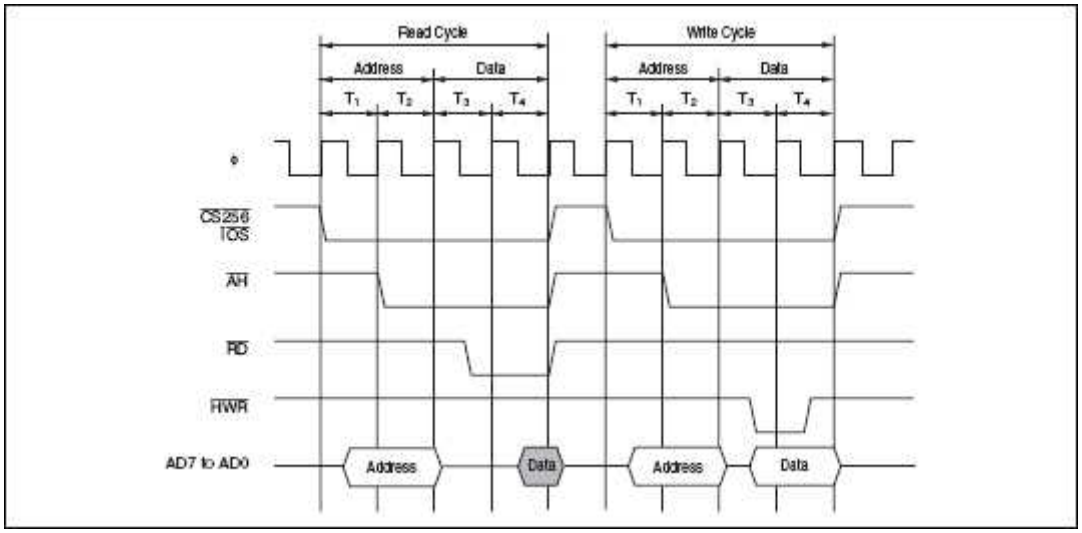

Figure 6.17 Bus Timing for 8-Bit, 2-State Access Space

[Correct]

(1) 8-Bit, 2-State Data Access Space

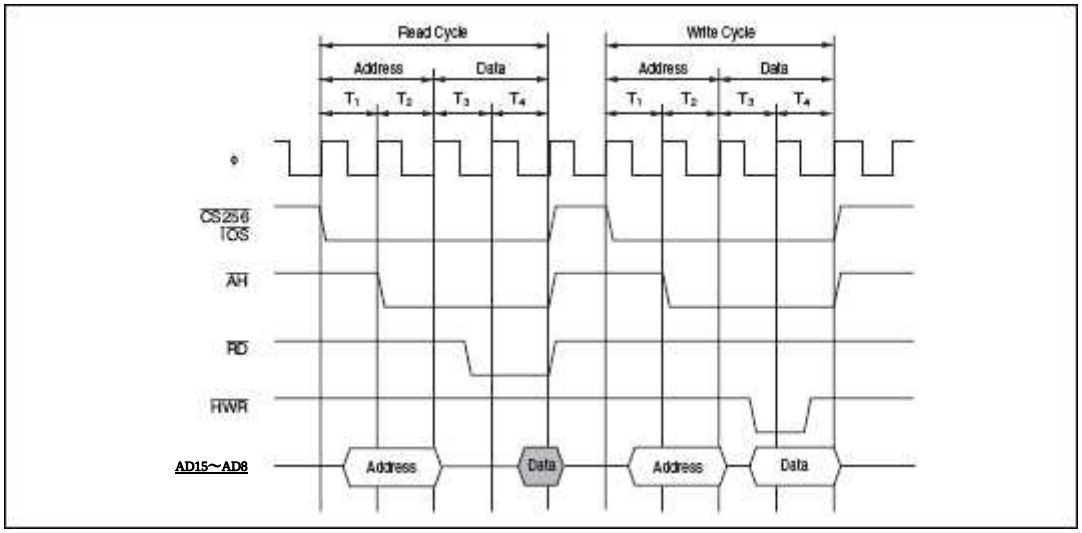

Figure 6.17 Bus Timing for 8-Bit, 2-State Access Space

Section 6.Bus Controller (BSC)

6.5 Bus Interface

6.5.5 Basic Operation Timing in Address-Data Multiplex Extended Mode

[Error]

(2) 8-Bit, 3-State Data Access Space

Figure 6.18 shows the bus timing for an 8-bit, 3-state access space. When an 8-bit access space is accessed, the lower half (AD7 to AD0) of the data bus is used. Wait states can be inserted.

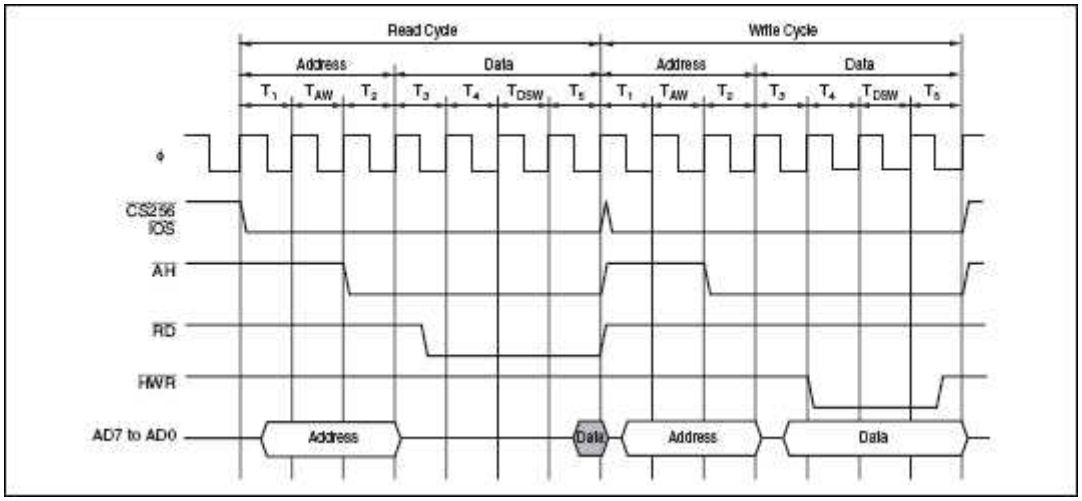

Figure 6.18 Bus Timing for 8-Bit, 3-State Access Space

[Correct]

(2) 8-Bit, 3-State Data Access Space

Figure 6.18 shows the bus timing for an 8-bit, 3-state access space. When an 8-bit access space is accessed, **the upper half (AD15 to AD8)** of the data bus is used. Wait states can be inserted.

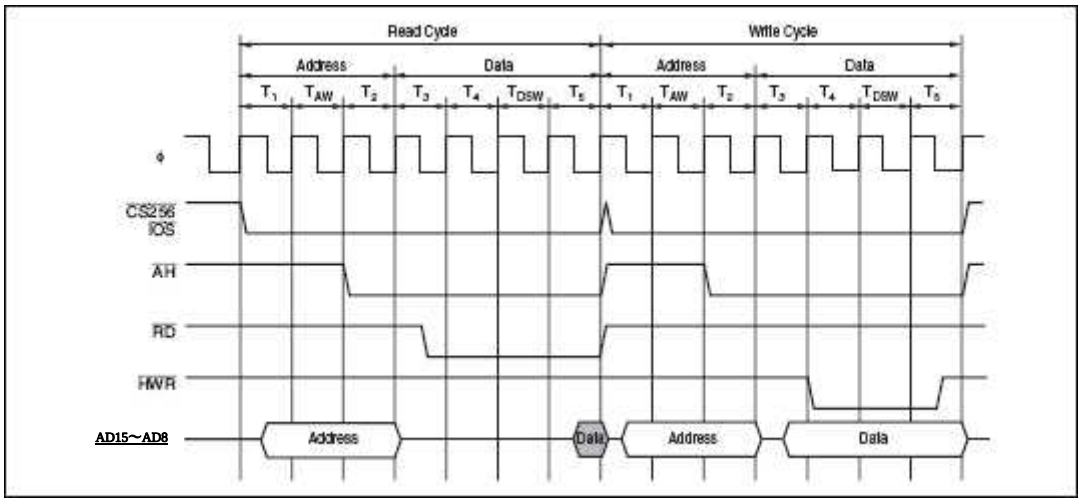

Figure 6.18 Bus Timing for 8-Bit, 3-State Access Space

Section 26. Boundary Scan (JTAG)

26.3 Register Descriptions

26.3.3 Boundary Scan Register (SDBSR)

Table 26.3 Correspondence between Pins and Boundary Scan Register (H8S/2472 Group)

		[Error]		[Correct]				[Error]		[Correct]	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.	Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
		from ETDI				E3	PF6	Input	329	Input	334
								Enable	328	Enable	333
								Output	327	Output	332
A1	VCC	—	—	—	—	E2	NMI	Input	326	Input	331
		—	—	—	—			—	—	—	—
		—	—	—	—			—	—	—	—
C3	P45	Input	345	Input	350	E1	STBY	—	—	—	—
		Enable	344	Enable	349			—	—	—	—
		Output	343	Output	348			—	—	—	—
B1	P46	Input	342	Input	347	F4	NC	—	—	—	—
		Enable	341	Enable	346			—	—	—	—
		Output	340	Output	345			—	—	—	—
C2	P47	Input	339	Input	344	F3	VCL	—	—	—	—
		Enable	338	Enable	343			—	—	—	—
		Output	337	Output	342			—	—	—	—
D3	P56	Input	336	Input	341	F1	MD2	Input	325	Input	330
		Enable	335	Enable	340			—	—	—	—
		Output	334	Output	339			—	—	—	—
C1	P57	Input	333	Input	338	F2	P51	Input	324	Input	329
		Enable	332	Enable	337			Enable	323	Enable	328
		Output	331	Output	336			Output	322	Output	327
D2	VSS	—	—	—	—	G4	P50	Input	321	Input	326
		—	—	—	—			Enable	320	Enable	325
		—	—	—	—			Output	319	Output	324
E4	RES	Input	330	Input	335	G3	P97	Input	318	Input	323
		—	—	—	—			Enable	317	Enable	322
		—	—	—	—			Output	316	Output	321
D1	MD1	—	—	—	—	G1	P96	Input	315	Input	320
		—	—	—	—			Enable	314	Enable	319
		—	—	—	—			Output	313	Output	318

		[Error]		[Correct]				[Error]		[Correct]	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.	Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
G2	P95	Input	312	Input	317	K3	PC5	Input	288	Input	293
		Enable	311	Enable	316			Enable	287	Enable	292
		Output	310	Output	315			Output	286	Output	291
H4	P94	Input	309	Input	314	K1	PC4	Input	285	Input	290
		Enable	308	Enable	313			Enable	284	Enable	289
		Output	307	Output	312			Output	283	Output	288
H3	P93	Input	306	Input	311	K2	PC3	Input	282	Input	287
		Enable	305	Enable	310			Enable	281	Enable	286
		Output	304	Output	309			Output	280	Output	285
H1	NC	—	—	—	—	L3	NC	—	—	—	—
		—	—	—	—			—	—	—	—
		—	—	—	—			—	—	—	—
H2	P92	Input	303	Input	308	L1	PC2	Input	279	Input	284
		Enable	302	Enable	307			Enable	278	Enable	283
		Output	301	Output	306			Output	277	Output	282
J4	P91	Input	300	Input	305	L2	NC	—	—	—	—
		Enable	299	Enable	304			—	—	—	—
		Output	298	Output	303			—	—	—	—
J3	P90	Input	297	Input	302	L4	PC1	Input	276	Input	281
		Enable	296	Enable	301			Enable	275	Enable	280
		Output	295	Output	300			Output	274	Output	279
J1	NC	—	—	—	—	M1	NC	—	—	—	—
		—	—	—	—			—	—	—	—
		—	—	—	—			—	—	—	—
J2	PC7	Input	294	Input	299	M2	PC0	Input	273	Input	278
		Enable	293	Enable	298			Enable	272	Enable	277
		Output	292	Output	297			Output	271	Output	276
K4	PC6	Input	291	Input	296	M3	PA7	Input	270	Input	275
		Enable	290	Enable	295			Enable	269	Enable	274
		Output	289	Output	294			Output	268	Output	273

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
N1	PA6	Input	267	Input	272
		Enable	266	Enable	271
		Output	265	Output	270
M4	PA5	Input	264	Input	269
		Enable	263	Enable	268
		Output	262	Output	267
N2	VCC	—	—	—	—
		—	—	—	—
		—	—	—	—
P1	PA4	Input	261	Input	266
		Enable	260	Enable	265
		Output	259	Output	264
P2	PA3	Input	258	Input	263
		Enable	257	Enable	262
		Output	256	Output	261
R1	NC	—	—	—	—
		—	—	—	—
		—	—	—	—
N3	PA2	Input	255	Input	260
		Enable	254	Enable	259
		Output	253	Output	258
R2	NC	—	—	—	—
		—	—	—	—
		—	—	—	—
P3	PA1	Input	252	Input	257
		Enable	251	Enable	256
		Output	250	Output	255
N4	NC	—	—	—	—
		—	—	—	—
		—	—	—	—

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
R3	PA0	Input	249	Input	254
		Enable	248	Enable	253
		Output	247	Output	252
P4	NC	—	—	—	—
		—	—	—	—
		—	—	—	—
M5	VSS	—	—	—	—
		—	—	—	—
		—	—	—	—
R4	NC	—	—	—	—
		—	—	—	—
		—	—	—	—
N5	P87	Input	246	Input	251
		Enable	245	Enable	250
		Output	244	Output	249
P5	P86	Input	243	Input	248
		Enable	242	Enable	247
		Output	241	Output	246
R5	P85	Input	240	Input	245
		Enable	239	Enable	244
		Output	238	Output	243
M6	P84	Input	237	Input	242
		Enable	236	Enable	241
		Output	235	Output	240
N6	P83	Input	234	Input	239
		Enable	233	Enable	238
		Output	232	Output	237
R6	P82	Input	231	Input	236
		Enable	230	Enable	235
		Output	239	Output	244

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
P6	P81	Input	228	Input	233
		Enable	227	Enable	232
		Output	226	Output	231
M7	P80	Input	225	Input	230
		Enable	224	Enable	229
		Output	223	Output	228
N7	NC	—	—	—	—
		—	—	—	—
		—	—	—	—
R7	PE7	Input	222	Input	227
		Enable	221	Enable	226
		Output	220	Output	225
P7	NC	—	—	—	—
		—	—	—	—
		—	—	—	—
M8	PE6	Input	219	Input	224
		Enable	218	Enable	223
		Output	217	Output	222
N8	PE5	Input	216	Input	221
		Enable	215	Enable	220
		Output	214	Output	219
R8	PE4	Input	213	Input	218
		Enable	212	Enable	217
		Output	211	Output	216
P8	PE3	Input	210	Input	215
		Enable	209	Enable	214
		Output	208	Output	213
M9	PE2	Input	207	Input	212
		Enable	206	Enable	211
		Output	205	Output	210

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
N9	PE1	Input	204	Input	209
		Enable	203	Enable	208
		Output	202	Output	207
R9	PE0	Input	201	Input	206
		Enable	200	Enable	205
		Output	199	Output	204
P9	VCC	—	—	—	—
		—	—	—	—
		—	—	—	—
M10	PD7	Input	198	Input	203
		Enable	197	Enable	202
		Output	196	Output	201
N10	PD6	Input	195	Input	200
		Enable	194	Enable	199
		Output	193	Output	198
R10	PD5	Input	192	Input	197
		Enable	191	Enable	196
		Output	190	Output	195
P10	PD4	Input	189	Input	194
		Enable	188	Enable	193
		Output	187	Output	192
N11	PD3	Input	186	Input	191
		Enable	185	Enable	190
		Output	184	Output	189
R11	PD2	Input	183	Input	188
		Enable	182	Enable	187
		Output	181	Output	186
P11	PD1	Input	180	Input	185
		Enable	179	Enable	184
		Output	178	Output	183

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
M11	PD0	Input	177	Input	182
		Enable	176	Enable	181
		Output	175	Output	180
R12	NC	—	—	—	—
		—	—	—	—
		—	—	—	—
P12	AVSS	—	—	—	—
		—	—	—	—
		—	—	—	—
N12	P70	Input	174	Input	179
		—	—	—	—
		—	—	—	—
R13	P71	Input	173	Input	173
		—	—	—	—
		—	—	—	—
M12	P72	Input	172	Input	177
		—	—	—	—
		—	—	—	—
P13	P73	Input	171	Input	176
		—	—	—	—
		—	—	—	—
R14	P74	Input	170	Input	175
		—	—	—	—
		—	—	—	—
P14	P75	Input	169	Input	174
		—	—	—	—
		—	—	—	—
R15	P76	Input	168	Input	173
		—	—	—	—
		—	—	—	—

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
N13	P77	Input	167	Input	172
		—	—	—	—
		—	—	—	—
P15	AVCC	—	—	—	—
		—	—	—	—
		—	—	—	—
N14	AVref	—	—	—	—
		—	—	—	—
		—	—	—	—
M13	P60	Input	166	Input	171
		Enable	165	Enable	170
		Output	164	Output	169
N15	P61	Input	163	Input	168
		Enable	162	Enable	167
		Output	161	Output	166
M14	P62	Input	160	Input	165
		Enable	159	Enable	164
		Output	158	Output	163
L12	P63	Input	157	Input	162
		Enable	156	Enable	161
		Output	155	Output	160
M15	P64	Input	154	Input	159
		Enable	153	Enable	158
		Output	152	Output	157
L13	P65	Input	151	Input	156
		Enable	150	Enable	155
		Output	149	Output	154
L14	P66	Input	148	Input	153
		Enable	147	Enable	152
		Output	146	Output	151

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
L15	P67	Input	145	Input	150
		Enable	144	Enable	149
		Output	143	Output	148
K12	VCC	—	—	—	—
		—	—	—	—
		—	—	—	—
K13	DrVCC	—	—	—	—
		—	—	—	—
		—	—	—	—
K15	USD-	—	—	—	—
		—	—	—	—
		—	—	—	—
K14	USD+	—	—	—	—
		—	—	—	—
		—	—	—	—
J12	NC	—	—	—	—
		—	—	—	—
		—	—	—	—
J13	DrVSS	—	—	—	—
		—	—	—	—
		—	—	—	—
J15	PUPDPLS	—	—	**Input**	**147**
		—	—	**Enable**	**146**
		Output	142	Output	145
J14	VBUS	—	—	—	—
		—	—	—	—
		—	—	—	—
H12	ETMS	—	—	—	—
		—	—	—	—
		—	—	—	—

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
H13	ETDO	—	—	—	—
		—	—	—	—
		—	—	—	—
H15	ETDI	—	—	—	—
		—	—	—	—
		—	—	—	—
H14	ETCK	—	—	—	—
		—	—	—	—
		—	—	—	—
G12	ETRST	—	—	—	—
		—	—	—	—
		—	—	—	—
G13	PF2	Input	141	Input	144
		Enable	140	Enable	143
		Output	139	Output	142
G15	PF1	Input	138	Input	141
		Enable	137	Enable	140
		Output	136	Output	139
G14	PF0	Input	135	Input	138
		Enable	134	Enable	137
		Output	133	Output	136
F12	NC	—	—	—	—
		—	—	—	—
		—	—	—	—
F13	VSS	—	—	—	—
		—	—	—	—
		—	—	—	—
F15	P27	Input	132	Input	135
		Enable	131	Enable	134
		Output	130	Output	133

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
F14	P26	Input	129	Input	132
		Enable	128	Enable	131
		Output	127	Output	130
E13	P25	Input	126	Input	129
		Enable	125	Enable	128
		Output	124	Output	127
E15	P24	Input	123	Input	126
		Enable	122	Enable	125
		Output	121	Output	124
E14	P23	Input	120	Input	123
		Enable	119	Enable	122
		Output	118	Output	121
E12	P22	Input	117	Input	120
		Enable	116	Enable	119
		Output	115	Output	118
D15	P21	Input	114	Input	117
		Enable	113	Enable	116
		Output	112	Output	115
D14	P20	Input	111	Input	114
		Enable	110	Enable	113
		Output	109	Output	112
D13	P17	Input	118	Input	121
		Enable	107	Enable	110
		Output	106	Output	109
C15	P16	Input	105	Input	108
		Enable	104	Enable	107
		Output	103	Output	106
D12	P15	Input	102	Input	105
		Enable	101	Enable	104
		Output	100	Output	103

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
C14	P14	Input	99	Input	102
		Enable	98	Enable	101
		Output	97	Output	100
B15	P13	Input	96	Input	99
		Enable	95	Enable	98
		Output	94	Output	97
B14	P12	Input	93	Input	96
		Enable	92	Enable	95
		Output	91	Output	94
A15	P11	Input	90	Input	93
		Enable	89	Enable	92
		Output	88	Output	91
C13	VSS	—	—	—	—
		—	—	—	—
		—	—	—	—
A14	P10	Input	87	Input	90
		Enable	86	Enable	89
		Output	85	Output	88
B13	PB7	Input	84	Input	87
		Enable	83	Enable	86
		Output	82	Output	85
C12	PB6	Input	81	Input	84
		Enable	80	Enable	83
		Output	79	Output	82
A13	PB5	Input	78	Input	81
		Enable	77	Enable	80
		Output	76	Output	79
B12	PB4	Input	75	Input	78
		Enable	74	Enable	77
		Output	73	Output	76

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
D11	PB3	Input	72	Input	75
		Enable	71	Enable	74
		Output	70	Output	73
A12	PB2	Input	69	Input	72
		Enable	68	Enable	71
		Output	67	Output	70
C11	PB1	Input	66	Input	69
		Enable	65	Enable	68
		Output	64	Output	67
B11	PB0	Input	63	Input	66
		Enable	62	Enable	65
		Output	61	Output	64
A11	VCC	—	—	—	—
		—	—	—	—
		—	—	—	—
D10	P30	Input	60	Input	63
		Enable	59	Enable	62
		Output	58	Output	61
C10	P31	Input	57	Input	60
		Enable	56	Enable	59
		Output	55	Output	58
A10	P32	Input	54	Input	57
		Enable	53	Enable	56
		Output	52	Output	55
B10	P33	Input	51	Input	54
		Enable	50	Enable	53
		Output	49	Output	52
D9	P34	Input	48	Input	51
		Enable	47	Enable	50
		Output	46	Output	49

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
C9	P35	Input	45	Input	48
		Enable	44	Enable	47
		Output	43	Output	46
A9	P36	Input	42	Input	45
		Enable	41	Enable	44
		Output	40	Output	43
B9	P37	Input	39	Input	42
		Enable	38	Enable	41
		Output	37	Output	40
D8	P40	Input	36	Input	39
		Enable	35	Enable	38
		Output	34	Output	37
C8	P41	Input	33	Input	36
		Enable	32	Enable	35
		Output	31	Output	34
A8	P42	Input	30	Input	33
		Enable	29	Enable	32
		Output	28	Output	31
B8	P43	Input	27	Input	30
		Enable	26	Enable	29
		Output	25	Output	28
D7	PEVref	—	—	—	—
		—	—	—	—
		—	—	—	—
C7	PECI	—	—	**Input**	**27**
		—	—	**Enable**	**26**
		—	—	**Output**	**25**
A7	P52	Input	24	Input	24
		Enable	23	Enable	23
		Output	22	Output	22

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
B7	P53	Input	21	Input	21
		Enable	20	Enable	20
		Output	19	Output	19
D6	FWE	Input	18	Input	18
		—	—	—	—
		—	—	—	—
C6	P54	Input	17	Input	17
		Enable	16	Enable	16
		Output	15	Output	15
A6	P55	Input	14	Input	14
		Enable	13	Enable	13
		Output	12	Output	12
B6	P44	Input	11	Input	11
		Enable	10	Enable	10
		Output	9	Output	9
C5	VCC	—	—	—	—
		—	—	—	—
		—	—	—	—
A5	UXTAL	—	—	—	—
		—	—	—	—
		—	—	—	—
B5	UEXTAL	—	—	—	—
		—	—	—	—
		—	—	—	—
D5	UXSEL	—	—	—	—
		—	—	—	—
		—	—	—	—

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
A4	PF5	Input	8	Input	8
		Enable	7	Enable	7
		Output	6	Output	6
B4	PF4	Input	5	Input	5
		Enable	4	Enable	4
		Output	3	Output	3
C4	NC	—	—	—	—
		—	—	—	—
		—	—	—	—
A3	VSS	—	—	—	—
		—	—	—	—
		—	—	—	—
D4	PF3	Input	2	Input	2
		Enable	1	Enable	1
		Output	0	Output	0
B3	RESO	—	—	—	—
		—	—	—	—
		—	—	—	—
A2	XTAL	—	—	—	—
		—	—	—	—
		—	—	—	—
B2	EXTAL	—	—	—	—
		—	—	—	—
		—	—	—	—
to ETDO					

Section 26. Boundary Scan (JTAG)

26.3 Register Descriptions

26.3.3 Boundary Scan Register (SDBSR)

Table 26.4 Correspondence between Pins and Boundary Scan Register (H8S/2462 Group)

		[Error]		[Correct]				[Error]		[Correct]	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.	Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
		from ETDI				10	PF6	Input	316	Input	319
								Enable	315	Enable	318
								Output	314	Output	317
1	VCC	–	–	–	–	11	NMI	Input	313	Input	316
		–	–	–	–			–	–	–	–
		–	–	–	–			–	–	–	–
2	P45	Input	332	Input	335	12	STBY	–	–	–	–
		Enable	331	Enable	334			–	–	–	–
		Output	330	Output	333			–	–	–	–
3	P46	Input	329	Input	332	13	VCL	–	–	–	–
		Enable	328	Enable	331			–	–	–	–
		Output	327	Output	330			–	–	–	–
4	P47	Input	326	Input	329	14	MD2	Input	312	Input	315
		Enable	325	Enable	328			–	–	–	–
		Output	324	Output	327			–	–	–	–
5	P56	Input	323	Input	326	15	P51	Input	311	Input	314
		Enable	322	Enable	325			Enable	310	Enable	313
		Output	321	Output	324			Output	309	Output	312
6	P57	Input	320	Input	323	16	P50	Input	308	Input	311
		Enable	319	Enable	322			Enable	307	Enable	310
		Output	318	Output	321			Output	306	Output	309
7	VSS	–	–	–	–	17	P97	Input	305	Input	308
		–	–	–	–			Enable	304	Enable	307
		–	–	–	–			Output	303	Output	306
8	RES	–	–	–	–	18	P96	Input	302	Input	305
		–	–	–	–			Enable	301	Enable	304
		–	–	–	–			Output	300	Output	303
9	MD1	Input	317	Input	320	19	P95	Input	299	Input	302
		–	–	–	–			Enable	298	Enable	301
		–	–	–	–			Output	297	Output	300

		[Error]		[Correct]				[Error]		[Correct]	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.	Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
20	P94	Input	296	Input	299	30	PC2	Input	266	Input	269
		Enable	295	Enable	298			Enable	265	Enable	268
		Output	294	Output	297			Output	264	Output	267
21	P93	Input	293	Input	296	31	PC1	Input	263	Input	266
		Enable	292	Enable	295			Enable	262	Enable	265
22	P92	Output	291	Output	294			Output	261	Output	264
		Input	290	Input	293	32	PC0	Input	260	Input	263
		Enable	289	Enable	292			Enable	259	Enable	262
		Output	288	Output	291			Output	258	Output	261
23	P91	Input	287	Input	290	33	PA7	Input	257	Input	260
		Enable	286	Enable	289			Enable	256	Enable	259
		Output	285	Output	288			Output	255	Output	258
24	P90	Input	284	Input	287	34	PA6	Input	254	Input	257
		Enable	283	Enable	286			Enable	253	Enable	256
		Output	282	Output	285			Output	252	Output	255
25	PC7	Input	281	Input	284	35	PA5	Input	251	Input	254
		Enable	280	Enable	283			Enable	250	Enable	253
		Output	279	Output	282			Output	249	Output	252
26	PC6	Input	278	Input	281	36	VCC	—	—	—	—
		Enable	277	Enable	280			—	—	—	—
		Output	276	Output	279			—	—	—	—
27	PC5	Input	275	Input	278	37	PA4	Input	248	Input	251
		Enable	274	Enable	277			Enable	247	Enable	250
		Output	273	Output	276			Output	246	Output	249
28	PC4	Input	272	Input	275	38	PA3	Input	245	Input	248
		Enable	271	Enable	274			Enable	244	Enable	247
		Output	270	Output	273			Output	243	Output	246
29	PC3	Input	269	Input	272	39	PA2	Input	242	Input	245
		Enable	268	Enable	271			Enable	241	Enable	244
		Output	267	Output	270			Output	240	Output	243

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
40	PA1	Input	239	Input	242
		Enable	238	Enable	241
		Output	237	Output	240
41	PA0	Input	236	Input	239
		Enable	235	Enable	238
		Output	234	Output	237
42	VSS	—	—	—	—
		—	—	—	—
		—	—	—	—
43	P87	Input	233	Input	236
		Enable	232	Enable	235
		Output	231	Output	234
44	P86	Input	230	Input	233
		Enable	229	Enable	232
		Output	228	Output	231
45	P85	Input	227	Input	230
		Enable	226	Enable	229
		Output	225	Output	228
46	P84	Input	224	Input	227
		Enable	223	Enable	226
		Output	222	Output	225
47	P83	Input	221	Input	224
		Enable	220	Enable	223
		Output	219	Output	222
48	P82	Input	218	Input	221
		Enable	217	Enable	220
		Output	216	Output	219
49	P81	Input	215	Input	218
		Enable	214	Enable	217
		Output	213	Output	216

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
50	P80	Input	212	Input	215
		Enable	211	Enable	214
		Output	210	Output	213
51	PE7	Input	209	Input	212
		Enable	208	Enable	211
		Output	207	Output	210
52	PE6	Input	206	Input	209
		Enable	205	Enable	208
		Output	204	Output	207
53	PE5	Input	203	Input	206
		Enable	202	Enable	205
		Output	201	Output	204
54	PE4	Input	200	Input	203
		Enable	199	Enable	202
		Output	198	Output	201
55	PE3	Input	197	Input	200
		Enable	196	Enable	199
		Output	195	Output	198
56	PE2	Input	194	Input	197
		Enable	193	Enable	196
		Output	192	Output	195
57	PE1	Input	191	Input	194
		Enable	190	Enable	193
		Output	189	Output	192
58	PE0	Input	188	Input	191
		Enable	187	Enable	190
		Output	186	Output	189
59	PD7	Input	185	Input	188
		Enable	184	Enable	187
		Output	183	Output	186

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
60	PD6	Input	182	Input	185
		Enable	181	Enable	184
		Output	180	Output	183
61	PD5	Input	179	Input	182
		Enable	178	Enable	181
		Output	177	Output	180
62	PD4	Input	176	Input	179
		Enable	175	Enable	178
		Output	174	Output	177
63	PD3	Input	173	Input	176
		Enable	172	Enable	175
		Output	171	Output	174
64	PD2	Input	170	Input	173
		Enable	169	Enable	172
		Output	168	Output	171
65	PD1	Input	167	Input	170
		Enable	166	Enable	169
		Output	165	Output	168
66	PD0	Input	164	Input	167
		Enable	163	Enable	166
		Output	162	Output	165
67	AVSS	—	—	—	—
		—	—	—	—
		—	—	—	—
68	P70	Input	161	Input	164
		—	—	—	—
		—	—	—	—
69	P71	Input	160	Input	163
		—	—	—	—
		—	—	—	—

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
70	P72	Input	159	Input	162
		—	—	—	—
		—	—	—	—
71	P73	Input	158	Input	161
		—	—	—	—
		—	—	—	—
72	P74	Input	157	Input	160
		—	—	—	—
		—	—	—	—
73	P75	Input	156	Input	159
		—	—	—	—
		—	—	—	—
74	P76	Input	155	Input	158
		—	—	—	—
		—	—	—	—
75	P77	Input	154	Input	157
		—	—	—	—
		—	—	—	—
76	AVCC	—	—	—	—
		—	—	—	—
		—	—	—	—
77	Avref	—	—	—	—
		—	—	—	—
		—	—	—	—
78	P60	Input	153	Input	156
		Enable	152	Enable	155
		Output	151	Output	154
79	P61	Input	150	Input	153
		Enable	149	Enable	152
		Output	148	Output	151

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
80	P62	Input	147	Input	150
		Enable	146	Enable	149
		Output	145	Output	148
81	P63	Input	144	Input	147
		Enable	143	Enable	146
		Output	142	Output	145
82	P64	Input	141	Input	144
		Enable	140	Enable	143
		Output	139	Output	142
83	P65	Input	138	Input	141
		Enable	137	Enable	140
		Output	136	Output	139
84	P66	Input	135	Input	138
		Enable	134	Enable	137
		Output	133	Output	136
85	P67	Input	132	Input	135
		Enable	131	Enable	134
		Output	130	Output	133
86	VCC	—	—	—	—
		—	—	—	—
		—	—	—	—
87	ETMS	—	—	—	—
		—	—	—	—
		—	—	—	—
88	ETDO	—	—	—	—
		—	—	—	—
		—	—	—	—
89	ETDI	—	—	—	—
		—	—	—	—
		—	—	—	—

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
90	ETCK	—	—	—	—
		—	—	—	—
		—	—	—	—
91	ETRST	—	—	—	—
		—	—	—	—
		—	—	—	—
92	PF1	Input	129	Input	132
		Enable	128	Enable	131
		Output	127	Output	130
93	PF0	Input	126	Input	129
		Enable	125	Enable	128
		Output	124	Output	127
94	VSS	—	—	—	—
		—	—	—	—
		—	—	—	—
95	P27	Input	123	Input	126
		Enable	122	Enable	125
		Output	121	Output	124
96	P26	Input	120	Input	123
		Enable	119	Enable	122
		Output	118	Output	121
97	P25	Input	117	Input	120
		Enable	116	Enable	119
		Output	115	Output	118
98	P24	Input	114	Input	117
		Enable	113	Enable	116
		Output	112	Output	115
99	P23	Input	111	Input	114
		Enable	110	Enable	113
		Output	109	Output	112

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
100	P22	Input	108	Input	111
		Enable	107	Enable	110
		Output	106	Output	109
101	P21	Input	105	Input	108
		Enable	104	Enable	107
		Output	103	Output	106
102	P20	Input	102	Input	105
		Enable	101	Enable	104
		Output	100	Output	103
103	P17	Input	99	Input	102
		Enable	98	Enable	101
		Output	97	Output	100
104	P16	Input	96	Input	99
		Enable	95	Enable	98
		Output	94	Output	97
105	P15	Input	93	Input	96
		Enable	92	Enable	95
		Output	91	Output	94
106	P14	Input	90	Input	93
		Enable	89	Enable	92
		Output	88	Output	91
107	P13	Input	87	Input	90
		Enable	86	Enable	89
		Output	85	Output	88
108	P12	Input	84	Input	87
		Enable	83	Enable	86
		Output	82	Output	85
109	P11	Input	81	Input	84
		Enable	80	Enable	83
		Output	79	Output	82

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
110	VSS	—	—	—	—
		—	—	—	—
		—	—	—	—
111	P10	Input	78	Input	81
		Enable	77	Enable	80
		Output	76	Output	79
112	PB7	Input	75	Input	78
		Enable	74	Enable	77
		Output	73	Output	76
113	PB6	Input	72	Input	75
		Enable	71	Enable	74
		Output	70	Output	73
114	PB5	Input	69	Input	72
		Enable	68	Enable	71
		Output	67	Output	70
115	PB4	Input	66	Input	69
		Enable	65	Enable	68
		Output	64	Output	67
116	PB3	Input	63	Input	66
		Enable	62	Enable	65
		Output	61	Output	64
117	PB2	Input	60	Input	63
		Enable	59	Enable	62
		Output	58	Output	61
118	PB1	Input	57	Input	60
		Enable	56	Enable	59
		Output	55	Output	58
119	PB0	Input	54	Input	57
		Enable	53	Enable	56
		Output	52	Output	55

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
120	VCC	—	—	—	—
		—	—	—	—
		—	—	—	—
121	P30	Input	51	Input	54
		Enable	50	Enable	53
		Output	49	Output	52
122	P31	Input	48	Input	51
		Enable	47	Enable	50
		Output	46	Output	49
123	P32	Input	45	Input	48
		Enable	44	Enable	47
		Output	43	Output	46
124	P33	Input	42	Input	45
		Enable	41	Enable	44
		Output	40	Output	43
125	P34	Input	39	Input	42
		Enable	38	Enable	41
		Output	37	Output	40
126	P35	Input	36	Input	39
		Enable	35	Enable	38
		Output	34	Output	37
127	P36	Input	33	Input	36
		Enable	32	Enable	35
		Output	31	Output	34
128	P37	Input	30	Input	33
		Enable	29	Enable	32
		Output	28	Output	31
129	P40	Input	27	Input	30
		Enable	26	Enable	29
		Output	25	Output	28

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
130	P41	Input	24	Input	27
		Enable	23	Enable	26
		Output	22	Output	25
131	P42	Input	21	Input	24
		Enable	20	Enable	23
		Output	19	Output	22
132	P43	Input	18	Input	21
		Enable	17	Enable	20
		Output	16	Output	19
133	PEVref	—	—	—	—
		—	—	—	—
		—	—	—	—
134	PECI	—	—	**Input**	**18**
		—	—	**Enable**	**17**
		—	—	**Output**	**16**
135	P52	Input	15	Input	15
		Enable	14	Enable	14
		Output	13	Output	13
136	P53	Input	12	Input	12
		Enable	11	Enable	11
		Output	10	Output	10
137	FWE	Input	9	Input	9
		—	—	–	–
		—	—	–	–
138	P54	Input	8	Input	8
		Enable	7	Enable	7
		Output	6	Output	6
139	P55	Input	5	Input	5
		Enable	4	Enable	4
		Output	3	Output	3

		【Error】		【Correct】	
Pin No.	Pin Name	Input/Output	Bit No.	Input/Output	Bit No.
140	P44	Input	2	Input	2
		Enable	1	Enable	1
		Output	0	Output	0
141	VSS	—	—	–	–
		—	—	–	–
		—	—	–	–
142	RESO	—	—	–	–
		—	—	–	–
		—	—	–	–
143	XTAL	—	—	–	–
		—	—	–	–
		—	—	–	–
144	EXTAL	—	—	–	–
		—	—	–	–
		—	—	–	–

to ETDO

Section 26. Boundary Scan (JTAG)

26.3 Register Descriptions

26.3.3 Boundary Scan Register (SDBSR)

Table 26.5 Correspondence between Pins and Boundary Scan Register (H8S/2463 Group)

Pin No.	Pin Name	Input/Output	Bit No.	Pin No.	Pin Name	Input/Output	Bit No.
				10	PF6	Input	316
		from ETDI				Enable	315
						Output	314
1	VCC	–	–	11	NMI	Input	313
		–	–			–	–
		–	–			–	–
2	P45	Input	332	12	STBY	–	–
		Enable	331			–	–
		Output	330			–	–
3	P46	Input	329	13	VCL	–	–
		Enable	328			–	–
		Output	327			–	–
4	P47	Input	326	14	MD2	Input	312
		Enable	325			–	–
		Output	324			–	–
5	P56	Input	323	15	P51	Input	311
		Enable	322			Enable	310
		Output	321			Output	309
6	P57	Input	320	16	P50	Input	308
		Enable	319			Enable	307
		Output	318			Output	306
7	VSS	–	–	17	P97	Input	305
		–	–			Enable	304
		–	–			Output	303
8	RES	–	–	18	P96	Input	302
		–	–			Enable	301
		–	–			Output	300
9	MD1	Input	317	19	P95	Input	299
		–	–			Enable	298
		–	–			Output	297

Pin No.	Pin Name	Input/Output	Bit No.	Pin No.	Pin Name	Input/Output	Bit No.
20	P94	Input	296	30	PC2	Input	266
		Enable	295			Enable	265
		Output	294			Output	264
21	P93	Input	293	31	PC1	Input	263
		Enable	292			Enable	262
		Output	291			Output	261
22	P92	Input	290	32	PC0	Input	260
		Enable	289			Enable	259
		Output	288			Output	258
23	P91	Input	287	33	PA7	Input	257
		Enable	286			Enable	256
		Output	285			Output	255
24	P90	Input	284	34	PA6	Input	254
		Enable	283			Enable	253
		Output	282			Output	252
25	PC7	Input	281	35	PA5	Input	251
		Enable	280			Enable	250
		Output	279			Output	249
26	PC6	Input	278	36	VCC	—	—
		Enable	277			—	—
		Output	276			—	—
27	PC5	Input	275	37	PA4	Input	248
		Enable	274			Enable	247
		Output	273			Output	246
28	PC4	Input	272	38	PA3	Input	245
		Enable	271			Enable	244
		Output	270			Output	243
29	PC3	Input	269	39	PA2	Input	242
		Enable	268			Enable	241
		Output	267			Output	240

Pin No.	Pin Name	Input/Output	Bit No.	Pin No.	Pin Name	Input/Output	Bit No.
40	PA1	Input	239	50	P80	Input	212
		Enable	238			Enable	211
		Output	237			Output	210
41	PA0	Input	236	51	PE7	Input	209
		Enable	235			Enable	208
		Output	234			Output	207
42	VSS	—	—	52	PE6	Input	206
		—	—			Enable	205
		—	—			Output	204
43	P87	Input	233	53	PE5	Input	203
		Enable	232			Enable	202
		Output	231			Output	201
44	P86	Input	230	54	PE4	Input	200
		Enable	229			Enable	199
		Output	228			Output	198
45	P85	Input	227	55	PE3	Input	197
		Enable	226			Enable	196
		Output	225			Output	195
46	P84	Input	224	56	PE2	Input	194
		Enable	223			Enable	193
		Output	222			Output	192
47	P83	Input	221	57	PE1	Input	191
		Enable	220			Enable	190
		Output	219			Output	189
48	P82	Input	218	58	PE0	Input	188
		Enable	217			Enable	187
		Output	216			Output	186
49	P81	Input	215	59	PD7	Input	185
		Enable	214			Enable	184
		Output	213			Output	183

Pin No.	Pin Name	Input/Output	Bit No.	Pin No.	Pin Name	Input/Output	Bit No.
60	PD6	Input	182	70	P72	Input	159
		Enable	181			—	—
		Output	180			—	—
61	PD5	Input	179	71	P73	Input	158
		Enable	178			—	—
		Output	177			—	—
62	PD4	Input	176	72	P74	Input	157
		Enable	175			—	—
		Output	174			—	—
63	PD3	Input	173	73	P75	Input	156
		Enable	172			—	—
		Output	171			—	—
64	PD2	Input	170	74	P76	Input	155
		Enable	169			—	—
		Output	168			—	—
65	PD1	Input	167	75	P77	Input	154
		Enable	166			—	—
		Output	165			—	—
66	PD0	Input	164	76	AVCC	—	—
		Enable	163			—	—
		Output	162			—	—
67	AVSS	—	—	77	P60	Input	153
		—	—			Enable	152
		—	—			Output	151
68	P70	Input	161	78	P61	Input	150
		—	—			Enable	149
		—	—			Output	148
69	P71	Input	160	79	P62	Input	147
		—	—			Enable	146
		—	—			Output	145

Pin No.	Pin Name	Input/Output	Bit No.	Pin No.	Pin Name	Input/Output	Bit No.
80	P63	Input	144	90	ETRST	—	—
		Enable	143			—	—
		Output	142			—	—
81	P64	Input	141	91	NC	—	—
		Enable	140			—	—
		Output	139			—	—
82	P65	Input	138	92	PF1	Input	129
		Enable	137			Enable	128
		Output	136			Output	127
83	P66	Input	135	93	PF0	Input	126
		Enable	134			Enable	125
		Output	133			Output	124
84	P67	Input	132	94	VSS	—	—
		Enable	131			—	—
		Output	130			—	—
85	VCC	—	—	95	P27	Input	123
		—	—			Enable	122
		—	—			Output	121
86	ETMS	—	—	96	P26	Input	120
		—	—			Enable	119
		—	—			Output	118
87	ETDO	—	—	97	P25	Input	117
		—	—			Enable	116
		—	—			Output	115
88	ETDI	—	—	98	P24	Input	114
		—	—			Enable	113
		—	—			Output	112
89	ETCK	—	—	99	P23	Input	111
		—	—			Enable	110
		—	—			Output	109

Pin No.	Pin Name	Input/Output	Bit No.	Pin No.	Pin Name	Input/Output	Bit No.
100	P22	Input	108	110	VSS	—	—
		Enable	107			—	—
		Output	106			—	—
101	P21	Input	105	111	P10	Input	78
		Enable	104			Enable	77
		Output	103			Output	76
102	P20	Input	102	112	PB7	Input	75
		Enable	101			Enable	74
		Output	100			Output	73
103	P17	Input	99	113	PB6	Input	72
		Enable	98			Enable	71
		Output	97			Output	70
104	P16	Input	96	114	PB5	Input	69
		Enable	95			Enable	68
		Output	94			Output	67
105	P15	Input	93	115	PB4	Input	66
		Enable	92			Enable	65
		Output	91			Output	64
106	P14	Input	90	116	PB3	Input	63
		Enable	89			Enable	62
		Output	88			Output	61
107	P13	Input	87	117	PB2	Input	60
		Enable	86			Enable	59
		Output	85			Output	58
108	P12	Input	84	118	PB1	Input	57
		Enable	83			Enable	56
		Output	82			Output	55
109	P11	Input	81	119	PB0	Input	54
		Enable	80			Enable	53
		Output	79			Output	52

Pin No.	Pin Name	Input/Output	Bit No.
120	VCC	—	—
		—	—
		—	—
121	P30	Input	51
		Enable	50
		Output	49
122	P31	Input	48
		Enable	47
		Output	46
123	P32	Input	45
		Enable	44
		Output	43
124	P33	Input	42
		Enable	41
		Output	40
125	P34	Input	39
		Enable	38
		Output	37
126	P35	Input	36
		Enable	35
		Output	34
127	P36	Input	33
		Enable	32
		Output	31
128	P37	Input	30
		Enable	29
		Output	28
129	P40	Input	27
		Enable	26
		Output	25

Pin No.	Pin Name	Input/Output	Bit No.
130	P41	Input	24
		Enable	23
		Output	22
131	P42	Input	21
		Enable	20
		Output	19
132	P43	Input	18
		Enable	17
		Output	16
133	P52	Input	15
		Enable	14
		Output	13
134	P53	Input	12
		Enable	11
		Output	10
135	FWE	Input	9
		—	—
		—	—
136	P54	Input	8
		Enable	7
		Output	6
137	P55	Input	5
		Enable	4
		Output	3
138	P44	Input	2
		Enable	1
		Output	0
139	NC	—	—
		—	—
		—	—

Pin No.	Pin Name	Input/Output	Bit No.
140	NC	—	—
		—	—
		—	—
141	VSS	—	—
		—	—
		—	—
142	RESO	—	—
		—	—
		—	—
143	XTAL	—	—
		—	—
		—	—
144	EXTAL	—	—
		—	—
		—	—
to ETDO			

Section 29. List of Registers

[Error]

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
SUBMSTPBL	SMSTPB7	SMSTPB6	SMSTPB5	PECI	SCIF	SMSTPB2	LPC	SMSTPB0	SYSTEM

[Correct]

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
SUBMSTPBL	SMSTPB7	SMSTPB6	SMSTPB5	**SMSTPB4**	**SMSTPB3**	SMSTPB2	**SMSTPB1**	SMSTPB0	SYSTEM