# RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

| Product Category | MPU/MCU | | Document No. | TN-RX*-A168B/E | Rev. | 2.00 |
|---|---|---|---|---|---|---|
| Title | Additions of Specifications Regarding the Capacitive Touch Sensing Unit (CTSU) | | Information Category | Technical Notification | | |
| Applicable Product | RX113 Group RX130 Group RX230 Group, RX231 Group | Lot No.  All | Reference Document | RX113 Group User's Manual: Hardware Rev.1.10 (R01UH0448EJ0110) RX130 Group User's Manual: Hardware Rev.1.00 (R01UH0560EJ0100) RX230 Group, RX231 Group User's Manual: Hardware Rev.1.10 (R01UH0496EJ0110) | | |

This document describes additions of specifications to the capacitive touch sensing unit (CTSU) section in User's Manual: Hardware for the applicable products. Accuracy of measurement can be improved more by calibrating the sensor ICO using the following registers and correcting the measured values.

Page and section numbers are based on the RX113 Group. Refer to the table on the last page for the corresponding page and section numbers in the other groups.
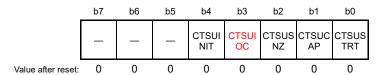
The changes made from TN-RX*-A168A/E to TN-RX*-A168B/E are indicated in blue as shown below.

• Page 1194 of 1458

   The CTSUIOC bit is added to bit 3 in the CTSUCR0 register as follows:

### 35.2.1  CTSU Control register 0 (CTSUCR0)

Address(es):  000A 0900h

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| — | — | — | CTSUI NIT | CTSUI OC | CTSUS NZ | CTSUC AP | CTSUS TRT |

Value after reset: 0 0 0 0 0 0 0 0

| Bit | Symbol | Bit Name | Description | R/W |
|---|---|---|---|---|
| b0 | CTSUSTRT | CTSU Measurement Operation Start | 0: Measurement operation stops 1: Measurement operation starts | R/W |
| b1 | CTSUCAP | CTSU Measurement Operation Start Trigger Select | 0: Software trigger 1: External trigger | R/W |
| b2 | CTSUSNZ | CTSU Wait State Power-Saving Enable | 0: Power-saving function during wait state is disabled 1: Power-saving function during wait state is enabled | R/W |
| b3 | CTSUIOC | CTSU Transmit Pin Control | 0: The TS pins are driven low 1: The TS pins are driven high | R/W |
| b4 | CTSUINIT | CTSU Control Block initialization | Writing 1 to this bit initializes the CTSU control block and registers.[1] This bit is read as 0. | R/W |
| b7 to b5 | — | Reserved | These bits are read as 0. The write value should be 0. | R/W |

**CTSUIOC Bit (CTSU Transmit Pin Control)**

This bit selects the logic level of the TS pin when the CTSUERRS.CTSUTSOD bit is set to 1.

This bit setting is ignored when the CTSUTSOD bit is 0.

- Page 1213 of 1458

The CTSUTSOC, CTSUDRV, CTSUTSOD, and CTSUSPMD[1:0] bits are added to bits 7 and 3 to 0 in the CTSUERRS register as follows:

### 35.2.18   CTSU Error Status Register (CTSUERRS)

Address(es):   000A 091Ch

| b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CTSUI COMP | — | — | — | — | — | — | — | CTSUT SOC | — | — | — | CTSUD RV | CTSUT SOD | CTSUSPMD [1:0] | |

Value after reset:

| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

| Bit | Symbol | Bit Name | Description | R/W |
|---|---|---|---|---|
| b1, b0 | CTSUSPMD[1:0] | Calibration Mode | b1 b0<br>0  0: Capacitance measurement mode<br>0  1: Setting prohibited<br>1  0: Calibration mode<br>1  1: Setting prohibited | R/W |
| b2 | CTSUTSOD | TS Pin Fixed Output | 0: Capacitance measurement mode<br>1: TS pins are forced to be high or low | R/W |
| b3 | CTSUDRV | Calibration Setting 1 | 0: Capacitance measurement mode<br>1: Calibration setting 1 | R/W |
| b6 to b4 | — | Reserved | These bits are read as 0. The write value should be 0. | R/W |
| b7 | CTSUTSOC | Calibration Setting 2 | 0: Capacitance measurement mode<br>1: Calibration setting 2 | R/W |
| b14 to b8 | — | Reserved | These bits are read as 0. The write value should be 0. | R/W |
| b15 | CTSUICOMP | TSCAP Voltage Error Monitor | 0: Normal TSCAP voltage<br>1: Abnormal TSCAP voltage | R |

**CTSUSPMD[1:0] Bit (Calibration Mode)**

These bits are used to calibrate the CTSU.

When measuring the capacitance, set these bits to 00b.

**CTSUTSOD bit (TS Pin Fixed Output)**

This bit is used to calibrate the CTSU. When setting this bit to 1, the TS pins are forced to the logic level specified by the CTSUCR0.CTSUIOC bit.

When measuring the capacitance, set this bit to 0.

**CTSUDRV bit (Calibration Setting 1)**

This bit is used to calibrate the CTSU.

When measuring the capacitance, set this bit to 0.

**CTSUTSOC bit (Calibration Setting 2)**
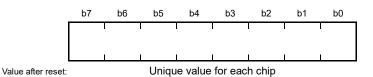
This bit is used to calibrate the CTSU.

When measuring capacitance, set this bit to 0.

• Page 1213 of 1488 (only for RX113 group and RX130 group)

The CTSUTRMR register is added to section 35.2 as follows:

### 35.2.19　CTSU Reference Current Calibration Register (CTSUTRMR)

Address(es):　007F FFBEh

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |

Value after reset:　　　　　　　　Unique value for each chip

The CTSUTRMR resister stores a reference current value calibrated under the specified condition for each chip at factory shipment.

When rewriting this register, set the CTSUERRS.CTSUSPMD[1:0] bits to 10b (calibration mode). When resetting the MCU, the values returns to the factory setting value.

Do not rewrite this register when the CTSUSPMD[1:0] bits are 00b (capacitance measurement mode).

### Reference Documents

| Applicable Product | Manual | Rev. | Document Number | Section Number (Page Number) |
|---|---|---|---|---|
| RX230 Group RX231 Group | RX230 Group, RX231 Group User's Manual: Hardware | Rev.1.10 | R01UH0496EJ0110 | 42.2.1 (page 1623) 42.2.18 (page 1642) |
| RX130 Group | RX130 Group User's Manual: Hardware | Rev.1.00 | R01UH0560EJ0100 | 31.2.1 (page 995) 31.2.18 (page 1014) |

End of document