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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A123A/E	Rev.	1.00
Title	Addition usage notes to Manual regarding the Resets and the Clock Generation Circuit in the RX64M Grourp		Information Category	Technical Notification		
Applicable Product	RX64M Group	Lot No. All	Reference Document	RX64M Group User's Manual Hardware Rev 1.00 (R01UH0377EJ0100)		

This document describes to addition usage notes to section 6.Resets、9. Clock Generation Circuit in RX64M Group User's Manual:

Hardware

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6.4 Usage Notes is added as follows:

After correction

6.4 Usage Notes

6.4.1 Notes on Using Power-On Reset and PLL Circuit Together

When using a power-on reset and the PLL circuit together, set the LVD1CR1.LVD1IDTSEL[1:0] bits or LVD2CR1.LVD2IDTSEL[1:0] bits to 01b, and select the voltage monitoring interrupt to be generated when a drop (Vcc < Vdet) is detected.

In addition, at the beginning of the interrupt handling routine, set the SCKCR3.CKSEL[2:0] bits to a value other than 100b to select a clock source other than the PLL circuit, then set the PLLCR2.PLLEN bit to 1 to stop the PLL circuit.

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9.10.7 Notes is added to 9.10 Usage Notes as follows.

After correction

9.10.7 Notes on Using Power-On Reset and PLL Circuit Together

When using a power-on reset and the PLL circuit together, set the LVD1CR1.LVD1IDTSEL[1:0] bits or LVD2CR1.LVD2IDTSEL[1:0] bits to 01b, and select the voltage monitoring interrupt to be generated when a drop (Vcc < Vdet) is detected.

In addition, at the beginning of the interrupt handling routine, set the SCKCR3.CKSEL[2:0] bits to a value other than 100b to select a clock source other than the PLL circuit, then set the PLLCR2.PLLEN bit to 1 to stop the PLL circuit.