To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-740-A111A/E	Rev.	1.00
Title	Additional Explanation on Interrupts		Information Category	Technical Notification		
Applicable Product	740 Family	Lot No.	Reference Document			

This update provides additional explanation on interrupt request generation, acceptance, and processing in the datasheet.

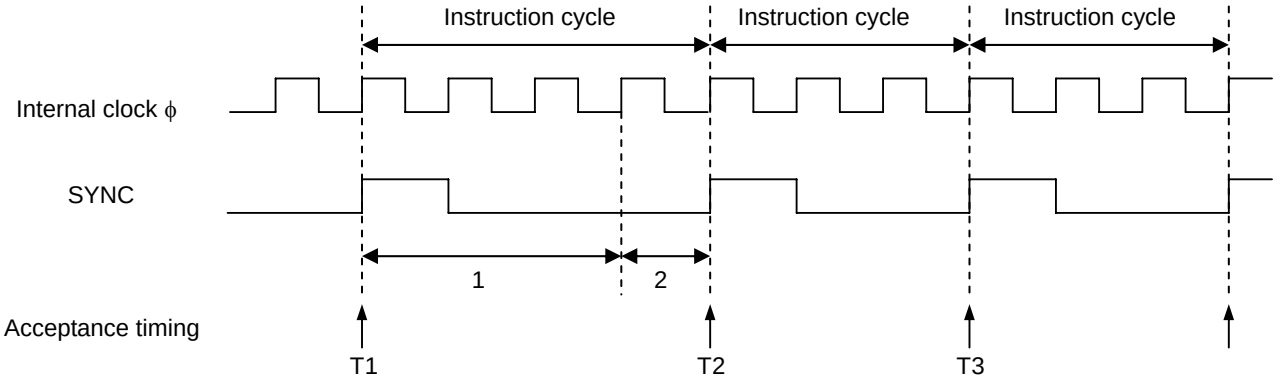
An interrupt can be divided into three phases: i.e., interrupt request generation, interrupt acceptance, and interrupt processing. When an interrupt request is generated, the interrupt block accepts it and sets the corresponding interrupt request flag. Upon detecting this flag, interrupt processing is executed.

Interrupt request generation and interrupt acceptance timings are shown in Figure 1.

An interrupt is accepted at the interrupt acceptance timing in each instruction cycle.

Even when multiple interrupt requests are simultaneously generated, if their interrupt acceptance timings are different (Figure 1 (ii)), the first accepted interrupt is processed regardless of the priority level.

When multiple interrupt requests are accepted at the same interrupt timing, they are processed in the order of their priority levels.



NOTE: Period 2 indicates the last ϕ cycle during one instruction cycle.

i. An interrupt request generated during period 1 is accepted at timing T2.
ii. An interrupt request generated during period 2 is accepted at timing T2 or T3.
Acceptance timings vary depending on conditions.

Figure 1. Interrupt Request Generation and Interrupt Acceptance Timings

For example, when multiple interrupt requests are generated during the period 2 above, the acceptance timing may be T2 for a lower priority interrupt and T3 for a higher priority interrupt. In this case, the lower priority interrupt is processed first.