**Product Category** | **MPU/MCU** | **Document No.** | **TN-RA*-A0087A/E** | **Rev.** | **1.00**
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Title | Addition of usage for Cache | Information Category | Technical Notification | Lot No. | All
| Applicable Product | RA6M4 Group, RA6M5 Group, RA6E1 Group, RA6E2 Group, RA6T2 Group, RA6T3 Group, RA4M3 Group, RA4E2 Group, RA4T1 Group | Reference Document | Refer table at the end of this document

The description about cache information is added as follows.

14.8.4.3 Cacheability for RA6M4, RA6M5
14.6.4.3 Cacheability for RA6E1, RA4M3
13.6.4.3 Cacheability for RA6T2, RA6E2, RA6T3, RA4E2, RA4T1

When the cache is enabled, the cacheability attribute is determined from the Cortex-M default system address map or by using an Arm MPU exclude 0x2800_0000 to 0x2FFF_FFFF area which is always treated as non-cacheable regardless of the default system address map or Arm MPU setting.

When using the default system address map, the cacheable attribution is determined as following:

- 0x0000_0000 to 0x27FF_FFFF: Cacheable
- 0x2800_0000 to 0x2FFF_FFFF: Non-cacheable
- 0x3000_0000 to 0x3FFF_FFFF: Cacheable
- 0x4000_0000 to 0x5FFF_FFFF: Non-cacheable
- 0x6000_0000 to 0x9FFF_FFFF: Cacheable
- 0xA000_0000 to 0xFFFF_FFFF: Non-cacheable

Note. It is recommended to use below MAIR_ATTR method for determining QSPI I/O register area if you use QSPI.

When not using the default system address map, MAIR_ATTR used for each MPU region decides the cacheable attribution as following:

- MAIR_ATTR[7:4] = 0b0000: Non-cacheable (Device memory)
- MAIR_ATTR[7:4] = 0b0100: Non-cacheable (Normal memory)
- MAIR_ATTR[7:4] = 0b1010: Cacheable

Other settings are not supported in the MCU.

Note. In case of accessing following areas, the area must be set to non-cacheable.

- Peripheral I/O register area (0x4000_0000 to 0x5FFF_FFFF)
  - for RA6M4, RA6M5, RA6E1, RA6E2, RA6T2, RA6T3, RA4M3, RA4E2, RA4T1
- QSPI I/O register area (0x6400_0000 to 0x67FF_FFFF)
  - for RA6M4, RA6M5, RA4M3, RA6E2

References
ARM®v8-M Architecture Reference Manual
## Reference Document Table

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