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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A167A/E	Rev.	1.00
Title	Addition Regarding the Description on A/D Sampling State Register 01 (ADSSTR01) of 12-Bit A/D Converter (S12ADa)		Information Category	Technical Notification		
Applicable Product	RX630 Group, RX63N Group, RX631 Group	Lot No. All Lots	Reference Document	See below “Reference Documents”		

This document describes an addition regarding the description on A/D Sampling State Register 01 (ADSSTR01) of 12-Bit A/D Converter (S12ADa) in the user’s manual: Hardware.

The description is added as follows to “SST1[7:0] Bits (Sampling Time 1 Setting)” in A/D Sampling State Register 01 (ADSSTR01).

[Before Correction]

SST1[7:0] Bits (Sampling Time 1 Setting)

These bits are used to set the sampling time for the analog input of the selected channel.

One state refers to one cycle of the A/D conversion clock (ADCLK), so when the frequency of the clock is 50 MHz, one state becomes 20 ns. The default setting is 20 states. The sampling time can be adjusted if the source impedance of the analog input signal is high enough that the sampling time is too short or the ADCLK frequency is too low for the current setting. Only set the SST1[7:0] bits while the ADSCR.ADST bit is 0.

The sampling time setting should be in the range from 10 to 255 states, so that the sampling time is longer than 0.4 µs.

[After Correction]

SST1[7:0] Bits (Sampling Time 1 Setting)

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The sampling time setting should be in the range from 10 to 255 states, so that the sampling time is longer than 0.4 µs, for channels AN008 to AN020. The sampling state of the channels AN000 to AN007 is fixed to 20 states.

[Reference Documents]

Group	Title	Rev.	Document No.	Object page
RX630	RX630 Group User’s Manual: Hardware	1.60	R01UH0040EJ0160	1427
RX63N, RX631	RX63N Group, RX631 Group User’s Manual: Hardware	1.80	R01UH0041EJ0180	1729