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# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-RA*-A0108A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Addition of note for Slave Bus Control Register in Buses chapter | | Information Category | Technical Notification | | |
| Applicable Product | RA4E1 Group<br>RA4M2 Group | Lot No.<br>All | Reference Document | Renesas RA4E1 Group User's Manual: Hardware Rev.1.10<br>Renesas RA4M2 Group User's Manual: Hardware Rev.1.30 | | |

Note for Slave Bus Control Register in Buses chapter is added.

14.3.3 BUSSCNT<slave> : Slave Bus Control Register (<slave> = FHBIU, FLBIU, S0BIU, EQBIU)

Note: While both of the following two conditions are met, the CPU may occupy the bus and DMAC/DTC data transfer may not be prioritized.

- Condition 1

  DMAC/DTC accesses FHBIU, FLBIU, S0BIU, EQBIU, and CPU fetches instructions from the same BUS slaves.

- Condition 2

  CPU instruction fetch loops through a specific address. For example, waiting time by software.

  Example:
  ```
  loop1:subs r0,#1
  cmp r0,#0
  bne loop1
  ```

To avoid this problem, set DMAC/DTC access bus and CPU instruction fetch to different BUS Slaves.

Example: DMAC/DTC accesses S0BIU (SRAM0 or Standby RAM), and CPU fetches instructions from FHBIU.

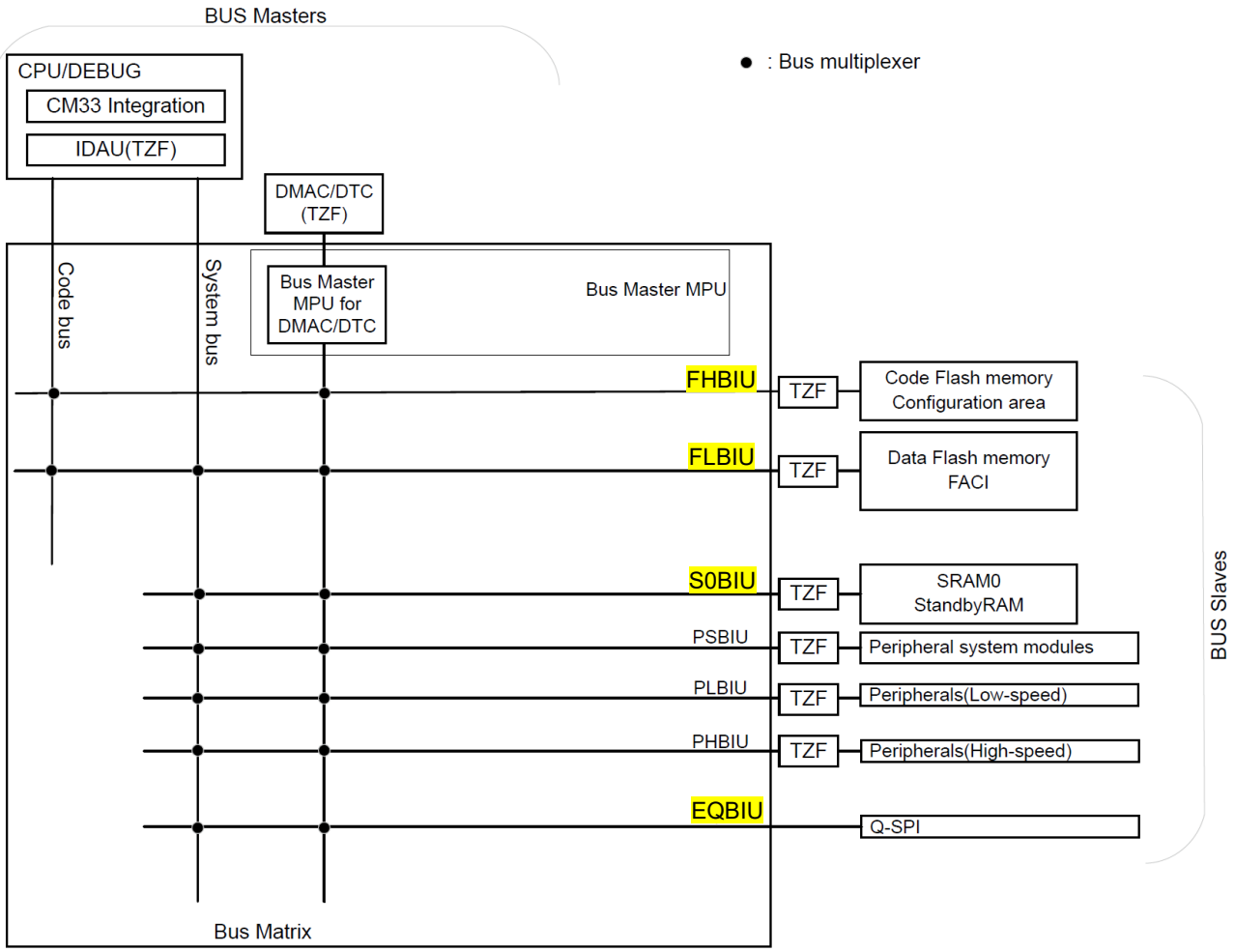


**Figure 14.1 Bus Connection**

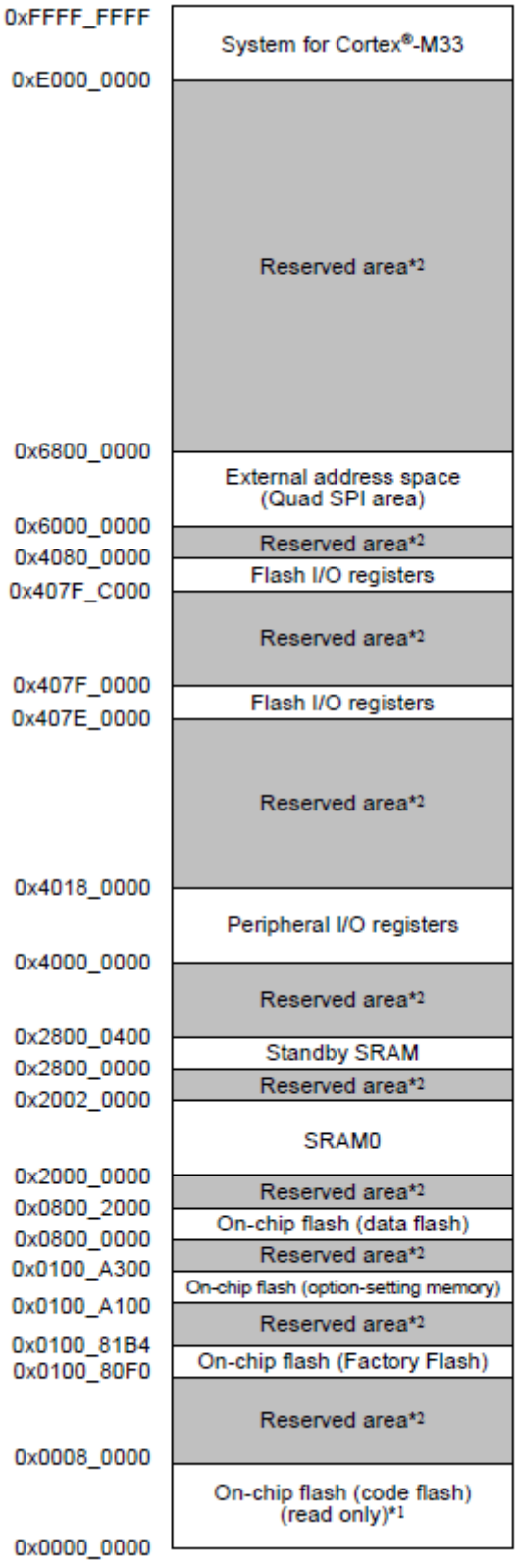


Figure 4.1 Memory map