The HOCOCR2 register for control of the HOCO clock is added, and the functional description related to the HOCOCR2 register is modified.

Table 1 Applicable products

<table>
<thead>
<tr>
<th>Product</th>
<th>RA6M4</th>
<th>RA6M5</th>
<th>RA6M2</th>
<th>RA6E2</th>
<th>RA4M2</th>
<th>RA4M3</th>
<th>RA4E1</th>
<th>RA4E2</th>
<th>RA6M1</th>
<th>RA6M2</th>
<th>RA6M3</th>
<th>RA6M4</th>
<th>RA6E1</th>
<th>RA6E2</th>
<th>RA6T2</th>
<th>RA6T1</th>
<th>RA4M1</th>
<th>RA4M2</th>
<th>RA4E1</th>
<th>RA4E2</th>
<th>RA6W1</th>
<th>RA4W1</th>
</tr>
</thead>
</table>

1. Added HOCOCR2 register.
2. Modified description NONSEC02 bit in CGFSAR.
5. Modified description of System Clock (ICLK) section in Clock Generation Circuit chapter.
6. Modified description of Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD) in Clock Generation Circuit chapter.
7. Modified description of FlashIF Clock (FCLK) section in Clock Generation Circuit chapter.
8. Modified description of External Bus Clock (BCLK) section in Clock Generation Circuit chapter.
9. Modified description of External Pin Output Clock (CLKOUT) section in Clock Generation Circuit chapter.
10. Modified description HOCCEN bit in Option Function Select Register 1.
11. Added HOCOCR2 to register protected by PCR0 bit in PRCR.
1. Added HOCOCR2 register.

- (RA6M4, RA6M5, RA6E1, RA6E2, RA6T2, RA4M2, RA4M3, RA4E1, RA4E2)

   **HOCOCR2**: High-Speed On-Chip Oscillator Control Register2

   **Base address**: SYSC = 0x4001_E000

   **Offset address**: 0x037

   **Bit position**: 7 6 5 4 3 2 1 0

   **Bit field**: 

   - 7:0: HCFRQ[1:0]  
     HOCO Frequency Setting
     - 00: 16MHz
     - 01: 18MHz
     - 10: 20MHz
     - 11: Setting prohibited

   **Value after reset**: 0 0 0 0 0 0 0 1 0 1

   **Notes**:
   - Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
   - If the security attribution is configured as secure:
     - Secure access and Non-secure read access are allowed
     - Non-secure write access is ignored, and TrustZone access error is not generated.
   - If the security attribution is configured as Non-secure:
     - Secure and Non-secure access are allowed

   **Note 1**: Value after reset of the HCFRQ[1:0] bits depend on OFS1.HOCOFRO[1:0] bits.

   The HOCOCR2 register controls the HOCO clock.

   Writing to the HOCOCR2 is prohibited when the HOCOCR.HCSTP bit is 0 (the HOCO operates).

- (RA6M1, RA6M2, RA6M3, RA6T1)

   **HOCOCR2**: High-Speed On-Chip Oscillator Control Register2

   **Base address**: SYSC = 0x4001_E000

   **Offset address**: 0x037

   **Bit position**: 7 6 5 4 3 2 1 0

   **Bit field**: 

   - 7:0: HCFRQ[1:0]  
     HOCO Frequency Setting
     - 00: 16MHz
     - 01: 18MHz
     - 10: 20MHz
     - 11: Setting prohibited

   **Value after reset**: 0 0 0 0 0 0 0 1 0 1

   **Notes**:
   - Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
   - Value after reset of the HCFRQ[1:0] bits depend on OFS1.HOCOFRO[1:0] bits.

   The HOCOCR2 register controls the HOCO clock.

   Writing to the HOCOCR2 is prohibited when the HOCOCR.HCSTP bit is 0 (the HOCO operates).
### (RA4M1, RA4W1)

#### HOCOCR2 : High-Speed On-Chip Oscillator Control Register2

- **Base address:** SYSC = 0x4001_E000
- **Offset address:** 0x037

<table>
<thead>
<tr>
<th>Bit position</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit field</td>
<td>–</td>
<td>–</td>
<td></td>
<td>–</td>
<td>–</td>
<td></td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>

#### Base address:
SYSC = 0x4001_E000
Offset address: 0x037

#### Bit position:

<table>
<thead>
<tr>
<th>Bit position</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit field</td>
<td>–</td>
<td>–</td>
<td>HCFRQ[2:0]</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>

#### Value after reset:

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- **Data format:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
<th>Description</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b2 to b0</td>
<td>–</td>
<td>–</td>
<td>These bits are read as 0. The write value should be 0.</td>
<td>R/W</td>
</tr>
<tr>
<td>b5 to b3</td>
<td>HCFRQ[2:0]</td>
<td>HOCO Frequency Setting 1</td>
<td>000: 24MHz 010: 32MHz 100: 48MHz 101: 64MHz Settings other than above are prohibited.</td>
<td>R/W</td>
</tr>
<tr>
<td>b7 to b6</td>
<td>–</td>
<td>–</td>
<td>These bits are read as 0. The write value should be 0.</td>
<td>R/W</td>
</tr>
</tbody>
</table>

#### Notes:
- Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The HOCOCR2 register controls the HOCO clock.
Writing to the HOCOCR2 is prohibited when the HOCOCR.HCSTP bit is 0 (the HOCO operates).
2. Modified description NONSEC02 bit in CGFSAR.

- (RA6M4, RA6M5, RA6E1, RA6E2, RA4M2, RA4M3, RA4E1, RA4E2) 8.2.1 CGFSAR : Clock Generation Function Security Attribute Register

### Before

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>NONSEC02</td>
<td>Non Secure Attribute bit 02</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Target register: HOCOCR, FLLCR1, FLLCR2, HOCOUTCR
Target factor: HOCO
0: Secure
1: Non Secure

(OMITTED SOME PARTS)

**NONSEC02 bit (Non Secure Attribute bit 02)**
This bit controls the security attribute of HOCOCR, FLLCR1, FLLCR2, HOCOUTCR.

### After

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>NONSEC02</td>
<td>Non Secure Attribute bit 02</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Target register: HOCOCR, HOCOCR2, FLLCR1, FLLCR2, HOCOUTCR
Target factor: HOCO
0: Secure
1: Non Secure

(OMITTED SOME PARTS)

**NONSEC02 bit (Non Secure Attribute bit 02)**
This bit controls the security attribute of HOCOCR, HOCOCR2, FLLCR1, FLLCR2, HOCOUTCR.

- (RA6T2) 8.2.1 CGFSAR : Clock Generation Function Security Attribute Register

### Before

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>NONSEC02</td>
<td>Non Secure Attribute bit 02</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Target register: HOCOCR, HOCOUTCR
Target factor: HOCO
0: Secure
1: Non Secure

(OMITTED SOME PARTS)

**NONSEC02 bit (Non Secure Attribute bit 02)**
This bit controls the security attribute of HOCOCR, HOCOUTCR.

### After

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>NONSEC02</td>
<td>Non Secure Attribute bit 02</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Target register: HOCOCR, HOCOCR2, HOCOUTCR
Target factor: HOCO
0: Secure
1: Non Secure

(OMITTED SOME PARTS)

**NONSEC02 bit (Non Secure Attribute bit 02)**
This bit controls the security attribute of HOCOCR, HOCOCR2, HOCOUTCR.
### 3. Modified description HOCOCR register.

- **(RA6M4, RA6M5)** 8.2.12 HOCOCR : High-Speed On-Chip Oscillator Control Register
  - **(RA6E1, RA4M2, RA4M3, RA4E1)** 8.2.11 HOCOCR : High-Speed On-Chip Oscillator Control Register
  - **(RA6T2)** 8.2.10 HOCOCR : High-Speed On-Chip Oscillator Control Register
  - **(RA6E2, RA4E2)** 8.2.9 HOCOCR : High-Speed On-Chip Oscillator Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>HCSTP</td>
<td>HOCO Stop</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Operate the HOCO clock $^2$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Stop the HOCO clock</td>
<td></td>
</tr>
<tr>
<td>7:1</td>
<td></td>
<td>These bits are read as 0. The write value should be 0.</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**Note:** Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

**Note:** If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

**Note:** If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If you are using the HOCO (HCSTP = 0), set the OFS1.HOCOFREQ0[1:0] bit to an optimum value.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>HCSTP</td>
<td>HOCO Stop</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Operate the HOCO clock $^2$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Stop the HOCO clock</td>
<td></td>
</tr>
<tr>
<td>7:1</td>
<td></td>
<td>These bits are read as 0. The write value should be 0.</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**Note:** Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

**Note:** If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

**Note:** If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If you are using the HOCO (HCSTP = 0), set the OFS1.HOCOFREQ0[1:0] bit to an optimum value.

**Note:** The value of OFS1.HOCOFREQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] even if OFS1.HOCOFREQ0[1:0] is not appropriate value.

- **(RA6M1, RA6M2, RA6T1)** 9.2.10 High-Speed On-Chip Oscillator Control Register (HOCOCR)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>HCSTP</td>
<td>HOCO Stop</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Operate the HOCO clock $^2$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Stop the HOCO clock</td>
<td></td>
</tr>
<tr>
<td>b7 to b1</td>
<td>—</td>
<td>Reserved</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**Note:** Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

**Note:** If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

**Note:** If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If you use the HOCO (HCSTP = 0), you must set the OFS1.HOCOFREQ0[1:0] bits to an optimum value.

**Note:** The value of OFS1.HOCOFREQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] even if OFS1.HOCOFREQ0[1:0] is not appropriate value.
### (RA6M3) 9.2.10 High-Speed On-Chip Oscillator Control Register (HOCOCR)

#### [before]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
<th>Description</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>HCSTP</td>
<td>HOCO Stop</td>
<td>0: Operate the HOCO clock⁷</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Stop the HOCO clock.</td>
<td></td>
</tr>
</tbody>
</table>

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If you are using the HOCO (HCSTP = 0), you must set the OFS1.HOCOFRQ0[1:0] bits to an optimum value.

<table>
<thead>
<tr>
<th>b7 to b1</th>
<th>—</th>
<th>Reserved</th>
<th>These bits are read as 0. The write value should be 0.</th>
<th>R/W</th>
</tr>
</thead>
</table>

#### [after]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
<th>Description</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>HCSTP</td>
<td>HOCO Stop</td>
<td>0: Operate the HOCO clock⁷</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Stop the HOCO clock.</td>
<td></td>
</tr>
</tbody>
</table>

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If you are using the HOCO (HCSTP = 0), you must set the OFS1.HOCOFRQ0[1:0] bits to an optimum value.

Note 3. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] even if OFS1.HOCOFRQ0[1:0] is not appropriate value.

### (RA4M1) 8.2.9 High-Speed On-Chip Oscillator Control Register (HOCOCR)

#### [before]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
<th>Description</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>HCSTP</td>
<td>HOCO Stop</td>
<td>0: Operate the HOCO clock⁷</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Stop the HOCO clock.</td>
<td></td>
</tr>
</tbody>
</table>

Note: Writing to OPCCR.OPCM[1:0] is prohibited while HOCOCR.HCSTP = 0 and OSCSF.HOCOSF = 0 (HOCO is in stabilization wait counting).

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If the operating frequency of HOCO is 48 MHz, VCC must be more than 1.8 V (VCC ≥ 1.8 V) when operating the HOCO.

Note 3. When using the HOCO (HCSTP = 0), the OFS1.HOCOFRQ1 bit must be set to an optimum value. During low-voltage mode, HOCOCR.HCSTP must always be 0.

Note: Writing HCSTP is prohibited while OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of operating power control mode) or FLSTOP.CFLSTOPF = 1 (during transition of flash).

<table>
<thead>
<tr>
<th>b7 to b1</th>
<th>—</th>
<th>Reserved</th>
<th>These bits are read as 0. The write value should be 0.</th>
<th>R/W</th>
</tr>
</thead>
</table>

#### [after]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
<th>Description</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>HCSTP</td>
<td>HOCO Stop</td>
<td>0: Operate the HOCO clock⁷</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Stop the HOCO clock.</td>
<td></td>
</tr>
</tbody>
</table>

Note: Writing to OPCCR.OPCM[1:0] is prohibited while HOCOCR.HCSTP = 0 and OSCSF.HOCOSF = 0 (HOCO is in stabilization wait counting).

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If the operating frequency of HOCO is 48 MHz, VCC must be more than 1.8 V (VCC ≥ 1.8 V) when operating the HOCO.

Note 3. When using the HOCO (HCSTP = 0), the OFS1.HOCOFRQ1 bit must be set to an optimum value. During low-voltage mode, HOCOCR.HCSTP must always be 0.

Note: Writing HCSTP is prohibited while OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of operating power control mode) or FLSTOP.CFLSTOPF = 1 (during transition of flash).

Note 4. The value of OFS1.HOCOFRQ1[2:0] bits is automatically transferred to HOCOCR2.HCFRQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ1[2:0] even if OFS1.HOCOFRQ1[2:0] is not appropriate value.
High-Speed On-Chip Oscillator Control Register (HOCOCR)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
<th>Description</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>HCSTP</td>
<td>HOCO Stop</td>
<td>0: Operate the HOCO clock(^*)(^1)(^4)</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Stop the HOCO clock.</td>
<td></td>
</tr>
<tr>
<td>b7 to b1</td>
<td>—</td>
<td>Reserved</td>
<td>These bits are read as 0. The write value should be 0.</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Note: Writing to OPCCR.OPCM[1:0] is prohibited while HOCOCR.HCSTP = 0 and OSCSF.HOCOSF = 0 (HOCO is in stabilization wait counting).

Note: Writing HCSTP is prohibited while OPCCR.OPCM = 1 or SOPCCR.SOPCM = 1 (during transition of operating power control mode) or FLSTOP.CFLSTOPF = 1 (during transition of flash).

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If the operating frequency of HOCO is 48 MHz, VCC must be more than 1.8 V (VCC ≥ 1.8 V) when operating the HOCO. If the operating frequency of HOCO is 64 MHz, VCC must be more than 2.4 V (VCC ≥ 2.4 V) when operating the HOCO.

Note 3. When using the HOCO (HCSTP = 0), the OFS1.HOCOFREQ1 bit must be set to an optimum value. During low-voltage mode, HOCOCR.HCSTP bit must always be 0.

---

Bit | Symbol | Function | Description | R/W |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>HCSTP</td>
<td>HOCO Stop</td>
<td>0: Operate the HOCO clock(^*)(^1)(^4)</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Stop the HOCO clock.</td>
<td></td>
</tr>
<tr>
<td>b7 to b1</td>
<td>—</td>
<td>Reserved</td>
<td>These bits are read as 0. The write value should be 0.</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Note: Writing to OPCCR.OPCM[1:0] is prohibited while HOCOCR.HCSTP = 0 and OSCSF.HOCOSF = 0 (HOCO is in stabilization wait counting).

Note: Writing HCSTP is prohibited while OPCCR.OPCM = 1 or SOPCCR.SOPCM = 1 (during transition of operating power control mode) or FLSTOP.CFLSTOPF = 1 (during transition of flash).

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If the operating frequency of HOCO is 48 MHz, VCC must be more than 1.8 V (VCC ≥ 1.8 V) when operating the HOCO. If the operating frequency of HOCO is 64 MHz, VCC must be more than 2.4 V (VCC ≥ 2.4 V) when operating the HOCO.

Note 3. When using the HOCO (HCSTP = 0), the OFS1.HOCOFREQ1 bit must be set to an optimum value. During low-voltage mode, HOCOCR.HCSTP bit must always be 0.

Note 4. The value of OFS1.HOCOFREQ1[2:0] bits is automatically transferred to HOCOCR2.HCFOREQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFOREQ1[2:0] even if OFS1.HOCOFREQ1[2:0] is not appropriate value.

- (RA6M4, RA6M5)
  8.2.15 FLLCR2 : FLL Control Register2
- (RA6E1, RA4M2, RA4M3, RA4E1)
  8.2.14 FLLCR2 : FLL Control Register2
- (RA6E2, RA4E2)
  8.2.12 FLLCR2 : FLL Control Register2

### before

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Function</th>
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</tr>
</thead>
<tbody>
<tr>
<td>10:0</td>
<td>FLLCNTL[10:0]</td>
<td>FLL Multiplication Control</td>
<td>R/W</td>
</tr>
</tbody>
</table>

- When OFS1.HOCOFREQ[1:0] is 00b (16MHz), these bits must be set to 0x1E9.
- When OFS1.HOCOFREQ[1:0] is 01b (18MHz), these bits must be set to 0x226.
- When OFS1.HOCOFREQ[1:0] is 10b (20MHz), these bits must be set to 0x263.
- Other settings are prohibited.

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</thead>
<tbody>
<tr>
<td>15:11</td>
<td></td>
<td>These bits are read as 0. The write value should be 0.</td>
<td>R/W</td>
</tr>
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</table>

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- Other settings are prohibited.

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</table>

### Note 1
The value of OFS1.HOCOFREQ[1:0] bits is automatically transferred to HOCOCR2.HCFREQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFREQ0[1:0].

- (RA6M1, RA6M2, RA6M3)
  9.2.14 FLL Control Register 2 (FLLCR2)
- (RA6T1)
  8.2.12 FLL Control Register 2 (FLLCR2)

### before

<table>
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<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit name</th>
<th>Description</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit10 to bit00</td>
<td>FLLCNTL[10:0]</td>
<td>FLL Multiplication Control</td>
<td>R/W</td>
<td></td>
</tr>
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</table>

- When OFS1.HOCOFREQ[1:0] is 00b (16 MHz), these bits must be set to 1E9h.
- When OFS1.HOCOFREQ[1:0] is 01b (18 MHz), these bits must be set to 226h.
- When OFS1.HOCOFREQ[1:0] is 10b (20 MHz), these bits must be set to 263h.
- Other settings are prohibited.

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<td>These bits are read as 0. The write value should be 0.</td>
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- When OFS1.HOCOFREQ[1:0] is 00b (16 MHz), these bits must be set to 1E9h.
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- Other settings are prohibited.

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<tr>
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<td></td>
<td>.</td>
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<td>R/W</td>
</tr>
</tbody>
</table>

Note 1 The value of OFS1.HOCOFREQ[1:0] bits is automatically transferred to HOCOCR2.HCFREQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFREQ0[1:0].
5. Modified description of System Clock (ICLK) section in Clock Generation Circuit chapter.

● (RA6M4, RA6M5, RA6E2, RA4M3, RA4E2) 8.7.1 System Clock (ICLK)

[before]

[after]
The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, the PLLMUL[5:0] bits and PLIDIV[1:0] bits in PLLCCR, and the HOFCOFRQ[1:0] bits in OFS1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ[1:0] bits is automatically transferred to HOCCR2.HCFRQ[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCCR2.HCFRQ[1:0] bits.

● (RA6E1, RA4M2, RA4E1) 8.7.1 System Clock (ICLK)

[before]
The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, and the HOFCOFRQ[1:0] bits in OFS1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ[1:0] bits is automatically transferred to HOCCR2.HCFRQ[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCCR2.HCFRQ[1:0] bits.

● (RA6M1, RA6T1) 9.7.1 System Clock (ICLK)

[before]
The ICLK frequency is specified in the following bits:
- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOFCOFRQ[1:0] bits in OFS1.

[after]
The ICLK frequency is specified in the following bits:
- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOFCOFRQ[1:0] bits in OFS1.

The value of OFS1.HOCOFRQ[1:0] bits is automatically transferred to HOCCR2.HCFRQ[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCCR2.HCFRQ[1:0] bits.

● (RA6M2, RA6M3) 9.7.1 System Clock (ICLK)

[before]
Specify the frequency in the following bits:
- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOFCOFRQ[1:0] bits in OFS1.

[after]
Specify the frequency in the following bits:
- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOFCOFRQ[1:0] bits in OFS1.

The value of OFS1.HOCOFRQ[1:0] bits is automatically transferred to HOCCR2.HCFRQ[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCCR2.HCFRQ[1:0] bits.
8.7.1 System Clock (ICLK)

Before

The ICLK frequency is specified in the following bits:

- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2

After

The ICLK frequency is specified in the following bits:

- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2

The value of OFS1.HOCOFREQ[2:0] bits is automatically transferred to HOCOCR2.HCFREQ[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFREQ[2:0] bits.

9.8.1 System Clock (ICLK)

Before

The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, the PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2, and the HOCOFREQ[2:0] bits in OFS1.

After

The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, the PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2, and the HOCOFREQ[2:0] bits in OFS1.

The value of OFS1.HOCOFREQ[2:0] bits is automatically transferred to HOCOCR2.HCFREQ[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFREQ[2:0] bits.
6. Modified description of Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD) in Clock Generation Circuit chapter.

- (RA6M4, RA6E1, RA6E2, RA4M3, RA4E1, RA4E2) 8.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

**[before]**
The frequency of the given clock is specified in the following bits:
- PCKA[2:0], PCKB[2:0], PCKC[2:0] and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ[0:1] bits in OFS1.

**[after]**
The frequency of the given clock is specified in the following bits:
- PCKA[2:0], PCKB[2:0], PCKC[2:0] and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ[0:1] bits in OFS1.

*1 Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ[0:1] bits is automatically transferred to HOCCCR2.HCFRQ[0:1] bits after reset, therefore HOCO frequency can also be specified by HOCCCR2.HCFRQ[0:1] bits.

- (RA6M5) 8.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

**[before]**
The frequency of the given clock is specified in the following bits:
- PCKA[2:0], PCKB[2:0], PCKC[2:0] and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ[0:1] bits in OFS1.

**[after]**
The frequency of the given clock is specified in the following bits:
- PCKA[2:0], PCKB[2:0], PCKC[2:0] and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ[0:1] bits in OFS1.

*1 Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ[0:1] bits is automatically transferred to HOCCCR2.HCFRQ[0:1] bits after reset, therefore HOCO frequency can also be specified by HOCCCR2.HCFRQ[0:1] bits.

- (RA4M2) 8.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

**[before]**
The frequency of the given clock is specified in the following bits:
- PCKA[2:0], PCKB[2:0], PCKC[2:0], PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ[0:1] bits in OFS1.

**[after]**
The frequency of the given clock is specified in the following bits:
- PCKA[2:0], PCKB[2:0], PCKC[2:0], PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ[0:1] bits in OFS1.

*1 Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ[0:1] bits is automatically transferred to HOCCCR2.HCFRQ[0:1] bits after reset, therefore HOCO frequency can also be specified by HOCCCR2.HCFRQ[0:1] bits.
The frequency of the given clock is specified in the following bits:
- PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFREQ[1:0] bits in OFS1.

Note 1. The value of OFS1.HOCOFREQ[1:0] bits is automatically transferred to HOCOCR2.HCFREQ[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFREQ[1:0] bits.

The frequency of the given clock is specified in the following bits:
- PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFREQ[1:0] bits in OFS1.

Note 1. The value of OFS1.HOCOFREQ[1:0] bits is automatically transferred to HOCOCR2.HCFREQ[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFREQ[1:0] bits.

The frequency of the given clock is specified in the following bits:
- PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[4:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFREQ[1:0] bits in OFS1.

Note 1. The value of OFS1.HOCOFREQ[1:0] bits is automatically transferred to HOCOCR2.HCFREQ[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFREQ[1:0] bits.
7. Modified description of FlashIF Clock (FCLK) section in Clock Generation Circuit chapter.

- (RA6M4, RA6E1, RA6E2, RA4M2, RA4M3, RA4E1, RA4E2) 8.7.3 FlashIF Clock (FCLK)
- (RA6T2) 8.6.3 FlashIF Clock (FCLK)

[before]
The FCLK frequency is specified in the following bits:
- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]
The FCLK frequency is specified in the following bits:
- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

*1 Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- (RA6M5) 8.7.3 FlashIF Clock (FCLK)

[before]
The FCLK frequency is specified in the following bits:
- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]
The FCLK frequency is specified in the following bits:
- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

*1 Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- (RA6M1, RA6T1) 9.7.3 Flash Interface Clock (FCLK)

[before]
The FCLK frequency is specified in the following bits:
- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]
The FCLK frequency is specified in the following bits:
- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

*1 Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.
9.7.3 Flash Interface Clock (FCLK)

Before
Specify the frequency in the following bits:
- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFREQ0[1:0] bits in OFS1.

After
Specify the frequency in the following bits:
- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFREQ0[1:0] bits in OFS1.

Note 1. The value of OFS1.HOCOFREQ0[1:0] bits is automatically transferred to HOCOCR2.HCFREQ0[1:0] bits after reset, therefore HOC frequency can also be specified by HOCOCR2.HCFREQ0[1:0] bits.

8.7.3 Flash Interface Clock (FCLK)

Before
The FCLK frequency is specified in the following bits:
- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[4:0] and PLIDIV[1:0] bits in PLLCCR2

After
The FCLK frequency is specified in the following bits:
- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[4:0] and PLIDIV[1:0] bits in PLLCCR2

Note 1. The value of OFS1.HOCOFREQ1[2:0] bits is automatically transferred to HOCOCR2.HCFREQ1[2:0] bits after reset, therefore HOC frequency can also be specified by HOCOCR2.HCFREQ1[2:0] bits.
8. Modified description of External Bus Clock (BCLK) section in Clock Generation Circuit chapter.

- **(RA6M4)** 8.7.4 External Bus Clock (BCLK)

[before]
Specify the frequency in the following bits:
- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]
Specify the frequency in the following bits:
- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6M5)** 8.7.4 External Bus Clock (BCLK)

[before]
Specify the frequency in the following bits:
- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]
Specify the frequency in the following bits:
- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6M1)** 9.7.4 External Bus Clock (BCLK)

[before]
The BCLK frequency is specified in the following bits:
- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]
The BCLK frequency is specified in the following bits:
- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.
(RA6M2, RA6M3) 9.7.4 External Bus Clock (BCLK)

[before]
Specify the frequency in the following bits:
- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFREQ0[1:0] bits in OFS1.

[after]
Specify the frequency in the following bits:
- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFREQ0[1:0] bits in OFS1.

Note 1. The value of OFS1.HOCOFREQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.
9. Modified description of External Pin Output Clock (CLKOUT) section in Clock Generation Circuit chapter.

- (RA6M4, RA6T2) 8.7.13 External Pin Output Clock (CLKOUT)
- (RA6M5) 8.7.17 External Pin Output Clock (CLKOUT)
- (RA6E2, RA4E2) 8.7.12 External Pin Output Clock (CLKOUT)
- (RA4M3) 8.7.11 External Pin Output Clock (CLKOUT)

[before]
The CLKOUT clock frequency is specified in the following bits:
- CKODIV[2:0] bits or CKOSEL[2:0] bits in CKOCR
- HOCFRQ[1:0] bits in OFS1

[after]
The CLKOUT clock frequency is specified in the following bits:
- CKODIV[2:0] bits or CKOSEL[2:0] bits in CKOCR
- HOCFRQ[1:0] bits in OFS1

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ[1:0] bits is automatically transferred to HOCOCR2.HCFRQ[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ[1:0] bits.

- (RA6E1, RA4M2, RA4E1) 8.7.11 External Pin Output Clock (CLKOUT)

[before]
The CLKOUT clock frequency is specified in the following bits:
- CKODIV[2:0] or CKOSEL[2:0] in CKOCR
- HOCFRQ[1:0] bits in OFS1

[after]
The CLKOUT clock frequency is specified in the following bits:
- CKODIV[2:0] or CKOSEL[2:0] in CKOCR
- HOCFRQ[1:0] bits in OFS1

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ[1:0] bits is automatically transferred to HOCOCR2.HCFRQ[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ[1:0] bits.

- (RA6M1, RA6T1) 9.7.12 Clock/Buzzer Output Clock (CLKOUT)

[before]
The CLKOUT frequency is specified in the following bits:
- CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR
- HOCFRQ[1:0] bits in OFS1

[after]
The CLKOUT frequency is specified in the following bits:
- CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR
- HOCFRQ[1:0] bits in OFS1

Note 1. The value of OFS1.HOCOFRQ[1:0] bits is automatically transferred to HOCOCR2.HCFRQ[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ[1:0] bits.

- (RA6M2) 9.7.13 Clock/Buzzer Output Clock (CLKOUT)
- (RA6M3) 9.7.14 Clock/Buzzer Output Clock (CLKOUT)

[before]
Specify the frequency in the following bits:
- CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR
- HOCFRQ[1:0] bits in OFS1

[after]
Specify the frequency in the following bits:
- CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR
- HOCFRQ[1:0] bits in OFS1

Note 1. The value of OFS1.HOCOFRQ[1:0] bits is automatically transferred to HOCOCR2.HCFRQ[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ[1:0] bits.
● (RA4M1)  8.7.12 Clock/Buzzer Output Clock (CLKOUT)
  (RA4W1)  9.8.12 Clock/Buzzer Output Clock (CLKOUT)

[before]
The CLKOUT clock frequency is specified in the following bits:
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2

[after]
The CLKOUT clock frequency is specified in the following bits:
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2

*Note 1.* The value of OFS1.HOCOFREQ1[2:0] bits is automatically transferred to HOCOCR2.HCFRQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ1[2:0] bits.
10. Modified description HOCOEN bit in Option Function Select Register 1.

- **(RA6M4, RA6M5)** 6.2.4 OFS1, OFS1_SEC, OFS1_SEL : Option Function Select Register 1
  
  (RA4M3) 6.2.3 OFS1, OFS1_SEC, OFS1_SEL : Option Function Select Register 1

[before] HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the HOCO Frequency Setting 0 bits (OFS1.HOCOFRQ0[1:0]) to an optimum value.

[after] HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the HOCO Frequency Setting 0 bits (OFS1.HOCOFRQ0[1:0]) to an optimum value.

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits when OFS1.HOCOEN=1.

- **(RA6E1, RA6E2, RA4E2)** 6.2.4 OFS1, OFS1_SEC, OFS1_SEL : Option Function Select Register 1
  
  (RA6T2, RA4M2, RA4E1) 6.2.3 OFS1, OFS1_SEC, OFS1_SEL : Option Function Select Register 1

[before] HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFRQ0 bit to an optimum value.

[after] HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFRQ0 bit to an optimum value.

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits when OFS1.HOCOEN=1.
7.2.2 Option Function Select Register 1 (OFS1)

**HOCOEN bit (HOCO Oscillation Enable)**

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFREQ[1:0] bits to an optimum value.

**[after]**

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFREQ[1:0] bits to an optimum value.

**Note 1.** The value of OFS1.HOCOFREQ[1:0] bits is automatically transferred to HOCOCR2.HCFREQ[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFREQ[1:0] bits when OFS1.HOCOEN=1.

---

**[RA6M3]** 7.2.2 Option Function Select Register 1 (OFS1)

**HOCOEN bit (HOCO Oscillation Enable)**

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). If you use the HOCO clock, you must set the OFS1.HOCOFREQ[1:0] bits to an optimum value.

**[after]**

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the clock source select bits (SCKSCR.CKSEL[2:0]). If you use the HOCO clock, you must set the OFS1.HOCOFREQ[1:0] bits to an optimum value.

**Note 1.** The value of OFS1.HOCOFREQ[1:0] bits is automatically transferred to HOCOCR2.HCFREQ[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFREQ[1:0] bits when OFS1.HOCOEN=1.

---

**[RA4M1]** 6.2.2 Option Function Select Register 1 (OFS1)

**HOCOEN bit (HOCO Oscillation Enable)**

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is switched to HOCO only by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, set the OFS1.HOCOFREQ1 bit to an optimum value.

**[after]**

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is switched to HOCO only by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, set the OFS1.HOCOFREQ1 bit to an optimum value.

**Note 1.** The value of OFS1.HOCOFREQ1[2:0] bits is automatically transferred to HOCOCR2.HCFREQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFREQ1[2:0] bits when OFS1.HOCOEN=1.
7.2.2 Option Function Select Register 1 (OFS1)

**HOCOEN bit (HOCO Oscillation Enable)**

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFREQ1 bit to an optimum value.

---

**Note 1.** The value of OFS1.HOCOFREQ1[2:0] bits is automatically transferred to HOCOCR2.HCFREQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFREQ1[2:0] bits when OFS1.HOCOEN=1.
### 11. Added HOCCOCR2 to register protected by PCR0 bit in PRCR.

#### (RA6M4, RA6E1)

Table 12.1 Association between the bits in the PRCR register and registers to be protected

<table>
<thead>
<tr>
<th>Bit</th>
<th>Register to be protected</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PRC0</strong></td>
<td>Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCCOCR, HOCCOCR2, MOCOCR, FLLCR1, FLLCR2, CKOCR, TRCKCR, OSTDSCR, OSTDSCR, PLL2CCR, PLL2CR, EBKOCR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, OCTACKDIVCR, USBCKCR, OCTACKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR</td>
</tr>
</tbody>
</table>

#### [after]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Register to be protected</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PRC0</strong></td>
<td>Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCCOCR, HOCCOCR2, MOCOCR, FLLCR1, FLLCR2, CKOCR, TRCKCR, OSTDSCR, OSTDSCR, PLL2CCR, PLL2CR, EBKOCR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, OCTACKDIVCR, USBCKCR, OCTACKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR</td>
</tr>
</tbody>
</table>

#### (RA6M5)

Table 12.1 Association between the bits in the PRCR register and registers to be protected

<table>
<thead>
<tr>
<th>Bit</th>
<th>Register to be protected</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PRC0</strong></td>
<td>Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCCOCR, HOCCOCR2, MOCOCR, FLLCR1, FLLCR2, CKOCR, OSTDSCR, OSTDSCR, PLL2CCR, PLL2CR, EBKOCR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, OCTACKDIVCR, CANFDCKDIVCR, USB60CKDIVCR, CECCDKDIVCR, USBCKCR, OCTACKCR, CANFDCKCR, USB60CKCR, CECCCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR</td>
</tr>
</tbody>
</table>

#### [after]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Register to be protected</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PRC0</strong></td>
<td>Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCCOCR, HOCCOCR2, MOCOCR, FLLCR1, FLLCR2, CKOCR, OSTDSCR, OSTDSCR, PLL2CCR, PLL2CR, EBKOCR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, OCTACKDIVCR, CANFDCKDIVCR, USB60CKDIVCR, CECCDKDIVCR, USBCKCR, OCTACKCR, CANFDCKCR, USB60CKCR, CECCCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR</td>
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</tbody>
</table>

#### (RA6E2, RA4E2)

Table 11.1 Association between the bits in the PRCR register and registers to be protected

<table>
<thead>
<tr>
<th>Bit</th>
<th>Register to be protected</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PRC0</strong></td>
<td>Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCCOCR, MOCOCR, FLLCR1, FLLCR2, CKOCR, OSTDSCR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, OCTACKDIVCR, USBCKCR, OCTACKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR</td>
</tr>
</tbody>
</table>

#### [after]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Register to be protected</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PRC0</strong></td>
<td>Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCCOCR, HOCCOCR2, MOCOCR, FLLCR1, FLLCR2, CKOCR, OSTDSCR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, OCTACKDIVCR, USBCKCR, OCTACKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR</td>
</tr>
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</table>
### Table 1

#### Association between the bits in the PRCR register and registers to be protected

<table>
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<tr>
<th>PRCR bit</th>
<th>Register to be protected</th>
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<tbody>
<tr>
<td><strong>PRC0</strong></td>
<td>Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCCOCR, MOCOCR, FLLCR1, FLLCR2, CKOCR, TRCKCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, USBCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR</td>
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<table>
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<th>PRCR bit</th>
<th>Register to be protected</th>
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<tbody>
<tr>
<td><strong>PRC0</strong></td>
<td>Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCCOCR, HOCCOCR2, MOCOCR, FLLCR1, FLLCR2, CKOCR, TRCKCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, USBCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR</td>
</tr>
</tbody>
</table>

#### (RA4M2, RA4M3, RA4E1)

Table 12.1 Association between the bits in the PRCR register and registers to be protected

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<th>PRCR bit</th>
<th>Register to be protected</th>
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<tbody>
<tr>
<td><strong>PRC0</strong></td>
<td>Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCCOCR, MOCOCR, FLLCR1, FLLCR2, CKOCR, TRCKCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, USBCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR</td>
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</tbody>
</table>

#### (RA6T2)

Table 11.1 Association between the bits in the PRCR register and registers to be protected

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<tr>
<th>PRCR bit</th>
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<tbody>
<tr>
<td><strong>PRC0</strong></td>
<td>Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCCOCR, MOCOCR, CKOCR, OSTDCR, OSTDSR, PLL2CR, PLL2CR, MOCOUTCR, HOCOUTCR, SCISPICKDIVCR, CANFDCKDIVCR, GPTCKDIVCR, IICCKDIVCR, SCISPICKCR, CANFDCKCR, GPTCKCR, IICCKCR, MOSCWTCR, MOMCR, LOCOCR, LOCOUTCR</td>
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#### (RA6M1)

Table 13.1 Association between PRCR bits and registers to be protected

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<tbody>
<tr>
<td><strong>PRC0</strong></td>
<td>Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCCOCR, MOCOCR, TRCKCR, OSTDCR, OSTDSR, PLL2CR, PLL2CR, MOCOUTCR, HOCOUTCR, SCISPICKDIVCR, CANFDCKDIVCR, GPTCKDIVCR, IICCKDIVCR, SCISPICKCR, CANFDCKCR, GPTCKCR, IICCKCR, MOSCWTCR, MOMCR, LOCOCR, LOCOUTCR</td>
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**RENESAS TECHNICAL UPDATE**  
**TN-RA*^-A0083A/E**  
Date: Jun. 12, 2023
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<tr>
<td>PRC0</td>
<td>- Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, EBCKOCR, SDCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCCOWTCR, PLLCR1, PLLCR2</td>
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### Table 12.1 Association between PRCR bits and registers to be protected

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<td>PRC0</td>
<td>- Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, EBCKOCR, SDCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCCOWTCR, PLLCR1, PLLCR2</td>
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<td>PRC0</td>
<td>- Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, EBCKOCR, SDCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCCOWTCR, PLLCR1, PLLCR2</td>
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<td>- Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, SLCDSCKCR, EBCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, USBCKCR</td>
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<td>PRC0</td>
<td>- Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, SLCDSCKCR, EBCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, USBCKCR</td>
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Table 13.1 Association between PRCR bits and registers to be protected

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Reference Document Table

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