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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0083A/E	Rev.	1.00
Title	Addition of HOCOCR2 register for HOCO clock control		Information Category	Technical Notification		
Applicable Product	RA6M1 group, RA6M2 group, RA6M3 group, RA6M4 group, RA6M5 group, RA6E1 group, RA6E2 group, RA6T1 group, RA6T2 group, RA4M1 group, RA4M2 group, RA4M3 group, RA4E1 group, RA4E2 group, RA4W1 group	Lot No. All	Reference Document	Refer table at the end of this document		

The HOCOCR2 register for control of the HOCO clock is added, and the functional description related to the HOCOCR2 register is modified.

Table 1 Applicable products Table

Product	RA6M4	RA6M5	RA6E1	RA6E2	RA6T2	RA4M2	RA4M3	RA4E1	RA4E2	RA6M1	RA6M2	RA6M3	RA6T1	RA4M1	RA4W1
CPU	Cortex-M33									Cortex-M4					
1. Added HOCOCR2 register.	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
2. Modified description NONSEC02 bit in CGFSAR.	✔	✔	✔	✔	✔	✔	✔	✔	✔	-	-	-	-	-	-
3. Modified description HOCOCR register.	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
4. Modified description FLLCNTL[10:0] bits in FLLCR2.	✔	✔	✔	✔	-	✔	✔	✔	✔	✔	✔	✔	✔	-	-
5. Modified description of System Clock (ICLK) section in Clock Generation Circuit chapter.	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
6. Modified description of Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD) in Clock Generation Circuit chapter.	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
7. Modified description of FlashIF Clock (FCLK) section in Clock Generation Circuit chapter.	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
8. Modified description of External Bus Clock (BCLK) section in Clock Generation Circuit chapter.	✔	✔	-	-	-	-	-	-	-	✔	✔	✔	-	-	-
9. Modified description of External Pin Output Clock (CLKOUT) section in Clock Generation Circuit chapter.	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
10. Modified description HOCOEN bit in Option Function Select Register 1.	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
11. Added HOCOCR2 to register protected by PCR0 bit in PRCR.	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔

1. Added HOCOCR2 register.

- **(RA6M4, RA6M5, RA6E1, RA6E2, RA6T2, RA4M2, RA4M3, RA4E1, RA4E2)**

HOCOCR2 : High-Speed On-Chip Oscillator Control Register2

Base address: SYSC = 0x4001_E000

Offset address: 0x037

Bit position:	7	6	5	4	3	2	1	0
Bit field:	–	–	–	–	–	–	HCFRQ0[1:0]	
Value after reset:	0	0	0	0	0	0	0/1*1	0/1*1

Bit	Symbol	Function	R/W
1:0	HCFRQ0[1:0]	HOCO Frequency Setting 0 00: 16MHz 01: 18MHz 10: 20MHz 11: Setting prohibited	R/W
7:2	–	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Value after reset of the HCFRQ0[1:0] bits depend on OFS1.HOCOFRQ0[1:0] bits.

The HOCOCR2 register controls the HOCO clock.
Writing to the HOCOCR2 is prohibited when the HOCOCR.HCSTP bit is 0 (the HOCO operates).

- **(RA6M1, RA6M2, RA6M3, RA6T1)**

HOCOCR2 : High-Speed On-Chip Oscillator Control Register2

Base address: SYSC = 0x4001_E000

Offset address: 0x037

Bit position:	7	6	5	4	3	2	1	0
Bit field:	–	–	–	–	–	–	HCFRQ0[1:0]	
Value after reset:	0	0	0	0	0	0	0/1*1	0/1*1

Bit	Symbol	Function	Description	R/W
b1 to b0	HCFRQ0[1:0]	HOCO Frequency Setting 0	00: 16MHz 01: 18MHz 10: 20MHz 11: Setting prohibited	R/W
b7 to b2	–	–	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. Value after reset of the HCFRQ0[1:0] bits depend on OFS1.HOCOFRQ0[1:0] bits.

The HOCOCR2 register controls the HOCO clock.
Writing to the HOCOCR2 is prohibited when the HOCOCR.HCSTP bit is 0 (the HOCO operates).

- **(RA4M1, RA4W1)**

HOCOCR2 : High-Speed On-Chip Oscillator Control Register2

Base address: SYSC = 0x4001_E000

Offset address: 0x037

Bit position:	7	6	5	4	3	2	1	0
Bit field:	–	–	HCFRQ1[2:0]			–	–	–
Value after reset:	0	0	0/1*1	0/1*1	0/1*1	0	0	0

Bit	Symbol	Function	Description	R/W
b2 to b0	–	–	These bits are read as 0. The write value should be 0.	R/W
b5 to b3	HCFRQ1[2:0]	HOCO Frequency Setting 1	000: 24MHz 010: 32MHz 100: 48MHz 101: 64MHz Settings other than above are prohibited.	R/W
b7 to b6	–	–	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. Value after reset of the HCFRQ1[2:0] bits depend on OFS1.HOCOFRQ1[2:0] bits.

The HOCOCR2 register controls the HOCO clock.
Writing to the HOCOCR2 is prohibited when the HOCOCR.HCSTP bit is 0 (the HOCO operates).

2. Modified description NONSEC02 bit in CGFSAR.

- **(RA6M4, RA6M5, RA6E1, RA6E2, RA4M2, RA4M3, RA4E1, RA4E2)** 8.2.1 CGFSAR : Clock Generation Function Security Attribute Register

[before]

Bit	Symbol	Function	R/W
2	NONSEC02	Non Secure Attribute bit 02 Target register: HOCOCR, FLLCR1, FLLCR2, HOCOUTCR Target factor: HOCO 0: Secure 1: Non Secure	R/W

(Omitted some parts)

NONSEC02 bit (Non Secure Attribute bit 02)
This bit controls the security attribute of HOCOCR, FLLCR1, FLLCR2, HOCOUTCR.

[after]

Bit	Symbol	Function	R/W
2	NONSEC02	Non Secure Attribute bit 02 Target register: HOCOCR, HOCOCR2, FLLCR1, FLLCR2, HOCOUTCR Target factor: HOCO 0: Secure 1: Non Secure	R/W

(Omitted some parts)

NONSEC02 bit (Non Secure Attribute bit 02)
This bit controls the security attribute of HOCOCR, HOCOCR2, FLLCR1, FLLCR2, HOCOUTCR.

- **(RA6T2)** 8.2.1 CGFSAR : Clock Generation Function Security Attribute Register

[before]

Bit	Symbol	Function	R/W
2	NONSEC02	Non Secure Attribute bit 02 Target register: HOCOCR, HOCOUTCR Target factor: HOCO 0: Secure 1: Non Secure	R/W

(Omitted some parts)

NONSEC02 bit (Non Secure Attribute bit 02)
This bit controls the security attribute of HOCOCR, HOCOUTCR.

[after]

Bit	Symbol	Function	R/W
2	NONSEC02	Non Secure Attribute bit 02 Target register: HOCOCR, HOCOCR2, HOCOUTCR Target factor: HOCO 0: Secure 1: Non Secure	R/W

(Omitted some parts)

NONSEC02 bit (Non Secure Attribute bit 02)
This bit controls the security attribute of HOCOCR, HOCOCR2, HOCOUTCR.

3. Modified description HOCOCR register.

- **(RA6M4, RA6M5)** 8.2.12 HOCOCR : High-Speed On-Chip Oscillator Control Register
  (RA6E1, RA4M2, RA4M3, RA4E1) 8.2.11 HOCOCR : High-Speed On-Chip Oscillator Control Register
  (RA6T2) 8.2.10 HOCOCR : High-Speed On-Chip Oscillator Control Register
  (RA6E2, RA4E2) 8.2.9 HOCOCR : High-Speed On-Chip Oscillator Control Register

[before]

Bit	Symbol	Function	R/W
0	HCSTP	HOCO Stop 0: Operate the HOCO clock *2 1: Stop the HOCO clock	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If you are using the HOCO (HCSTP = 0), set the OFS1.HOCOFRQ0[1:0] bit to an optimum value.

[after]

Bit	Symbol	Function	R/W
0	HCSTP	HOCO Stop 0: Operate the HOCO clock *2 *3 1: Stop the HOCO clock	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If you are using the HOCO (HCSTP = 0), set the OFS1.HOCOFRQ0[1:0] bit to an optimum value.

Note 3 The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] even if OFS1.HOCOFRQ0[1:0] is not appropriate value.

- **(RA6M1, RA6M2, RA6T1)** 9.2.10 High-Speed On-Chip Oscillator Control Register (HOCOCR)

[before]

Bit	Symbol	Function	Description	R/W
b0	HCSTP	HOCO Stop	0: Operate the HOCO clock*2 1: Stop the HOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If you use the HOCO (HCSTP = 0), you must set the OFS1.HOCOFRQ0[1:0] bits to an optimum value.

[after]

Bit	Symbol	Function	Description	R/W
b0	HCSTP	HOCO Stop	0: Operate the HOCO clock*2 *3 1: Stop the HOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If you use the HOCO (HCSTP = 0), you must set the OFS1.HOCOFRQ0[1:0] bits to an optimum value.

Note 3 The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] even if OFS1.HOCOFRQ0[1:0] is not appropriate value.

● **(RA6M3)** 9.2.10 High-Speed On-Chip Oscillator Control Register (HOCOCR)

[before]

Bit	Symbol	Function	Description	R/W
b0	HCSTP	HOCO Stop	0: Operate the HOCO clock*2 1: Stop the HOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.
Note 2. If you are using the HOCO (HCSTP = 0), you must set the OFS1.HOCOFRQ0[1:0] bits to an optimum value.

[after]

Bit	Symbol	Function	Description	R/W
b0	HCSTP	HOCO Stop	0: Operate the HOCO clock*2 *3 1: Stop the HOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.
Note 2. If you are using the HOCO (HCSTP = 0), you must set the OFS1.HOCOFRQ0[1:0] bits to an optimum value.
Note 3 The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] even if OFS1.HOCOFRQ0[1:0] is not appropriate value.

● **(RA4M1)** 8.2.9 High-Speed On-Chip Oscillator Control Register (HOCOCR)

[before]

Bit	Symbol	Function	Description	R/W
b0	HCSTP	HOCO Stop	0: Operate the HOCO clock*2 *3 1: Stop the HOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Writing to OPCCR.OPCM[1:0] is prohibited while HOCOCR.HCSTP = 0 and OSCSF.HOCOSF = 0 (HOCO is in stabilization wait counting).
Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.
Note 2. If the operating frequency of HOCO is 48 MHz, VCC must be more than 1.8 V (VCC ≥ 1.8 V) when operating the HOCO.
If the operating frequency of HOCO is 64 MHz, VCC must be more than 2.4 V (VCC ≥ 2.4 V) when operating the HOCO.
Note 3. When using the HOCO (HCSTP = 0), the OFS1.HOCOFRQ1 bit must be set to an optimum value. During low-voltage mode, HOCOCR.HCSTP must always be 0.
Note: Writing HCSTP is prohibited while OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of operating power control mode) or FLSTOP.CFLSTOPF = 1 (during transition of flash).

[after]

Bit	Symbol	Function	Description	R/W
b0	HCSTP	HOCO Stop	0: Operate the HOCO clock*2 *3 *4 1: Stop the HOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Writing to OPCCR.OPCM[1:0] is prohibited while HOCOCR.HCSTP = 0 and OSCSF.HOCOSF = 0 (HOCO is in stabilization wait counting).
Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.
Note 2. If the operating frequency of HOCO is 48 MHz, VCC must be more than 1.8 V (VCC ≥ 1.8 V) when operating the HOCO.
If the operating frequency of HOCO is 64 MHz, VCC must be more than 2.4 V (VCC ≥ 2.4 V) when operating the HOCO.
Note 3. When using the HOCO (HCSTP = 0), the OFS1.HOCOFRQ1 bit must be set to an optimum value. During low-voltage mode, HOCOCR.HCSTP must always be 0.
Note: Writing HCSTP is prohibited while OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of operating power control mode) or FLSTOP.CFLSTOPF = 1 (during transition of flash).
Note 4 The value of OFS1.HOCOFRQ1[2:0] bits is automatically transferred to HOCOCR2.HCFRQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ1[2:0] even if OFS1.HOCOFRQ1[2:0] is not appropriate value.

● **(RA4W1)** 9.2.9 High-Speed On-Chip Oscillator Control Register (HOCOCR)

[before]

Bit	Symbol	Function	Description	R/W
b0	HCSTP	HOCO Stop	0: Operate the HOCO clock*2 *3 1: Stop the HOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Writing to OPCCR.OPCM[1:0] is prohibited while HOCOCR.HCSTP = 0 and OSCSF.HOCOSF = 0 (HOCO is in stabilization wait counting).

Note: Writing HCSTP is prohibited while OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of operating power control mode) or FLSTOP.CFLSTOPF = 1 (during transition of flash).

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If the operating frequency of HOCO is 48 MHz, VCC must be more than 1.8 V (VCC ≥ 1.8 V) when operating the HOCO. If the operating frequency of HOCO is 64 MHz, VCC must be more than 2.4 V (VCC ≥ 2.4 V) when operating the HOCO.

Note 3. When using the HOCO (HCSTP = 0), the OFS1.HOCOFRQ1 bit must be set to an optimum value. During low-voltage mode, HOCOCR.HCSTP bit must always be 0.

[after]

Bit	Symbol	Function	Description	R/W
b0	HCSTP	HOCO Stop	0: Operate the HOCO clock*2 *3 *4 1: Stop the HOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Writing to OPCCR.OPCM[1:0] is prohibited while HOCOCR.HCSTP = 0 and OSCSF.HOCOSF = 0 (HOCO is in stabilization wait counting).

Note: Writing HCSTP is prohibited while OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of operating power control mode) or FLSTOP.CFLSTOPF = 1 (during transition of flash).

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.

Note 2. If the operating frequency of HOCO is 48 MHz, VCC must be more than 1.8 V (VCC ≥ 1.8 V) when operating the HOCO. If the operating frequency of HOCO is 64 MHz, VCC must be more than 2.4 V (VCC ≥ 2.4 V) when operating the HOCO.

Note 3. When using the HOCO (HCSTP = 0), the OFS1.HOCOFRQ1 bit must be set to an optimum value. During low-voltage mode, HOCOCR.HCSTP bit must always be 0.

Note 4 The value of OFS1.HOCOFRQ1[2:0] bits is automatically transferred to HOCOCR2.HCFRQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ1[2:0] even if OFS1.HOCOFRQ1[2:0] is not appropriate value.

4. Modified description FLLCNTL[10:0] bits in FLLCR2.

- **(RA6M4, RA6M5)** 8.2.15 FLLCR2 : FLL Control Register2
  (RA6E1, RA4M2, RA4M3, RA4E1) 8.2.14 FLLCR2 : FLL Control Register2
  (RA6E2, RA4E2) 8.2.12 FLLCR2 : FLL Control Register2

[before]

Bit	Symbol	Function	R/W
10:0	FLLCNTL[10:0]	FLL Multiplication Control When OFS1.HOCOFRQ[1:0] is 00b (16MHz), these bits must be set to 0x1E9. When OFS1.HOCOFRQ[1:0] is 01b (18MHz), these bits must be set to 0x226. When OFS1.HOCOFRQ[1:0] is 10b (20MHz), these bits must be set to 0x263 Other settings are prohibited.	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W

[after]

Bit	Symbol	Function	R/W
10:0	FLLCNTL[10:0]	FLL Multiplication Control When OFS1.HOCOFRQ0[1:0] is 00b (16MHz), these bits must be set to 0x1E9. When OFS1.HOCOFRQ0[1:0] is 01b (18MHz), these bits must be set to 0x226. When OFS1.HOCOFRQ0[1:0] is 10b (20MHz), these bits must be set to 0x263 Other settings are prohibited.	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W

Note 1 The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0].

- **(RA6M1, RA6M2, RA6M3)** 9.2.14 FLL Control Register 2 (FLLCR2)
  (RA6T1) 8.2.12 FLL Control Register 2 (FLLCR2)

[before]

Bit	Symbol	Bit name	Description	R/W
bit10 to bit00	FLLCNTL[10:0]	FLL Multiplication Control	• When OFS1.HOCOFRQ0[1:0] is 00b (16 MHz), these bits must be set to 1E9h • When OFS1.HOCOFRQ0[1:0] is 01b (18 MHz), these bits must be set to 226h • When OFS1.HOCOFRQ0[1:0] is 10b (20 MHz), these bits must be set to 263h. Other settings are prohibited.	R/W
bit15: to bit11	—	.	These bits are read as 0. The write value should be 0.	R/W

[after]

Bit	Symbol	Bit name	Description	R/W
bit10 to bit00	FLLCNTL[10:0]	FLL Multiplication Control	• When OFS1.HOCOFRQ0[1:0] is 00b (16 MHz), these bits must be set to 1E9h • When OFS1.HOCOFRQ0[1:0] is 01b (18 MHz), these bits must be set to 226h • When OFS1.HOCOFRQ0[1:0] is 10b (20 MHz), these bits must be set to 263h. Other settings are prohibited.	R/W
bit15: to bit11	—	.	These bits are read as 0. The write value should be 0.	R/W

Note 1 The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0].

5. Modified description of System Clock (ICLK) section in Clock Generation Circuit chapter.

- **(RA6M4, RA6M5, RA6E2, RA4M3, RA4E2)** 8.7.1 System Clock (ICLK)

[before]
The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, the PLLMUL[5:0] bits and PLIDIV[1:0] bits in PLLCCR, and the HOCOFRQ0[1:0] bits in OFS1.

[after]
The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, the PLLMUL[5:0] bits and PLIDIV[1:0] bits in PLLCCR, and the HOCOFRQ0[1:0] bits in OFS1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6E1, RA4M2, RA4E1)** 8.7.1 System Clock (ICLK)
  (RA6T2) 8.6.1 System Clock (ICLK)

[before]
The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, the PLLMUL[5:0], and PLIDIV[1:0] bits in PLLCCR, and the HOCOFRQ0[1:0] bits in OFS1.

[after]
The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, the PLLMUL[5:0], and PLIDIV[1:0] bits in PLLCCR, and the HOCOFRQ0[1:0] bits in OFS1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6M1, RA6T1)** 9.7.1 System Clock (ICLK)

[before]
The ICLK frequency is specified in the following bits:
- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]
The ICLK frequency is specified in the following bits:
- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6M2, RA6M3)** 9.7.1 System Clock (ICLK)

[before]
Specify the frequency in the following bits:
- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]
Specify the frequency in the following bits:
- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

● **(RA4M1)** 8.7.1 System Clock (ICLK)

[before]

The ICLK frequency is specified in the following bits:

- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2
- HOCOFRQ1[2:0] bits in OFS1.

[after]

The ICLK frequency is specified in the following bits:

- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2
- HOCOFRQ1[2:0] bits in OFS1.

The value of OFS1.HOCOFRQ1[2:0] bits is automatically transferred to HOCOCR2.HCFRQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ1[2:0] bits.

● **(RA4W1)** 9.8.1 System Clock (ICLK)

[before]

The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, the PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2, and the HOCOFRQ1[2:0] bits in OFS1.

[after]

The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, the PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2, and the HOCOFRQ1[2:0] bits in OFS1.

The value of OFS1.HOCOFRQ1[2:0] bits is automatically transferred to HOCOCR2.HCFRQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ1[2:0] bits.

6. Modified description of Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD) in Clock Generation Circuit chapter.

- **(RA6M4, RA6E1, RA6E2, RA4M3, RA4E1, RA4E2)** 8.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)
  (RA6T2) 8.6.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

[before]

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0] and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0] and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1. *1

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6M5)** 8.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

[before]

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0] and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] bits and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0] and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] bits and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1. *1

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA4M2)** 8.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

[before]

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0], PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0], PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1. *1

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

● **(RA6M1, RA6T1)** 9.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

[before]

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1. *1

  Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

● **(RA6M2, RA6M3)** 9.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

[before]

Specify the frequency in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

Specify the frequency in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1. *1

  Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

● **(RA4M1)** 8.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)
(RA4W1) 9.8.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

[before]

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2
- HOCOFRQ1[2:0] bits in OFS1.

[after]

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2
- HOCOFRQ1[2:0] bits in OFS1. *1

  Note 1. The value of OFS1.HOCOFRQ1[2:0] bits is automatically transferred to HOCOCR2.HCFRQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ1[2:0] bits.

7. Modified description of FlashIF Clock (FCLK) section in Clock Generation Circuit chapter.

- **(RA6M4, RA6E1, RA6E2, RA4M2, RA4M3, RA4E1, RA4E2)** 8.7.3 FlashIF Clock (FCLK)
  (RA6T2) 8.6.3 FlashIF Clock (FCLK)

[before]

The FCLK frequency is specified in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

The FCLK frequency is specified in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1. *1

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6M5)** 8.7.3 FlashIF Clock (FCLK)

[before]

The FCLK frequency is specified in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] bits and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

The FCLK frequency is specified in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] bits and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1. *1

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6M1, RA6T1)** 9.7.3 Flash Interface Clock (FCLK)

[before]

The FCLK frequency is specified in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

The FCLK frequency is specified in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1. *1

Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6M2, RA6M3)** 9.7.3 Flash Interface Clock (FCLK)

[before]

Specify the frequency in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

Specify the frequency in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1. *1

  Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA4M1)** 8.7.3 Flash Interface Clock (FCLK)
  (RA4W1) 9.8.3 Flash Interface Clock (FCLK)

[before]

The FCLK frequency is specified in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2
- HOCOFRQ1[2:0] bits in OFS1.

[after]

The FCLK frequency is specified in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2
- HOCOFRQ1[2:0] bits in OFS1. *1

  Note 1. The value of OFS1.HOCOFRQ1[2:0] bits is automatically transferred to HOCOCR2.HCFRQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ1[2:0] bits.

8. Modified description of External Bus Clock (BCLK) section in Clock Generation Circuit chapter.

- **(RA6M4)** 8.7.4 External Bus Clock (BCLK)

[before]

Specify the frequency in the following bits:

- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

Specify the frequency in the following bits:

- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1. *1

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6M5)** 8.7.4 External Bus Clock (BCLK)

[before]

Specify the frequency in the following bits:

- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] bits and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

Specify the frequency in the following bits:

- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] bits and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1. *1

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6M1)** 9.7.4 External Bus Clock (BCLK)

[before]

The BCLK frequency is specified in the following bits:

- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

The BCLK frequency is specified in the following bits:

- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1. *1

Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6M2, RA6M3)** 9.7.4 External Bus Clock (BCLK)

[before]

Specify the frequency in the following bits:

- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

Specify the frequency in the following bits:

- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1. *1

Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

9. Modified description of External Pin Output Clock (CLKOUT) section in Clock Generation Circuit chapter.

- **(RA6M4, RA6T2)** 8.7.13 External Pin Output Clock (CLKOUT)
  (RA6M5) 8.7.17 External Pin Output Clock (CLKOUT)
  (RA6E2, RA4E2) 8.7.12 External Pin Output Clock (CLKOUT)
  (RA4M3) 8.7.11 External Pin Output Clock (CLKOUT)

[before]

The CLKOUT clock frequency is specified in the following bits:

- CKODIV[2:0] bits or CKOSEL[2:0] bits in CKOCR
- HOCOFRQ0[1:0] bits in OFS1

[after]

The CLKOUT clock frequency is specified in the following bits:

- CKODIV[2:0] bits or CKOSEL[2:0] bits in CKOCR
- HOCOFRQ0[1:0] bits in OFS1 *1

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6E1, RA4M2, RA4E1)** 8.7.11 External Pin Output Clock (CLKOUT)

[before]

The CLKOUT clock frequency is specified in the following bits:

- CKODIV[2:0] or CKOSEL[2:0] in CKOCR
- HOCOFRQ0[1:0] bits in OFS1

[after]

The CLKOUT clock frequency is specified in the following bits:

- CKODIV[2:0] or CKOSEL[2:0] in CKOCR
- HOCOFRQ0[1:0] bits in OFS1 *1

Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6M1, RA6T1)** 9.7.12 Clock/Buzzer Output Clock (CLKOUT)

[before]

The CLKOUT frequency is specified in the following bits:

- CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

The CLKOUT frequency is specified in the following bits:

- CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR
- HOCOFRQ0[1:0] bits in OFS1. *1

Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA6M2)** 9.7.13 Clock/Buzzer Output Clock (CLKOUT)
  (RA6M3) 9.7.14 Clock/Buzzer Output Clock (CLKOUT)

[before]

Specify the frequency in the following bits:

- CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR
- HOCOFRQ0[1:0] bits in OFS1.

[after]

Specify the frequency in the following bits:

- CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR
- HOCOFRQ0[1:0] bits in OFS1. *1

Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits.

- **(RA4M1)** 8.7.12 Clock/Buzzer Output Clock (CLKOUT)
  (RA4W1) 9.8.12 Clock/Buzzer Output Clock (CLKOUT)

[before]

The CLKOUT clock frequency is specified in the following bits:

- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2
- HOCOFRQ1[2:0] bits in OFS1.

[after]

The CLKOUT clock frequency is specified in the following bits:

- PLLMUL[4:0] and PLODIV[1:0] bits in PLLCCR2
- HOCOFRQ1[2:0] bits in OFS1. *1

Note 1. The value of OFS1.HOCOFRQ1[2:0] bits is automatically transferred to HOCOCR2.HCFRQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ1[2:0] bits.

10. Modified description HOCOEN bit in Option Function Select Register 1.

- **(RA6M4, RA6M5)** 6.2.4 OFS1, OFS1_SEC, OFS1_SEL : Option Function Select Register 1
  (RA4M3) 6.2.3 OFS1, OFS1_SEC, OFS1_SEL : Option Function Select Register 1

[before]
HOCOEN bit (HOCO Oscillation Enable)
The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the HOCO Frequency Setting 0 bits (OFS1.HOCOFRQ0[1:0]) to an optimum value.

[after]
HOCOEN bit (HOCO Oscillation Enable)
The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the HOCO Frequency Setting 0 bits (OFS1.HOCOFRQ0[1:0] [*1]) to an optimum value.
Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits when OFS1.HOCOEN=1.

- **(RA6E1, RA6E2, RA4E2)** 6.2.4 OFS1, OFS1_SEC, OFS1_SEL : Option Function Select Register 1
  (RA6T2, RA4M2, RA4E1) 6.2.3 OFS1, OFS1_SEC, OFS1_SEL : Option Function Select Register 1

[before]
HOCOEN bit (HOCO Oscillation Enable)
The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFRQ0 bit to an optimum value.

[after]
HOCOEN bit (HOCO Oscillation Enable)
The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFRQ0 bit [*1] to an optimum value.
Note 1. OFS1 is for non-secure developers and OFS1_SEC is for secure developers. The applied setting value is determined by OFS1_SEL. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits when OFS1.HOCOEN=1.

● **(RA6M1, RA6M2, RA6T1)** 7.2.2 Option Function Select Register 1 (OFS1)

[before]

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFRQ0[1:0] bits to an optimum value.

[after]

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFRQ0[1:0] bits *1 to an optimum value.

Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits when OFS1.HOCOEN=1.

● **(RA6M3)** 7.2.2 Option Function Select Register 1 (OFS1)

[before]

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enable or disable after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the clock source select bits (SCKSCR.CKSEL[2:0]). If you use the HOCO clock, you must set the OFS1.HOCOFRQ0[1:0] bits to an optimum value.

[after]

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enable or disable after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the clock source select bits (SCKSCR.CKSEL[2:0]). If you use the HOCO clock, you must set the OFS1.HOCOFRQ0[1:0] bits *1 to an optimum value.

Note 1. The value of OFS1.HOCOFRQ0[1:0] bits is automatically transferred to HOCOCR2.HCFRQ0[1:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ0[1:0] bits when OFS1.HOCOEN=1.

● **(RA4M1)** 6.2.2 Option Function Select Register 1 (OFS1)

[before]

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is switched to HOCO only by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, set the OFS1.HOCOFRQ1 bit to an optimum value.

[after]

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is switched to HOCO only by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, set the OFS1.HOCOFRQ1 bit *1 to an optimum value.

Note 1. The value of OFS1.HOCOFRQ1[2:0] bits is automatically transferred to HOCOCR2.HCFRQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ1[2:0] bits when OFS1.HOCOEN=1.

● **(RA4W1)** 7.2.2 Option Function Select Register 1 (OFS1)

[before]

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFRQ1 bit to an optimum value.

[after]

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFRQ1 bit *1 to an optimum value.

Note 1. The value of OFS1.HOCOFRQ1[2:0] bits is automatically transferred to HOCOCR2.HCFRQ1[2:0] bits after reset, therefore HOCO frequency can also be specified by HOCOCR2.HCFRQ1[2:0] bits when OFS1.HOCOEN=1.

11. Added HOCOCR2 to register protected by PCR0 bit in PRCR.

● **(RA6M4,RA6E1)** Table 12.1 Association between the bits in the PRCR register and registers to be protected

[before]

PRCR bit	Register to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, MOCOCR, FLLCR1, FLLCR2, CKOCR, TRCKCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, EBCKOCR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, OCTACKDIVCR, USBCKCR, OCTACKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR

[after]

PRCR bit	Register to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, HOCOCR2, MOCOCR, FLLCR1, FLLCR2, CKOCR, TRCKCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, EBCKOCR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, OCTACKDIVCR, USBCKCR, OCTACKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR

● **(RA6M5)** Table 12.1 Association between the bits in the PRCR register and registers to be protected

[before]

PRCR bit	Register to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, MOCOCR, FLLCR1, FLLCR2, CKOCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, EBCKOCR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, OCTACKDIVCR, CANFDCKDIVCR, USB60CKDIVCR, CECCKDIVCR, USBCKCR, OCTACKCR, CANFDCKCR, USB60CKCR, CECCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR

[after]

PRCR bit	Register to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, HOCOCR2, MOCOCR, FLLCR1, FLLCR2, CKOCR, TRCKCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, EBCKOCR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, OCTACKDIVCR, CANFDCKDIVCR, USB60CKDIVCR, CECCKDIVCR, USBCKCR, OCTACKCR, CANFDCKCR, USB60CKCR, CECCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR

● **(RA6E2, RA4E2)** Table 11.1 Association between the bits in the PRCR register and registers to be protected

[before]

PRCR bit	Register to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, MOCOCR, FLLCR1, FLLCR2, CKOCR, OSTDCR, OSTDSR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, I3CCKDIVCR, CANFDCKDIVCR, CECCKDIVCR, USBCKCR, I3CCKCR, CANFDCKCR, CECCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR

[after]

PRCR bit	Register to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, HOCOCR2, MOCOCR, FLLCR1, FLLCR2, CKOCR, OSTDCR, OSTDSR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, I3CCKDIVCR, CANFDCKDIVCR, CECCKDIVCR, USBCKCR, I3CCKCR, CANFDCKCR, CECCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR

● **(RA4M2, RA4M3, RA4E1)** Table 12.1 Association between the bits in the PRCR register and registers to be protected

[before]

PRCR bit	Register to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, MOCOCR, FLLCR1, FLLCR2, CKOCR, TRCKCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, USBCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR

[after]

PRCR bit	Register to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, HOCOCR2, MOCOCR, FLLCR1, FLLCR2, CKOCR, TRCKCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, USBCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR

● **(RA6T2)** Table 11.1 Association between the bits in the PRCR register and registers to be protected

[before]

PRCR bit	Register to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, MOCOUTCR, HOCOUTCR, SCISPICKDIVCR, CANFDCKDIVCR, GPTCKDIVCR, IICCKDIVCR, SCISPICKCR, CANFDCKCR, GPTCKCR, IICCKCR, MOSCWTCR, MOMCR, LOCOCR, LOCOUTCR

[after]

PRCR bit	Register to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, HOCOCR2, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, MOCOUTCR, HOCOUTCR, SCISPICKDIVCR, CANFDCKDIVCR, GPTCKDIVCR, IICCKDIVCR, SCISPICKCR, CANFDCKCR, GPTCKCR, IICCKCR, MOSCWTCR, MOMCR, LOCOCR, LOCOUTCR

● **(RA6M1)** Table 13.1 Association between PRCR bits and registers to be protected

[before]

PRCR bit	Registers to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKDIVCR2, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, EBCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, FLLCR1, FLLCR2

[after]

PRCR bit	Registers to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKDIVCR2, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, HOCOCR2, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, EBCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, FLLCR1, FLLCR2

● **(RA6M2)** Table 14.1 Association between PRCR bits and registers to be protected
(RA6M3) Table 13.1 Association between PRCR bits and registers to be protected

[before]

PRCR bit	Registers to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKDIVCR2, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, EBCKOCR, SDCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, FLLCR1, FLLCR2

[after]

PRCR bit	Registers to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKDIVCR2, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, HOCOCR2, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, EBCKOCR, SDCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, FLLCR1, FLLCR2

● **(RA6T1)** Table 12.1 Association between PRCR bits and registers to be protected

[before]

PRCR bit	Registers to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, FLLCR1, FLLCR2.

[after]

PRCR bit	Registers to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, HOCOCR2, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, FLLCR1, FLLCR2.

● **(RA4M1)** Table 12.1 Association between PRCR bits and registers to be protected

[before]

PRCR bit	Registers to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCR, PLLCCR2, MEMWAIT, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, SLCDSCKCR, EBCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, USBCKCR

[after]

PRCR bit	Registers to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCR, PLLCCR2, MEMWAIT, MOSCCR, HOCOCR, HOCOCR2, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, SLCDSCKCR, EBCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, USBCKCR

● (RA4W1) Table 13.1 Association between PRCR bits and registers to be protected

[before]

PRCR bit	Registers to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCR, PLLCCR2, BCKCR, MEMWAIT, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, SLCDSCKCR, EBCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, USBCKCR

[after]

PRCR bit	Registers to be protected
PRC0	● Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCR, PLLCCR2, BCKCR, MEMWAIT, MOSCCR, HOCOCR, HOCOCR2, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, SLCDSCKCR, EBCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, USBCKCR

Reference Document Table

Product	Document name
RA6M4 Group	Renesas RA6M4 Group User's Manual: Hardware Rev.1.20
RA6M5 Group	Renesas RA6M5 Group User's Manual: Hardware Rev.1.20
RA6E1 Group	Renesas RA6E1 Group User's Manual: Hardware Rev.1.10
RA6E2 Group	Renesas RA6E2 Group User's Manual: Hardware Rev.1.10
RA6T2 Group	Renesas RA6T2 Group User's Manual: Hardware Rev.1.30
RA4M2 Group	Renesas RA4M2 Group User's Manual: Hardware Rev.1.20
RA4M3 Group	Renesas RA4M3 Group User's Manual: Hardware Rev.1.30
RA4E1 Group	Renesas RA4E1 Group User's Manual: Hardware Rev.1.10
RA4E2 Group	Renesas RA4E2 Group User's Manual: Hardware Rev.1.10
RA6M1 Group	Renesas RA6M1 Group User's Manual: Hardware Rev.1.20
RA6M2 Group	Renesas RA6M2 Group User's Manual: Hardware Rev.1.20
RA6M3 Group	Renesas RA6M3 Group User's Manual: Hardware Rev.1.20
RA6T1 Group	Renesas RA6T1 Group User's Manual: Hardware Rev.1.20
RA4M1 Group	Renesas RA4M1 Group User's Manual: Hardware Rev.1.00
RA4W1 Group	Renesas RA4W1 Group User's Manual: Hardware Rev.1.00