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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A862A/E	Rev.	1.00
Title	The addition to the description of assertion/negation expanded cycle in MPX-I/O of the Bus State Controller (BSC)		Information Category	Technical Notification		
Applicable Product	SH7084 Group SH7085 Group SH7086 Group	Lot No. ALL	Reference Document	SH7080 Group User's Manual: Hardware Rev.5.00(R01UH0198EJ0500)		

We would like to inform you of addition to the description of assertion/negation expanded cycle in MPX-I/O of the Bus State Controller (BSC) in the applicable products.

1. Update of the register description

9.4.3 CSn Space Wait Control Register (CSnWCR) (n = 0 to 8)

(2) MPX-I/O

- CS5WCR

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
12, 11	SW[1:0]	00	R/W	Number of Delay Cycles from Address and $\overline{\text{CSn}}$ Assertion to $\overline{\text{RD}}$ and $\overline{\text{WRxx}}$ Assertion Specify the number of delay cycles from address and $\overline{\text{CSn}}$ assertion to $\overline{\text{RD}}$ and $\overline{\text{WRxx}}$ assertion. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles
1, 0	HW[1:0]	00	R/W	Delay Cycles from $\overline{\text{RD}}$ and $\overline{\text{WRxx}}$ Negation to Address and $\overline{\text{CSn}}$ Negation Specify the number of delay cycles from $\overline{\text{RD}}$ and $\overline{\text{WRxx}}$ negation to address and $\overline{\text{CSn}}$ negation. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles

[After change]

Bit	Bit Name	Initial Value	R/W	Description
12, 11	SW[1:0]	00	R/W	Number of Delay Cycles from the End of the Address Cycles(Ta3) to $\overline{RD}$ and $\overline{WRxx}$ Assertion Specify the number of delay cycles from the end of the address cycles(Ta3) to $\overline{RD}$ and $\overline{WRxx}$ assertion. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles
1, 0	HW[1:0]	00	R/W	Delay Cycles from $\overline{RD}$ and $\overline{WRxx}$ Negation to $\overline{CSn}$ Negation Specify the number of delay cycles from $\overline{RD}$ and $\overline{WRxx}$ negation to $\overline{CSn}$ negation. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles

2. Addition to the description of operation

9.5.5 MPX-I/O Interface

[Before change]

The data cycle is the same as that in a normal space access.

Timing charts are shown in figures 9.11 to 9.13.

[After change]

The data cycle is the same as that in a normal space access.

The delay cycle of SW[1:0] is inserted between Ta3 and T1 cycle.

The delay cycle of HW[1:0] is added after T2 cycle.

Timing charts are shown in figures 9.11 to 9.13.

[Addition]

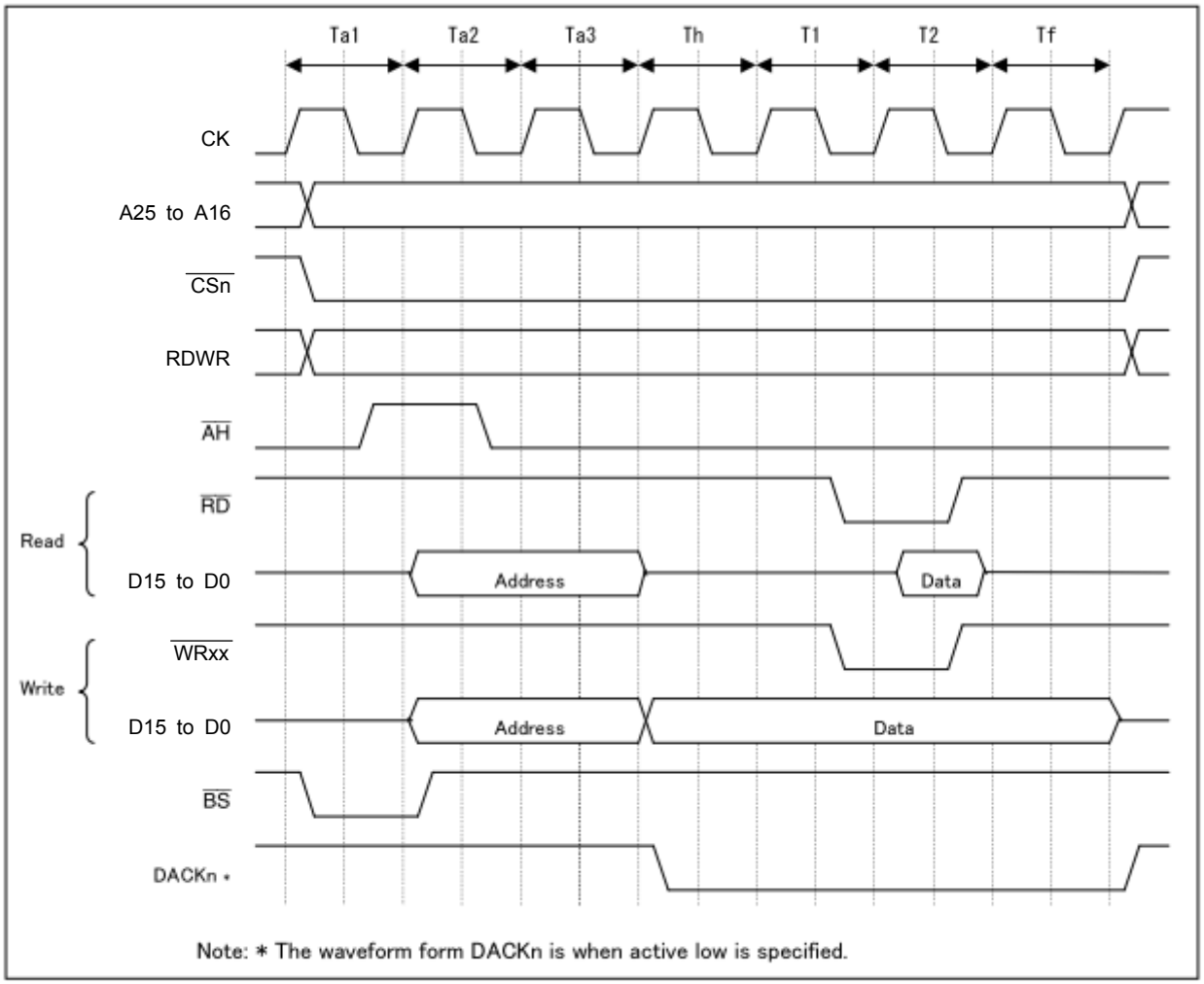

Figure 9.11 (2) Access Timing for MPX Space
(Address Cycle No WAIT, Assert Period Expansion 1.5, Data Cycle No Wait, Negation Period Expansion 1.5)