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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A861A/E	Rev.	1.00
Title	The addition to the description of assertion/negation expanded cycle in MPX-I/O of the Bus State Controller (BSC)		Information Category	Technical Notification		
Applicable Product	See below	Lot No. ALL	Reference Document	See below		

We would like to inform you of addition to the description of assertion/negation expanded cycle in MPX-I/O of the Bus State Controller (BSC) in the applicable products.

The following # denotes section number and $$/mm denotes figure number. The following table shows correspondence of each product.

Group	Section number (#)	Figure number ($$)	Figure number (mm)
SH7206	8	Figures 8.12 to 8.14	8.12
SH7203	9	Figures 9.11 to 9.13	9.11
SH7263	9	Figures 9.11 to 9.13	9.11
SH7262, SH7264	9	Figures 9.11 to 9.13	9.11
SH7211	8	Figures 8.10 to 8.12	8.10
SH7214, SH7216	9	Figures 9.11 to 9.13	9.11
SH7231	10	Figures 10.11 to 10.13	10.11
SH7239, SH7237	9	Figures 9.10 to 9.12	9.10
SH7285, SH7286, SH7243	9	Figures 9.11 to 9.13	9.11

1. Update of the register description

#.4.3 CSn Space Wait Control Register (CSnWCR)

(1) Normal Space, SRAM with Byte Selection, MPX-I/O

- CS5WCR

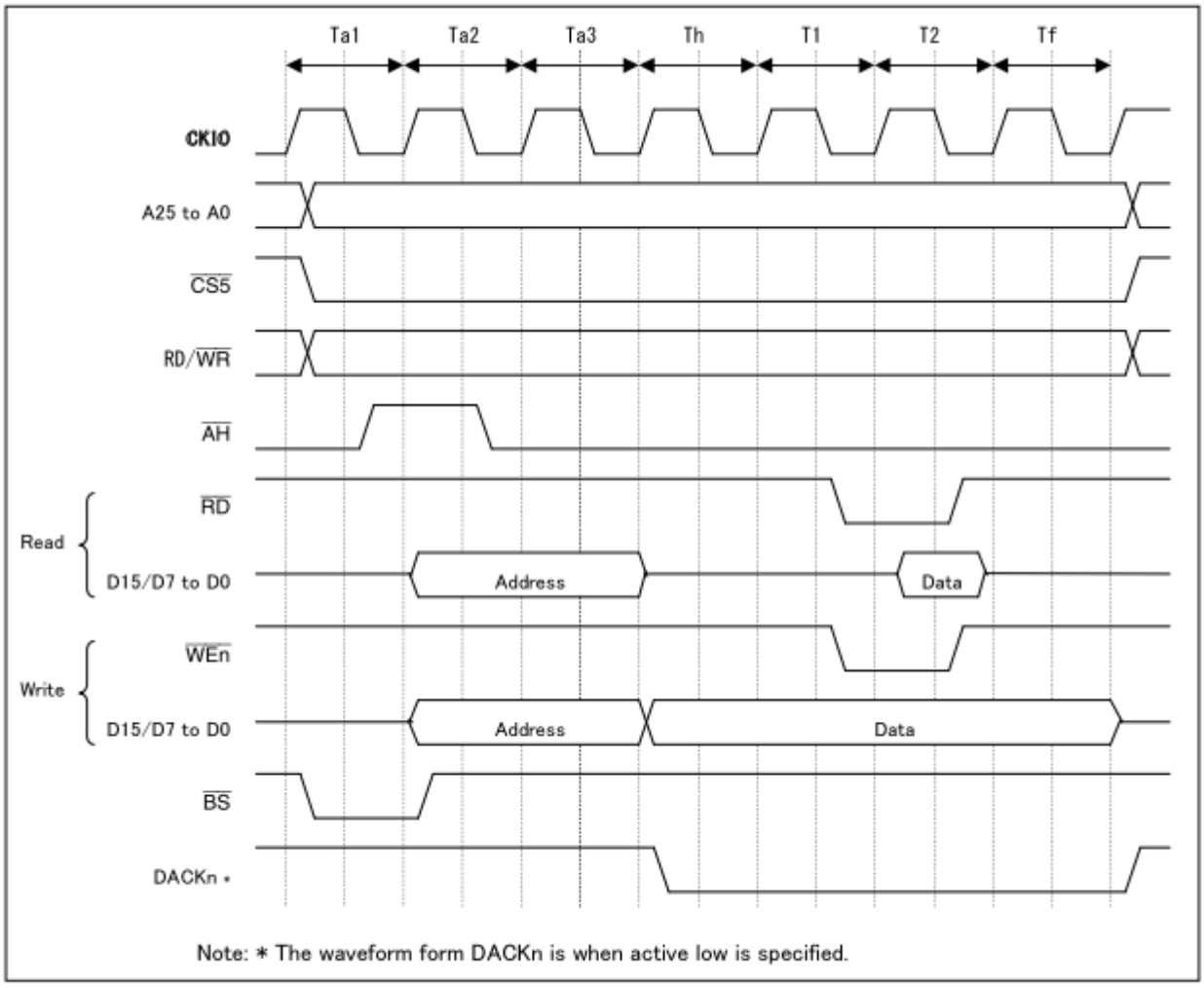
Bit	Bit Name	Initial Value	R/W	Description
12, 11	SW[1:0]	00	R/W	Number of Delay Cycles from Address, $\overline{CS5}$ Assertion to $\overline{RD}$, $\overline{WE}$ Assertion Specify the number of delay cycles from address and $\overline{CS5}$ assertion to $\overline{RD}$ and $\overline{WEn}$ assertion when area 5 is specified as the normal space, SRAM with byte selection. Specify the number of delay cycles from the end of the address cycles(Ta3) to $\overline{RD}$ and $\overline{WEn}$ assertion when area 5 is specified as MPX-I/O. 00: 0.5 cycles 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles
1, 0	HW[1:0]	00	R/W	Delay Cycles from RD, $\overline{WEn}$ Negation to Address, $\overline{CS5}$ Negation Specify the number of delay cycles from $\overline{RD}$ and $\overline{WEn}$ negation to address and $\overline{CS5}$ negation when area 5 is specified as the normal space, SRAM with byte selection. Specify the number of delay cycles from $\overline{RD}$ and $\overline{WEn}$ negation to $\overline{CS5}$ negation when area 5 is specified as MPX-I/O. 00: 0.5 cycles 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles

2. Addition to the description of operation

#.5.5 MPX-I/O Interface

The data cycle is the same as that in a normal space access.
The delay cycle of SW[1:0] is inserted between Ta3 and T1 cycle.
The delay cycle of HW[1:0] is added after T2 cycle.
Timing charts are shown $$.

[Addition]



mm (2) Access Timing for MPX Space
(Address Cycle No WAIT, Assert Period Expansion 1.5, Data Cycle No Wait, Negation Period Expansion 1.5)

Applicable Products and Reference Documents

Group	Reference Document Title	Rev.	Document No.
SH7206	SH7206 Group User's Manual: Hardware	Rev.4.00	R01UH0283EJ0400
SH7203	SH7203 Group Hardware Manual	Rev.3.00	REJ09B0313-0300
SH7263	SH7263 Group Hardware Manual	Rev.3.00	REJ09B0290-0300
SH7262, SH7264	SH7262 Group, SH7264 Group User's Manual: Hardware	Rev.3.00	R01UH0134EJ030
SH7211	SH7211 Group Hardware Manual	Rev.3.00	REJ09B0344-0300
SH7214, SH7216	SH7214 Group, SH7216 Group User's Manual: Hardware	Rev.3.00	R01UH0230EJ0300
SH7231	SH7231 Group User's Manual: Hardware	Rev.2.00	R01UH0073EJ0200
SH7239, SH7237	SH7239 Group, SH7237 Group User's Manual: Hardware	Rev.1.00	R01UH0086EJ0100
SH7285, SH7286, SH7243	SH7280 Group, SH7243 Group User's Manual: Hardware	Rev.3.00	R01UH0229EJ0300