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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A894A/E	Rev.	1.00
Title	Addition of the description about the minimum number of idle cycles on the internal bus of the bus state controller (BSC)		Information Category	Technical Notification		
Applicable Product	• SH7214 Group, SH7216 Group • SH7239 Group, SH7237 Group	Lot No. All lots	Reference Document	• SH7214 Group, SH7216 Group User's Manual: Hardware Rev.4.00 (R01UH0230EJ0400) • SH7239 Group, SH7237 Group User's Manual: Hardware Rev.2.00 (R01UH0086EJ0200)		

We would like to inform you of the correction of errors in the above listed user's manuals. Please refer to the following for details.

In the following, $$/## indicates the table number and items 1. to 2. indicate the corresponding section numbers for the correction. The table below lists the corresponding section, table, and figure numbers for respective products.

Group	Section Number	1. Table Number ($$)	2. Table Number (##)
SH7214, SH7216	9	Table 9.22	Table 9.23
SH7239, SH7237	9	Table 9.8	Table 9.9

1. Minimum Number of Idle Cycles on Internal Bus (CPU Operation)

9.5.10 Wait between Access Cycles

[Before correction]

Table 9.$$ Minimum Number of Idle Cycles on Internal Bus (CPU Operation)

	Clock Ratio (Iϕ:Bϕ)			
CPU Operation	8:1	4:1	2:1	1:1
Write → write	0	0	0	0
Write → read	0	0	0	0
Read → write	1	1	2	3
Read → read	0	0	0	0

Conditions

- The bits for setting the idle cycles between access cycles in CS1BCR and CS2BCR are all set to 0
- In CS1WCR and CS2WCR the WM bit is set to 1 (external $\overline{\text{WAIT}}$ pin disabled) and the HW[1:0] bits are set to 00 ($\overline{\text{CS}}$ negation is not extended)
- For both the CS1 and CS2 spaces, normal SRAM devices are connected, the bit width is 32 bits, and access size is also 32 bits.

[After correction]

Table 9.$$ Minimum Number of Idle Cycles on Internal Bus (CPU Operation)

	Clock Ratio (Iϕ:Bϕ)			
CPU Operation	8:1	4:1	2:1	1:1
Write → write	0	0	0	0
Write → read	0	0	0	0
Read → write	1 or 0*	1 or 0*	2 or 0*	3 or 0*
Read → read	0	0	0	0

Operating conditions:

1. The bits for setting the idle cycles between access cycles in CS1BCR and CS2BCR are all set to 0.
2. In CS1WCR and CS2WCR, the WM bit is set to 1 (external WAIT pin disabled), the SW[1:0] bits are set to 00 (CS assertion is not extended), and the HW[1:0] bits are set to 00 (CS negation is not extended).
3. For both the CS1 and CS2 spaces, SRAM devices are connected, the bit width is 16 bits.
4. The unit of access by the CPU data transfer instructions is 16 bits (MOV.W).

Note: 1. This is the case where fetching of an instruction from the external bus (through the F bus) is followed by a data transfer instruction writing to the external bus (through the M bus).

2. Minimum Number of Idle Cycles on Internal Bus (DMAC Operation)

[Before correction]

Table 9.$$ Minimum Number of Idle Cycles on Internal Bus (DMAC Operation)

DMAC Operation	Transfer Mode					
	Dual Address				Single Address*2	
Activation source	Auto request	Peripheral module request	External request (level)	External request (edge)	External request (level)	External request (edge)
Write → write	1	1	3	3	6	1
Write → read	0	0	2 or 0*1	1 or 0*1	0	0
Read → write	0	0	0	0	0	0
Read → read	2	2	5	4	5	2

Operating conditions

1. The write → write cycle means transfer from an on-chip memory to an external memory. The read → read cycle means transfer from an external memory to an on-chip memory. The write → read cycle and read → write cycle mean transfer between external memories. Each of the operations is performed in burst mode.
2. The external data bus width is 16 bits and the DMA transfer size is 16 bits.
3. Ick : Bck = 1 : 1/4

Notes: 1. For the write → read cycles in transfer with an external request (level), 0 means different channels are activated successively and 2 means the same channel is activated successively.
For the write → read cycles in transfer with an external request (edge), 0 means different channels are activated successively and 1 means the same channel is activated successively.
2. The write → read and read → write columns in single address transfer indicate the case when different channels are activated successively. The "write" means transfer from a device with DACK to external memory and the "read" means transfer from external memory to a device with DACK.

[After correction]

Table 9.$$ Minimum Number of Idle Cycles on Internal Bus (DMAC Operation)

DMAC Operation	Transfer Mode				
	Dual Address				
	Auto-request	Peripheral Module	External request (level,AM=0)	External request (level,AM=1)	External request (edge)
Write → write*3	2	2	4*1 or 2*2	9*1*4 or 2*2	4*1 or 2*2
Write → read*3	0	0	2*1 or 0*2	6*1*4 or 0*2	1*1 or 0*2
Read → write	0	0	0	0	0
Read → read	2	2	5*1 or 2*2	4*1 or 2*2	4*1 or 2*2

DMAC Operation	Transfer Mode	
	Single Address	
	External request (level)	External request (edge)
Write → write*3	7*1*4 or 0*2	2*1 or 0*2
Write → read*3	0*2	0*2
Read → write	0*2	0*2
Read → read	5*1 or 0*2	2*1 or 0*2

Operating conditions:

1. The bits for setting the idle cycles between access cycles in CS1BCR and CS2BCR are all set to 0.
2. In CS1WCR and CS2WCR, the WM bit is set to 1 (external $\overline{\text{WAIT}}$ pin disabled), the SW[1:0] bits are set to 00 ($\overline{\text{CS}}$ assertion is not extended), and the HW[1:0] bits are set to 00 ($\overline{\text{CS}}$ negation is not extended).
3. For both the CS1 and CS2 spaces, SRAM devices are connected, the bit width is 16 bits.
4. The DMA transfer size is 16 bits. The operating mode of the DMAC is burst mode.
5. Numbers of cycles given for write → write sequences in dual address transfer are for data transfer between the on-chip memory and external memory, those given for read → read sequences are for data transfer between external memory and the on-chip memory, and those given for write → read and read → write sequences are for data transfer between locations in external memory.
6. In single address transfer, “write” means transfer from a device that has DACK to external memory and “read” means transfer from external memory to a device that has DACK.

Notes: *1. The minimum number of idle cycles in continuous DMA transfer on the same channel.

*2. The minimum number of idle cycles in continuous DMA transfer between different channels.

*3. When $\overline{\text{CS}}$ assertion extension (Th), access wait cycles (Tw), and $\overline{\text{CS}}$ negation extension (Tf) have been inserted for the previous access, the minimum numbers of idle cycles are reduced from the values in the table by Th+Tw+Tf due to the effect of the write buffer.

*4. The effect of the write buffer does not reduce the minimum number of idle cycles.