To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

Classification of Production	MPU&MCU		No	TN-SH7-487A/E	Rev	1.0
THEME	Addition of connectable SDRAM with SH7615.	Classification of Information	1. Spec change (2.) Supplement of Documents 3. Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	HD6417615ARF HD6417615ARFV	Lot No. —	Reference Documents	SH7615 Hardware Manual ADE-602-198 Rev.1.0	term of validity Permanent	

We report newly that 128-Mbit and 256-Mbit Synchronous DRAM are connectable with SH7615.
For the setting method, please refer to the following [After] table of MCR in BSC.
This addition is public presentation of the specification about the portion which was not exhibited before, and the product itself is not changed.
For the applied lot, please refer to the Product Lot Code in the following [Mass production schedule].

[Before]

Section 7 Bus State Controller(BSC)

7.2.7 Individual Memory Control Resister(MCR)

● For synchronous DRAM interface

Bit7:AMX2	Bit5:AMX1	Bit4:AMX0	Description
0	0	0	16-Mbit DRAM(1M X 16bits), 64-Mbit DRAM(2M X 32bits) *2
		1	16-Mbit DRAM(2M X 8bits) *1
	1	0	16-Mbit DRAM(4M X 4bits) *1
		1	4-Mbit DRAM(256k X 16bits)
1	0	0	64-Mbit DRAM(4M X 16bits)
		1	64-Mbit DRAM(8M X 8bits) *1
	1	0	Reserved (do not set)
		1	2-Mbit DRAM(128k X 16bits)

Notes: 1. Reserved. Do not set when SZ bit in MCR is 0 (16-bit bus width).
2. See sction 7.5.11 for the method of connection to a 64-Mbit DRAM with a 2M X 32-bit configuration.

[After]

Section 7 Bus State Controller(BSC)

7.2.7 Individual Memory Control Resister(MCR)

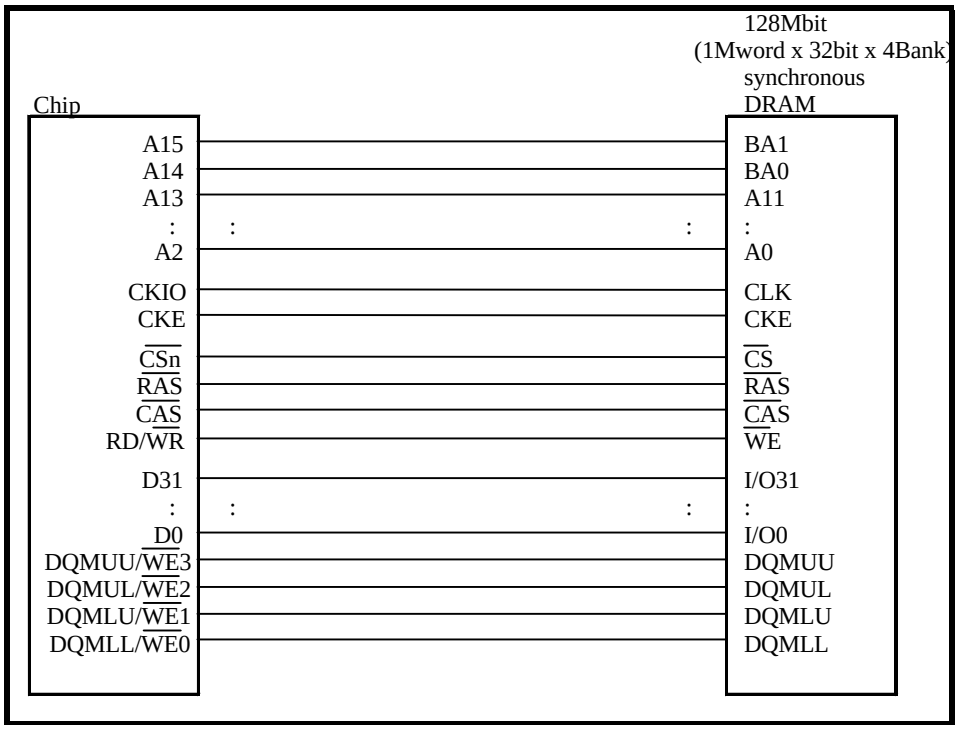
Figure1 128Mbit Synchronous DRAM (4Mword×32bit) Connection Example

● For synchronous DRAM interface

Bit7:AMX2	Bit5:AMX1	Bit4:AMX0	Description
0	0	0	16-Mbit DRAM(1M x 16bits), 64-Mbit DRAM(2M x 32bits) *2
		1	16-Mbit DRAM(2M x 8bits) *1
	1	0	16-Mbit DRAM(4M x 4bits) *1
		1	4-Mbit DRAM(256k x 16bits)
1	0	0	64-Mbit DRAM(4M x 16bits), 128-Mbit DRAM(4M x 32bits) *3
		1	64-Mbit DRAM(8M x 8bits) *1, 128-Mbit DRAM(8M x 16bits) *1 *4, 256-Mbit DRAM(8M x 32bits) *1 *5
	1	0	Reserved (do not set)
		1	2-Mbit DRAM(128k x 16bits)

Notes: 1. Reserved. Do not set when SZ bit in MCR is 0 (16-bit bus width).

2. See sction 7.5.11 for the method of connection to a 64-Mbit DRAM with a 2M X 32-bit configuration.
3. See Figure1 for the method of connection to a 128-Mbit DRAM with a 4M X 32-bit configuration.
4. In the case of a 128-Mbit DRAM(8M X 16-bit), connect to two 128M bit DRAMs (8M X 16-bit) by 32-bit data width as Figure2.
5. See Figure3 for the method of connection to a 256-Mbit DRAM with a 8M X 32-bit configuration.



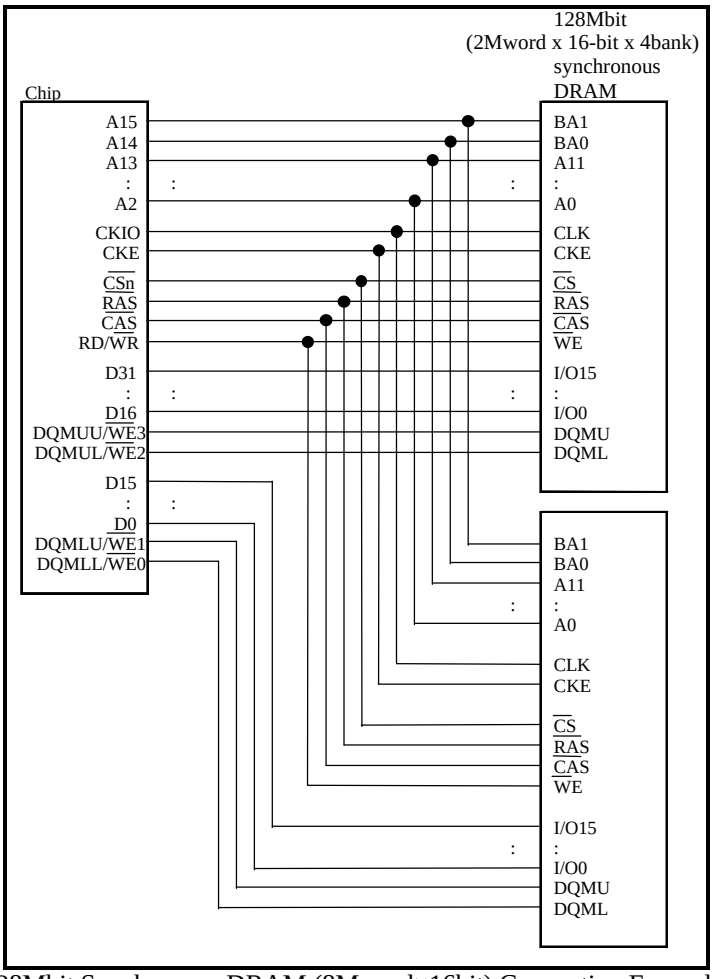


Figure2 128Mbit Synchronous DRAM (8Mword×16bit) Connection Example

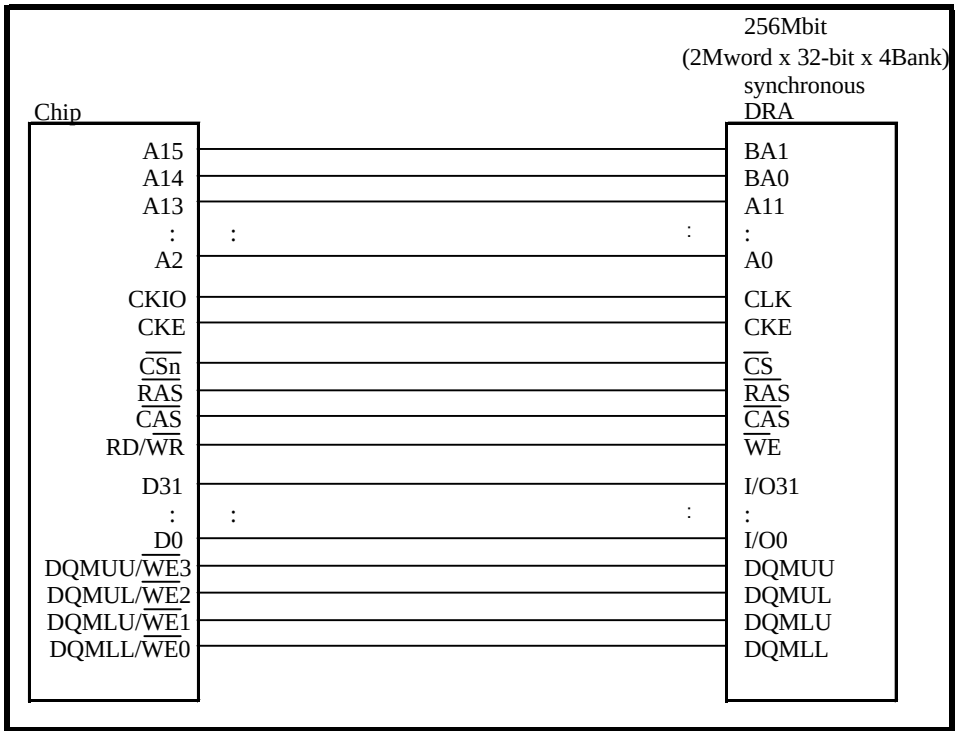


Figure3 256Mbit Synchronous DRAM (8Mword×32bit) Connection Example

[Mass production schedule]

It applies from the following Product Lot Code.

	Product Lot Code
HD6417615ARF :	3D1
HD6417615ARFV :	0314