# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-RX*-A021A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Addition and Change to Specifications regarding Settings for Main Clock Oscillator and PLL Wait Control Registers and Clock Oscillation Stabilization Wait Time | | Information Category | Technical Notification | | |
| Applicable Product | RX630 Group, RX63N Group RX631 Group, RX63T Group | Lot No. | Reference Document | User's Manual: Hardware for Applicable Products (see the table at the end of this document) | | |
| | | All | | | | |

This document describes addition and change to specifications regarding settings for main clock oscillator and PLL wait control registers and the clock oscillation stabilization wait time in the above applicable products.

(1)  Added detailed specifications of clock oscillation stabilization wait time.

(2)  Changed electrical characteristics of clock oscillation stabilization wait time.

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Setting the wait control register:

Set the main clock oscillator and PLL wait control registers to a value satisfying wait time listed in the table below.

Symbols for electrical characteristics are used in the table.

| Clock for Oscillation | | Wait Control Register | Wait Time |
|---|---|---|---|
| Main clock | | MOSCWTCR.MSTS[4:0] | Wait time ≥ tMAINOSC × fMAIN [cycle] |
| PLL clock | When the PLL starts operating after the main clock oscillation is stabilized | PLLWTCR.PSTS[4:0] | Wait time ≥ tPLL1 × fPLL [cycle] |
| | When the PLL starts operating before the main clock oscillation is stabilized | | Wait time ≥ (tMAINOSC + tPLL1) × fPLL [cycle] |

Clock oscillation stabilization wait time:

After the main clock oscillator and the PLL start oscillating, use the clock after the wait time listed in the table below.

Symbols for electrical characteristics are used in the table.

| Clock Used | | Oscillation Stabilization Wait Time | |
|---|---|---|---|
| | | Symbol | Description |
| Main clock | | tMAINOSCWT | If n = wait time selected by the MOSCWTCR.MSTS[4:0] bits, $tMAINOSC + \dfrac{n+16384}{fMAIN}$ |
| PLL clock | When the PLL starts operating after the main clock oscillation is stabilized | tPLLWT1 | If n = wait time selected by the PLLWTCR.PSTS[4:0] bits, $tPLL1 + \dfrac{n+131072}{fPLL}$ |
| | When the PLL starts operating before the main clock oscillation is stabilized | tPLLWT2 | If n = wait time selected by the PLLWTCR.PSTS[4:0] bits, $tMAINOSC + tPLL1 + \dfrac{n+131072}{fPLL}$ |

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(2)  Changed electrical characteristics of oscillation stabilization wait time.

Changed oscillator start-up time and oscillation stabilization wait time for the main clock and PLL clock in Electrical

Characteristics "Clock Timing" as follows:

Main clock

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Main clock oscillator start-up time | tMAINOSC | — | — | See Note 1 | ms |
| Main clock oscillation stabilization wait time | tMAINOSCWT | — | — | See Note 2 | ms |

Note 1: When using the main clock, request the oscillator manufacturer to evaluate the oscillator. Refer to the evaluation
results by the oscillator manufacturer for oscillator start-up time.

Note 2: If n = number of cycles selected by the MOSCWTCR.MSTS[4:0] bits, the main clock oscillation stabilization wait time
is calculated by the following formula:

$$tMAINOSCWT = tMAINOSC + \frac{n+16384}{fMAIN}$$

PLL clock

| Item | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| PLL lock time | The PLL starts operating after the main clock oscillation is stabilized | tPLL1 | — | — | 500 | µs |
| PLL clock oscillation stabilization wait time | | tPLLWT1 | — | — | See Note 1 | ms |
| PLL lock time | The PLL starts operating before the main clock oscillation is stabilized | tPLL1 | — | — | tMAINOSC + tPLL1 | ms |
| PLL clock oscillation stabilization wait time | | tPLLWT1 | — | — | See Note 1 | ms |

Note 1: If n = number of cycles selected by the PLLWTCR.PSTS[4:0] bits, the PLL clock oscillation stabilization wait time is
calculated by the following formulas:

$$tPLLWT1 = tPLL1 + \frac{n+131072}{fPLL}$$

$$tPLLWT2 = tPLL2 + \frac{n+131072}{fPLL} = tMAINOSC + tPLL1 + \frac{n+131072}{fPLL}$$

[Applicable products and related documents]

| Family | Group | Related Document | Rev. | Document No. |
|---|---|---|---|---|
| RX | RX630 | RX630 Group User's Manual: Hardware | 1.20 | R01UH0040EJ0120 |
| | RX63N, RX631 | RX63N Group, RX631 Group User's Manual: Hardware | 1.00 | R01UH0041EJ0100 |
| | RX63T | RX63T Group User's Manual: Hardware | 1.00 | R01UH0238EJ0100 |