RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A032A/E	Rev.	1.00
Title	Addendum for PFC Pin Function Settings of RZ/G1M		Information Category	Technical Notification		
Applicable Product	RZ/G Series, RZ/G1M	Lot No.	Reference Document	RZ/G1M User's Manual: Hardware Rev.1.00 Sep. 30, 2016 (R01UH0626EJ0100)		
		All lots				

There is a following addendum about the RZ/G1M user's manual: hardware.

[Summary]

  Addendum for PFC IPSR3 and IPSR6 HSCIF functions

[Products]

  RZ/G1M

[Note]

  There is no specification change (addendum only).

[Description]

  The following HSCIF pin functions of IPSR3 and IPSR6 registers are double assigned in one function number on the PFC. These bit allocations are correct and they can be specified by MOD_SEL and MOD_SEL3 registers. For details, refer to section 5.3.13, IPSR3, 5.3.16, IPSR6, 5.3.27 MOD_SEI and 5.3.29, MOD_SEL3.

  (Gray parts (abcd) are newly added.)

  IPSR3: IP3[11:9] Function 2, HRX2_B/HRX2_D* (RD/WR# pin)

  IPSR6: IP6[18:16] Function 2, HRX1_C/HRX1_E* (IRQ4 pin)

  IPSR6: IP6[20:19] Function 2, HTX1_C/HTX1_E* (IRQ5 pin)

- Addendum: Note. *: These pin functions can be specified by MOD_SEL and MOD_SEL3 registers.

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